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SCR MANUAL

INCLUDING TRIACS AND OTHER THYRISTORS

FIFTH EDITION

GENERAL ELECTRIC

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GENERAL ELECTRIC

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FOREWORD

TO THE FIFTEENTH ANNIVERSARY EDITION OF THE SCR MANUAL

Publication of this 5th Edition marks fifteen years since General Electric introduced the first commercial SCR. Though still a teenager, the SCR has grown to be the most prominent semiconductor device for static power conversion and control.

The fast-growing success of the SCR is paralleled by the growth of the General Electric SCR Manual. First published as an application note in 1958, the General Electric SCR Manual has been periodically revised, maintaining the basic theme of a practical, rather than theoretical, circuit and application guide for design engineers, students, teachers, and experimenters. This Edition is written by a group of engineers who, figuratively, live in the solid state power conversion arena. They are in constant touch with equipment designers and, as such, are exposed to the varied circuit problems and decisions peculiar to the application of power semiconductor devices. These authors have gained their insight and experience by contributing to literally thousands of successful design projects involving thyristors in addition to drawing on the experience and work of their predecessors.

The previous Edition has been completely reviewed in detail. Much that is new has been added, reflecting the polish that SCR applications have acquired in the past five years. These changes do not stand out as new chapters, rather, each chapter has had the additional or revised information blended in with that which remains current and valid. For those of you who have used previous editions the format remains intact to maintain any familiarity you may have developed.

The dual trends of increasing performance in military and industrial SCR's on the one hand and the shift to fabrication techniques which lend themselves to very high volume production of consumer and light industrial SCR's on the other hand are evident in the revisions to this manual. Considerably more detail is included on the parameters of SCR's along with application tips for the high performance SCR's. Information showing the designer how to approach optimum utilization of high volume, plastic encapsulated SCR's is also provided. Still, overall, considerable effort has been spent in keeping the SCR Manual concise and general in nature. For those desiring in-depth treatment of highly specialized subjects, we refer them to the comprehensive application notes listed on page **657**.

I sincerely hope that you will find this new Manual useful and informative.

H. D. Culley
General Manager
Semiconductor Products Department
Syracuse, New York

This 5th Edition of the SCR Manual is dedicated to one of the most competent and diverse groups of engineers ever listed on one page . . . the previous contributors to the SCR Manual, who helped lay the foundation for this fascinating technology.

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INTRODUCTION

We have not changed the SCR Manual for the sake of change. Rather we have folded into the fourth edition answers to questions which you, the equipment designers have been asking for the past few years. We have certainly included the device and circuit innovations of these past years. Finally, we have continued our past policy of presenting information in as clear, concise and uncomplicated a fashion as possible.

HOW TO LEARN ABOUT THE SCR

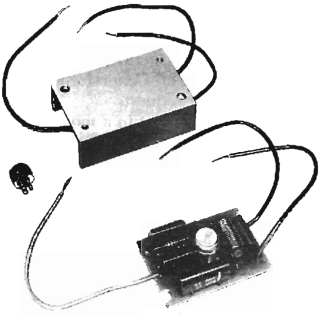
If you, the reader, are already familiar with the SCR and wish guidance in the design of practical applications, this Manual is ideal for your needs. If you wish more detailed information on a specialized subject, consider the references listed at the end of each chapter, as well as the comprehensive list of General Electric application notes (p.658) which are available on request.

If you wish to explore thyristors in a more analytical sense, either as a semiconductor or as a circuit element, we refer you to "Semiconductor Controlled Rectifiers . . . Principles and Applications of p-n-p-n Devices," a book published by Prentice-Hall, Englewood Cliffs, New Jersey.

If you have heard of the SCR but would like to start from scratch in learning how it can help you, we suggest that you obtain a copy of the General Electric "Electronics Experimenters' Circuit Manual." This manual describes some 40 ingenious circuits and projects useful in

teaching the fundamentals of electronics while constructing projects having lasting value in the automobile, home, workshop and campsite. This book was written by our application engineers on the assumption that the reader, although learned in his own field of competence, is new to the SCR and other semiconductors as well.

If you are really impatient to see how a basic thyristor circuit can work with your equipment load, or if you have no facilities to assemble your own circuit from electronic components, you may wish to experiment with one of several standard assemblies available from your G-E distributor. A typical standard triac variable voltage control is shown below. They are described further in Chapter 7.



A BRIEF DESCRIPTION OF THE SCR

The SCR is senior and most influential member of the thyristor family of semiconductor components. Younger members of the thyristor family share the latching (regenerative) characteristics of the SCR. They include the triac, bidirectional diode switch, the silicon controlled switch (SCS), the silicon unilateral and bilateral switches (SUS, SBS), and light activated devices like the LASCR and LASCS. Most recent additions to the thyristor family are the complementary SCR, the programmable unijunction transistor (PUT) and the "assymmetrical trigger."

Let's go back to the head of the family after whom this Manual was named. The SCR is a semiconductor . . . a rectifier . . . a static latching switch . . . capable of operating in microseconds . . . and a sensitive amplifier. It *isn't* an overgrown transistor, since it has far greater power capabilities, both voltage and current, under both continuous and surge conditions, and can control far more watts per dollar.

As a *silicon semiconductor*—the SCR is compact, static, capable of being hermetically sealed, or passivated, silent in operation and free from the effects of vibration and shock. A properly designed and fabricated SCR has no inherent failure mechanism. When properly chosen and protected, it should have virtually limitless operating life even in harsh atmospheres. Thus countless billions of operations can be expected, even in explosive and corrosive environments.

As a *rectifier*—the SCR will conduct current in only one direction. But this serves as an advantage when the load requires DC, for here the SCR serves both to control *and* rectify—as in a regulated battery charger.

As a *latching switch*—the SCR is an ON-OFF switch, unlike the vacuum tube and transistor which are basically variable resistances (even though they too can be used as on-off switches). The SCR can be turned on by a momentary application of control current to the gate (a pulse as short as a fraction of a microsecond will do), while tubes or transistors (and the basic relay) require a continuous ON signal. In short the SCR *latches* into conduction, providing an inherent memory useful for many functions. The SCR can be turned ON in about one microsecond, and OFF in 10 to 20 microseconds; further improvements in switching speed are being made all along.

Just as a switch or relay contact is commonly rated in terms of the current it can safely carry and interrupt, as well as the voltage at which it is capable of operating, the SCR is rated in terms of peak voltage and forward current. General Electric offers a complete family of SCR's with current carrying capacities from 1/4 amp to 1600 amps RMS, and up to 2600 volts at this writing. Higher voltage and current loads are readily handled by series and parallel connection of SCR's.

As an *amplifier*—the smallest General Electric SCR's can be latched into conduction with control signals of only a few microwatts and a few microseconds duration. These SCR's are capable of switching 100's of watts. The resulting control power gain of over 10 million makes the small SCR one of the most sensitive control devices available. With a low cost unijunction transistor firing circuit driving the larger SCR's, stable turn-on control power gains of many billions are completely practical. This extraordinary control gain makes possible inexpensive control circuits using very low level signals, such as produced by thermistors, cadmium sulfide light sensitive resistors, and other transducers.

Most of the foregoing list of assets of the SCR apply equally well to the other members of the thyristor family as you will see in this Manual. Meanwhile the shortcomings and limitations of thyristors become less significant as the years pass. Newly introduced high voltage and bidirectional types lift the transient and operating voltage barriers. High speed thyristors allow operation at ultrasonic frequencies and under severe dynamic conditions, and lower semiconductor costs permit use of higher current rated thyristors instead of critically designed and expensive overcurrent protection systems.

Best of all, SCR's and thyristors for every type of application . . . industrial, military, aerospace, commercial, consumer . . . are *more economical than ever.* Best indication of this is the rapidly increasing tempo of applications of the new plastic-encapsulated thyristors in high volume consumer applications where every penny is critical.

Here are just some of the conventional types of controls and elements that thyristors are busy replacing and improving upon:

Thyratrons
Relays
Magnetic Amplifiers
Ignitrons
M-G Sets
Rheostats
Power Transistors
Motor Starters
Transformers
Limit Switches
Constant Voltage Transformers
Saturable Reactors
Contactors
Variable Autotransformers
Fuses
Timers
Vacuum Tubes
Thermostats
Mechanical Speed Changers
Centrifugal Switches
Ignition Points

Welcome to the exciting world of the thyristor family, its circuits and applications. Please bear in mind that the material in this Manual is intended only as a general guide to circuit approaches. It is not all-encompassing. However, our years of experience in offering application help have shown that, given some basic starting points like those in this Manual, you the circuit designer inevitably come up with the best, and often unique, approach for your particular problems.

We, in particular, would like to direct your attention to Chapter 20, "Selecting the Proper Thyristor and Checking the Completed Circuit Design." Here, we have tried to pull together a roadmap of the route to successful design with thyristors avoiding the pitfalls we, and others, have learned the hard way.

You will find the "Application Index" on pages 671 a useful guide in starting the search for the ideal circuit for your application. The list of Application Notes starting on page 674 will also provide specialized help beyond the detail of this Manual.

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1 CONSTRUCTION AND BASIC THEORY OF OPERATION

1.1 WHAT IS A THYRISTOR?

The name thyristor[1] defines any semiconductor switch whose bistable action depends on p-n-p-n regenerative feedback. Thyristors can be two, three, or four terminal devices, and both unidirectional and bi-directional devices are available.

1.2 CLASSIFICATIONS OF THYRISTORS

The silicon controlled rectifier (SCR) is by far the best known of all thyristor devices. Because it is a unidirectional device (current flows from anode to cathode only) and has three terminals (anode, cathode and control gate), the SCR is classified as a *reverse blocking triode thyristor*. Other members of the reverse blocking triode thyristor family include the silicon unilateral switch (SUS), the light activated silicon controlled rectifier (LASCR), the complementary SCR (CSCR), the gate turn-off switch (GTO), and the programmable unijunction transistor (PUT). The silicon controlled switch (SCS) is a reverse blocking *tetrode* thyristor (it has two control gates), while the Shockley diode is a reverse blocking diode thyristor. Bidirectional thyristors are classified as p-n-p-n devices that can conduct current in either direction; commercially available bidirectional triode thyristors include the triac (for *tri*ode *AC* switch), and the silicon bilateral switch (SBS).

1.3 TWO TRANSISTOR ANALOGY OF p-n-p-n OPERATION[2]

A simple p-n-p-n structure, like the conventional SCR, can best be visualized as consisting of two transistors, a p-n-p and an n-p-n interconnected to form a regenerative feedback pair as shown in Figure 1.1.

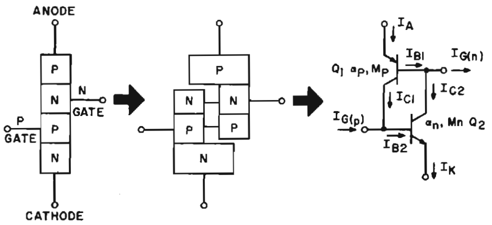


FIGURE 1.1 TWO TRANSISTOR ANALOGUE OF P-N-P-N STRUCTURES

From this figure, it is evident that the collector of the n-p-n transistor (along with possible n-gate drive) provides base drive for the p-n-p transistor.

$$I_{B1} = I_{C2} + I_{G(n)} \tag{1.1}$$

Similarly, the collector of the p-n-p transistor along with any p-gate current ($I_{G(p)}$) supplies the base drive for the n-p-n transistor.

$$I_{B2} = I_{C1} + I_{G(p)} \tag{1.2}$$

Thus, a regenerative situation exists when the positive feedback gain exceeds one.

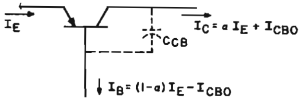


FIGURE 1.2 COMMON BASE CURRENT RELATIONSHIPS

The p-n-p-n structure may be analyzed in terms of its common base current gains (α_p and α_n) and the avalanche multiplication coefficients of holes and electrons, M_p and M_n respectively. From 1.2, the base current for the n-p-n transistor is seen to be:

$$I_{B2} = I_K\,(1 - \alpha_n\,M_n) - I_{CBO(2)} \tag{1.3}$$

where $I_{CBO(2)}$ is the collector-to-base leakage current of transistor Q_2. However, the collector current of the p-n-p is:

$$I_{C1} = \alpha_p\,M_p\,I_A + I_{CBO(1)} \tag{1.4}$$

But since

$$I_{B2} = I_{C1} + I_{G(p)} \tag{1.5}$$
$$I_A + I_{G(p)} = I_K + I_{G(n)} \tag{1.6}$$

Equations 1.3 to 1.6 can be solved for

$$I_A = \frac{\alpha_n\,M_n\,I_{G(p)} + I_{G(n)}\,(1 - \alpha_p\,M_p) + I_{CBO(1)} + I_{CBO(2)}}{1 - \alpha_p\,M_p - \alpha_n\,M_n} \tag{1.7}$$

Call "$\alpha_p\,M_p + \alpha_n\,M_n$" the loop gain G.

With proper bias applied (positive anode to cathode voltage) and in the absence of any gate signal, M_n and M_p are approximately unity and the transistor alphas are both low. The denominator of Equation 1.7 approaches one, and I_A is little higher than the sum of the individual transistor leakage currents. Under these conditions the p-n-p-n structure is said to be in its *forward blocking* or high impedance "off" state. The switch to the low impedance "on" state is initiated simply by raising the loop gain to unity. Inspection of Equation 1.7 shows that as this term $\rightarrow$ 1, $I_A \rightarrow \infty$. Physically, as the loop gain approaches unity and the circuit starts to regenerate, each transistor drives its mate

into saturation. Once in saturation, all junctions assume a forward bias, and total potential drop across the device approximates that of a single p-n junction. Anode current is limited only by the external circuit.

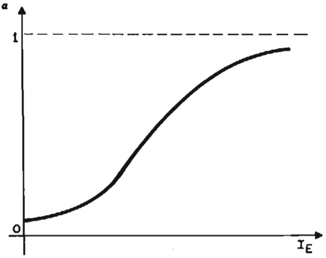


FIGURE 1.3 EMITTER CURRENT DEPENDENCE OF α IN A SILICON TRANSISTOR

The loop gain G can approach one (1) either by an increase in M_p or M_n with increasing voltage or with an increase in the alphas with either voltage or current. In most silicon transistors, α is quite low at low emitter currents, but increases fairly rapidly as emitter current is increased. This effect (Figure 1.3) is due to the presence in the silicon of special impurity centers. Any mechanism which causes a temporary increase in transistor emitter current is therefore potentially capable of turning on a p-n-p-n device. The most important of these mechanisms are:

1. Voltage. As the collector-to-emitter voltage of a transistor is increased, eventually a point is reached where the energy of the (leakage) current carriers arriving at the collector junction is sufficient to dislodge additional carriers. These carriers in turn dislodge more carriers, and the whole junction goes into a form of avalanche breakdown characterized by a sharp increase in collector current. In a p-n-p-n device, when the avalanche current makes $G \rightarrow 1$, switching takes place. This is the turn-on mechanism normally employed to switch four layer diodes into conduction.

2. Rate of change of voltage. Any p-n junction has capacitance – the larger the junction area, the larger the capacitance. Figure 1.2 shows the collector-to-base capacitance dotted in. If a step function of voltage is impressed suddenly across the collector-to-emitter terminals of the transistor, a charging current i will flow from the emitter-to-collector to charge the device capacitance

$$i = C\,dv/dt \tag{1.8}$$

In Figure 1.1, the charging current flowing in the p-n-p represents base current for the n-p-n so that G can rapidly approach 1, switching on the device.

3. Temperature. At high temperatures, leakage current in a reverse biased silicon p-n junction doubles approximately with every 8°C increase in junction temperature. When the temperature generated

leakage current in a p-n-p-n structure has risen sufficiently for $G \rightarrow 1$, switching occurs.

4. Transistor Action. Collector current is increased in conventional transistor manner by temporarily injecting additional ("gate") current carriers into a transistor base region. This is the machanism normally employed to turn-on SCR's and other p-n-p-n devices which have an external connection ("gate" lead) to one or more of the transistor bases.

By convention, SCR's that are turned on by injecting current into the lower p-base (via an external connection to this base) are called "conventional" SCR's, while those that withdraw current from the upper n-base are called "complementary" SCR's. The four-terminal silicon controlled switch (SCS) has connections made to *both* bases and either or both bases may be used to initiate switching. More external gate current is required to trigger a p-n-p-n device via the n-gate rather than the p-gate for two reasons:

a) The upper n-base region is of high resistivity silicon (the upper p-n junction supports the major part of any applied reverse voltage) so that α_p is very small.
b) From Figure 1.1, n-base drive necessarily removes current from the loop and therefore reduces G.

5. Radiant energy ("light"). Incident radiant energy within the spectral bandwidth of silicon impinging on and penetrating into the silicon lattice releases considerable numbers of hole electron pairs. When the resultant device leakage current climbs above the critical level for $G \rightarrow 1$, triggering will ensue. This triggering mechanism makes possible the light activated SCR. In these devices a translucent "window" is provided in the device encapsulation in order that "light" may reach the silicon pellet. The LASCR, because it is provided with a gate lead, may be triggered either by light or by electrical gate current. Chapter 14 is devoted to light activated thyristors.

1.4 REVERSE BLOCKING THYRISTOR (SCR) TURN-OFF MECHANISM

When a reverse blocking thyristor is in the conducting state, each of the three junctions of Figure 1.4 are in a condition of forward bias and the two base regions (B_P, B_N) are heavily saturated with holes and electrons (stored charge).

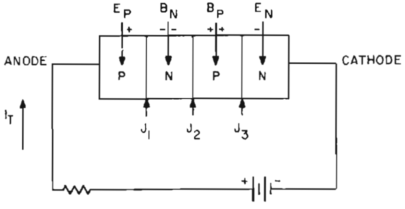


FIGURE 1.4 THYRISTOR BIASED IN CONDUCTING STATE (GATE OPEN CIRCUITED)

To turn-off the thyristor in a minimum time, it is necessary to apply a reverse voltage. When this reverse voltage is applied the holes and electrons in the vicinity of the two end junctions (J_1, J_3) will diffuse to these junctions and result in a reverse current in the external circuit. The voltage across the thyristor will remain at about +0.7 volts as long as an appreciable reverse current flows. After the holes and electrons in the vicinity of J_1 and J_3 have been removed, the reverse current will cease and the junctions J_1 and J_3 will assume a blocking state. The reverse voltage across the thyristor will then increase to a value determined by the external circuit. Recovery of the device is not complete, however, since a high concentration of holes and electrons still exists in the vicinity of the center junction (J_2). This concentration decreases by the process of recombination in a manner which is largely independent of the external bias conditions. After the hole and electron concentration at J_2 has decreased to a low value, J_2 will regain its blocking state and a forward voltage (less than $V_{(BO)}$) may be applied to the thyristor without causing it to turn-on. The time that elapses after the cessation of forward current flow and before forward voltage may safely be reapplied is called the thyristor "turn-off time," t_q and can range from several microseconds to as high as several hundred microseconds depending upon the design and construction of the particular thyristor.

1.5 IMPROVEMENTS FOR DYNAMIC SCR OPERATION

Ever since its introduction, circuit design engineers have been subjecting the SCR to increasing levels of operating stress and demanding that these devices perform satisfactorily there. Different stress demands that the SCR must be able to meet are:

1) Higher blocking voltages
2) More current carrying capability
3) Higher di/dt's
4) Higher dv/dt's
5) Shorter turn-off times
6) Lower gate drive
7) Higher operating frequencies

There are many different SCR's available today, which can meet one or more of these requirements. But as always, an improvement in one characteristic is usually only gained at the expense of another. It is constructive to consider five device attributes which in combination determine the thyristor's current rating and switching capability.

1. Voltage. There are four methods to increase the voltage rating — surface contouring, increasing the B_n base width and/or its resistivity, and/or its lifetime.

a) Surface contouring or beveling allows higher voltage operation by reducing the electric fields at the surface of the silicon pellet. It is the most advantageous since it achieves this with no other sacrifice in SCR operation except for a slight current derating due to decreased emitter area. Beveling techniques generally are used only on premium-type industrial devices,

where the added costs due to a bigger silicon pellet plus the requirement that the pellet be round for maximum beveling effectiveness can be justified. Consumer type devices whose pellets generally are "scribed" into square or rectangular shapes for lowest cost are generally not beveled. Beveling effectiveness here is destroyed by field concentration effects at the pellet corners.

b) The most obvious way to increase the voltage rating is to increase the base width B_n (see Section 1.4) or its resistivity. However, these actions will also increase the "on-state" voltage drop so that the allowable current decreases. High frequency performance is degraded because the di/dt rating goes down and turn-off time increases due to increased stored charge in this base.

c) A more subtle way is to increase the minority carrier lifetime in B_n. This decreases the thermally generated leakage current in the depletion region (I_{CBO}). Additional benefits are lower "on-state" voltage and better di/dt rating. Of course, turn-off time will also increase and dv/dt withstand capability decreases (see also Section 5 below, Turn-Off Time).

2. Current. The allowable current through a device depends primarily upon the "on-state" voltage. Any variable that decreases this voltage drop (and hence, internal power dissipation), will raise the current limit. Favorable effects are larger pellets, smaller B_n base width, higher lifetimes, and lower silicon resistivity.

3. di/dt. The problem of di/dt failures is well recognized today.[3] Essentially the SCR is trying to conduct too much current through too small a pellet area during the initial turn-on and the resultant, localized junction temperature rise burns it out. The obvious answer is to have the SCR turn on more area initially and this is precisely the objective of the newer gate structures discussed below.

a) Conventional Side Gate or Point Gate (Figure 1.5(a)). This is inherently the simplest gate structure and provides adequate performance for low di/dt applications. The area initially turned on is quite small and depends upon the amplitude of the gating signal. All of the early SCR's had a point contact gate and it is still the most common gate amongst the consumer and light industrial SCR's.

b) Conventional Center Gate (Figure 1.5(b)). Same as the conventional side gate except the di/dt ratings are generally higher due to the fact that a small circle rather than a point is turned on. Di/dt capability is still quite a strong function of gate drive.

c) Field Initiated (F.I.) Gate (Figure 1.5(c)). This gate structure is designed to turn on a definite length of SCR emitter periphery even with soft gate drive. The F.I. gate is a double switching type gate. That is, from an equivalent circuit view, it behaves as a main SCR triggered by a small pilot SCR. A portion of the anode current of the pilot SCR becomes the gate drive to the main. By this technique, only a small amount of gate drive is required to initiate conduction in the pilot portion of the SCR. With this type of structure, delay time is a

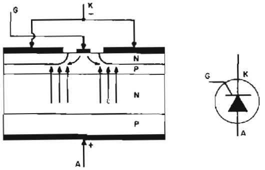


FIGURE 1.5(a) CONVENTIONAL SIDE GATE SCR

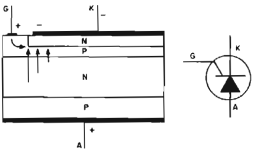


FIGURE 1.5(b) CONVENTIONAL GATE SCR

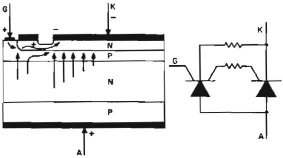


FIGURE 1.5(c) F-1 GATE SCR

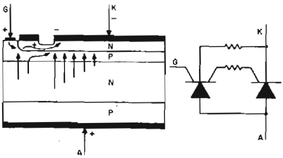


FIGURE 1.5(d) N+ GATE SCR

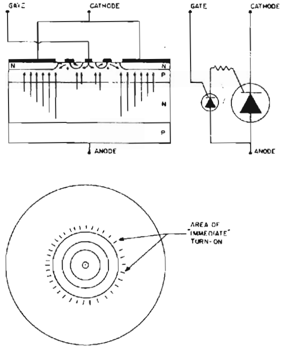


FIGURE 1.5(e) JUNCTION DIAGRAM, PLAN VIEW AND EQUIVALENT CIRCUIT FOR AMPLIFYING GATE SCR

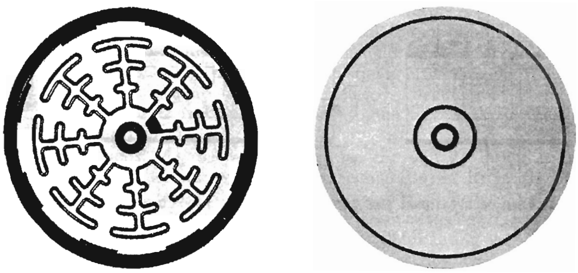


FIGURE 1.5(f) THE INTERDIGITATED AMPLIFYING GATE STRUCTURE IS SHOWN ON THE LEFT COMPARED TO THE CIRCULAR AMPLIFYING GATE

strong function of gate drive. Even though high di/dt is achieved with soft drive, the circuit designer may be forced to provide a stiff gate drive to achieve relatively short delay time.

d) N+ Gate (Figure 1.5(d)). This gate structure is designed to turn-on a definite length of line, but not with soft gate drive; here a stiff drive is required. However, with this structure a consistently short delay time is achieved. This enhanced parameter along with others makes SCR's fabricated with the N+ gate ideal for applications requiring series and/or parallel operation of SCR's.

e) Amplifying Gate (Figure 1.5(e)). The principals involved in the amplifying gate are quite similar to those employed in the F.I. structure. That is, double switching is employed but optimized to the point where the main SCR portion switches immediately after conduction is initiated in the pilot portion of the device. The anode current of the pilot portion of the device causes rapid turn-on of a significant portion of the main current-carrying portion of the device. The three most important criteria to building an optimized amplifying gate SCR are:

1. Complete turn-on of the emitter periphery of the main current-carrying area to insure low switching loss density.
2. Instantaneous turn-on of the main current-carrying area after turn-on of the pilot area.
3. Complete turn-on of the pilot portion of the device.

The design of the amplifying gate structure optimizes these three criteria. To initiate turn-on, only a relatively small amount of conventional gate current is required due to the pilot SCR action — thus the term "amplifying." Schematically, the amplifying gate SCR looks like a main power handling SCR triggered by a small "pilot" SCR. The area of immediate turn-on is sizeable as shown on the plan-view of the pellet structure as shown in Figure 1.5(e).

f) Distributed Amplifying Gate (Figure 1.5(f)). Although it is possible to turn on a ring around the amplifying gate as previously described, a finite spreading velocity requires a finite period of time before conduction moves out from the periphery of the amplifying gate to cause the entire annular portion of the thyristor to be "on." Depending on the designed voltage and speed characteristics of a thyristor, the spreading velocity can range anywhere from 3000 to 8000 cm/second.[5] This represents spreading times of 50 μseconds for a 110 ampere device to better than 300 μseconds for a 550 ampere device. One can appreciate that for narrow pulses (less than the above times) something less than the entire pellet is in conduction and wide pulse current capability cannot be realized.

The solution employed to extend the amplifying gate principle to thyristors designed for narrow pulse application is interdigitation. Figure 1.5(f) shows the extension of the amplifying gate technology to include interdigitation. The fingers extending out into the cathode area increase the gate periphery from something a little better than 2 cm to about 33 centimeters. The distance now which spreading must traverse is much reduced so that total turn-on occurs in something on the order of 10 to 30 μseconds. Of course the region for conduction is much reduced with interdigitation but "who cares?"; you wouldn't use any more for narrow pulses and you wouldn't use an interdigitated device for wide pulses. The previously mentioned non-interdigitated devices are much superior for wide pulse applications.

4. dv/dt. It was mentioned in Section 1.3 that a rapidly rising voltage waveform could switch on an SCR. Since this can lead to spurious operation, SCR's to be used in circuits with high dv/dt's should be of the "shorted emitter" construction with its intrinsic high dv/dt withstand capability.[9]

Figure 1.6 shows a "shorted emitter" thyristor structure. Externally applied gate current I_G flows from gate to cathode *laterally* through the gate p-region. The voltage drop developed across the lateral base resistance of p forward biases the right hand edge of the cathode junction. If gate current is sufficiently large, electrons are injected from this point, and the device turns on in normal p-n-p-n fashion when regeneration begins.

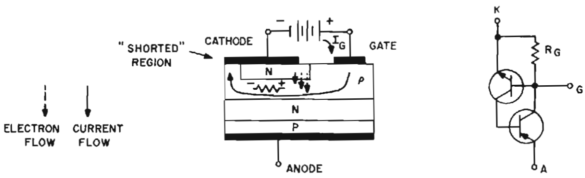


FIGURE 1.6 SHORTED EMITTER STRUCTURE

The effect of the partial gate to cathode short is the same as placing a resistor in parallel with the gate cathode junction of a conventional non-shorted emitter device.[2] This resistor (R_G in Figure 1.6) diverts some of the thyristor's thermally generated leakage current and/or dv/dt induced capacitive charging current around the gate-cathode junction, by providing an alternative lower impedance path to the cathode. Regeneration is reduced and a shorted emitter thyristor has, as a result, superior high temperature characteristics and dv/dt capability. Emitter shorts reduce the emitter area that can conduct principle current and also interfere with the turn-on of the device, thereby reducing di/dt.[5]

5. Turn-off Time (t_q). Section 1.4 pointed out that the stored minority charge in the B_n base must decay to zero by recombination before forward voltage may be applied to the SCR without its turning on. This recombination effect can be represented by the simple formula

$$- \frac{dp_n}{dt}_{\text{recomb}} = \frac{p_n}{\tau_p} \tag{1.9}$$

where p_n is the excess minority charge (holes in this case) and τ_p is the lifetime of holes in the B_n base. Representative values of τ_p range from 0.1 to 1000 μseconds and depend upon purity, structure and doping of the silicon. High frequency operation requires short turn-off times so that τ_p must be made small. The usual way is by gold doping, i.e. the introduction of gold impurities into B_n, which act as additional recombination centers. However, as mentioned before, as τ_p goes down, so does the voltage and current ratings. α_p also is reduced so that more gate drive may be required as well.

6. Gate Current. In designing thyristors for high frequency applications, almost all of the structure changes which are introduced tend to require greater gate drive. Lowering the carrier lifetime to obtain short turn-off time, introducing a shorted emitter to obtain improved dv/dt, increasing the amount of cathode periphery, use of an n^+ gate to reduce delay time, all of these modifications require increased gate current. The amplifying gate mentioned above overcomes some of these problems.

7. High Frequency Operation. High frequency operation stretches all of the SCR ratings to their limits. The circuit subjects the SCR concurrently to high di/dt's, high dv/dt's, and short turn-off times, not to mention high voltage and current. From the previous discussion, it should be evident that short turn-off times often conflict with low on-state voltages; shorted emitter construction which allows high dv/dt, lowers di/dt. Thus the device designer's goal is to provide a design which has a balanced set of attributes to maximize the power switching capability of the device while maintaining gate trigger control.

1.6 V-I CHARACTERISTICS OF REVERSE BLOCKING TRIODE OR TETRODE THYRISTORS

Figure 1.7 illustrates the V-1 characteristics of a typical gate-controlled reverse blocking thyristor. In the forward blocking region,

increasing the forward voltage does not tend to increase leakage current until the point is reached where avalanche multiplication begins to take place. Past this point, the leakage current increases quite rapidly until the total current through the device is sufficient to raise the internal loop gain $\geqq 1$. At this point the device will go into the high conduction region, provided that anode current remains in excess of a minimum value called the *holding current.* When anode current drops below the holding current, the internal loop gain goes to less than 1 and the p-n-p-n device reverts to its forward blocking state. In the reverse direction, the p-n-p-n structure looks like two reverse-biased p-n junctions in series, so that it exhibits characteristics very similar to an ordinary back-biased silicon rectifier. For most commercially available devices (SCR, SCS, LASCR, four layer diode), the peak *reverse* voltage capability is designed to be at least equal in magnitude to the minimum forward breakover voltage.

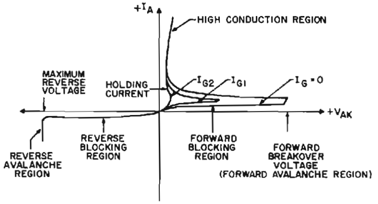


FIGURE 1.7 V-I CHARACTERISTICS OF A REVERSE BLOCKING THYRISTOR

For increasing magnitudes of gate current, the region of characteristics between breakover current and holding current (Figure 1.7) is narrowed and the forward breakover voltage is reduced. For sufficiently high gate currents, the entire forward blocking region is removed, and the V-I characteristics are essentially identical to those of a p-n rectifier.

In typical operation the reverse blocking thyristor is biased well below its minimum forward breakover voltage, and triggering is accomplished by injecting current into the gate lead. ("Light" is of course used in place of gate current to trigger the LASCR.) This is a very advantageous mode of operation, since it is possible to use a device with a forward breakover voltage much higher than any voltage likely to be encountered in the circuit, and to use only a moderate amount of trigger power to start the high conduction state. Circuit design and reliability are thus greatly enhanced. Once the gate has been used to trigger the thyristor into conduction it loses control, and the only method of turning a conducting device off is to reduce anode current below the holding current level. *(This applies to LASCR likewise, once it has been triggered.) Typically a two to fifty microsecond gate pulse will initiate conduction.

*The gate turn-off switch (GTO), as its name suggests, can be turned off by means of its gate terminal. See Section 1.7.

As already mentioned, leakage current through a thyristor increases with temperature. The forward breakover voltage therefore tends to be quite temperature sensitive. At a high enough temperature (well above its maximum *rated* temperature) the thyristor loses completely its ability to block forward voltage and assumes characteristics just like a p-n diode.

In smaller SCR's, SCS's, or LASCR's this temperature effect on the breakover voltage can be minimized by extracting the forward leakage current from the gate. This prevents current from passing through the emitter of the n-p-n section of the device and maintains a low alpha in this section. It is also possible to actually increase the forward breakover voltage point on some small SCR's by this means. The effect of negative gate current on the forward blocking characteristics, however, becomes negligible on higher current SCR's (except for interdigitated gate structures) due to the ineffectiveness of the gate in removing leakage current from the entire broad area of the n-p-n base region. (See also Chapter 4, for more details.)

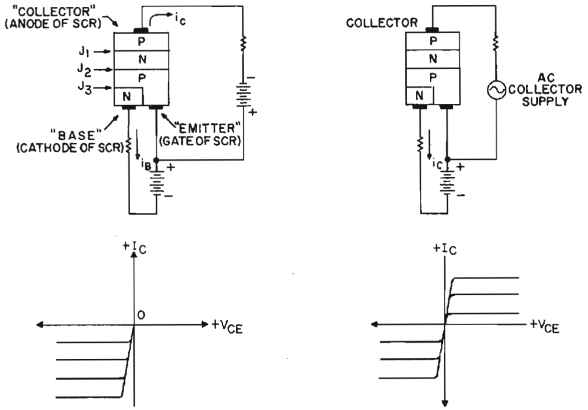
As might be expected, the gate cathode V-I characteristics of a gate-operated thyristor are essentially those of a p-n junction diode. Since the increase in h_{FE} with current is utilized, these devices are *current triggered* as opposed to voltage triggered, like a gas thyratron. This distinction must be kept in mind when designing triggering circuits, in that a relatively low impedance voltage source or a current source is required.

1.7 GATE TURN-OFF SWITCH OR GATE CONTROLLED SWITCH

The gate turn-off switch is a four layer p-n-p-n device similar in construction to the SCR. Like the SCR, the GTO is triggered into conduction by raising its loop gain to unity. In the simple two transistor p-n-p-n analogue of Figure 1.1 with the device switched on, assume that α_p equals α_n so that equal currents flow in each transistor section. If the p-n-p transistor's collector current were diverted away from the n-p-n transistor's base region and out of the gate lead, the n-p-n transistor would be cut-off, and the p-n-p-n device would revert to its forward blocking state. Turn-off gain, defined as the ratio of anode current flowing prior to turn-off to negative gate current required to effect turn-off, would be at least two (2) in this case. If α_p is now made much less than unity when the device is in its "on" state, and α_n is made about equal to unity to maintain $\alpha_n + \alpha_p = 1$, only a small percentage of the total anode current will flow in the collector of the p-n-p transistor. It is this current that is withdrawn to turn the GTO "off." For a typical device, gains from 5 to 25 are realizable depending on current, temperature gate pulse duration and other variables. Because of the difficulties in ensuring that control can be maintained by the gate contact at high cathode current densities (due to cross-biasing effects), gate turn-off devices operate at much lower current densities than SCR's and are therefore less economical. In addition, the recent availability of high voltage high gain silicon power transistors with superior saturation ("on" voltage) characteristics has tended to reduce the demand for gate turn-off devices.

1.8 THYRISTOR USED AS A REMOTE BASE TRANSISTOR

As already described, a reverse blocking thyristor structure may be visualized as consisting of two interconnected transistors. When the structure is conventionally biased, i.e., *positive* anode to cathode voltage, *positive* gate to cathode voltage, the transistors act as a regenerative pair and give the p-n-p-n device its normal bistable characteristics. A p-n-p-n structure may be biased, however, so that the transistors are *unable* to regenerate, and in this case the bistable action is eliminated. The device, when so biased, exhibits the linear characteristics of an amplifier. Referring to Figure 1.8, a negative bias on the base lead with respect to the emitter lead causes electrons to be injected across junction J3 for collection at J2. Upon collection at J2 these electrons furnish base drive for the p-n-p section in much the same way as if a lead were attached directly to it. Hence the name "remote base" transistor. When the anode is biased positively, junction J_1 is forward biased and the SCR acts just like a normal n-p-n transistor. Common-emitter current gains (beta) vary from much less than unity to above five (5), depending on the characteristics of the parent p-n-p-n device, specifically holding current. Since in most cases α_1 is small compared to α_2, the devices are also usable as symmetrical AC amplifiers or switches.



(a) p-n-p-n Structure Biased as p-n-p Transistor

(b) p-n-p-n Structure Used as Symmetrical Transistor

FIGURE 1.8 REMOTE BASE TRANSISTOR

1.9 THYRISTOR CONSTRUCTION

The successful and reliable operation of a thyristor is predicated on its proper design and construction. The fabrication methods chosen for a particular thyristor type depend a great deal therefore on the service expected from that type. A seventy ampere SCR destined for use in a harsh military environment may differ radically in design from a six ampere triac intended for the light industrial or consumer markets.

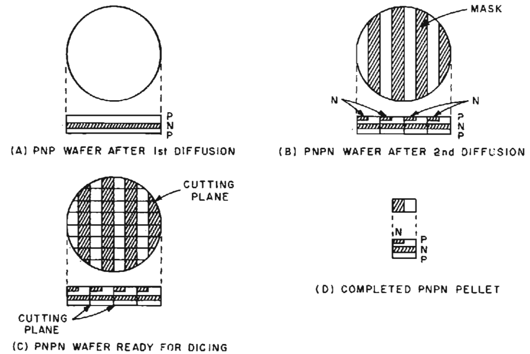


FIGURE 1.9 ALL-DIFFUSED PELLET FORMATION

1.9.1 Pellet Fabrication

The heart of a p-n-p-n device is its multi-layered "pellet" of alternate p and n type semiconductor material. This semiconductor is almost always silicon, although germanium has been used. Pellets may be fabricated by any one of several methods, depending on the desired characteristics, complexity, and size of the finished device. The most popular pellet fabrication methods are:

Alloy diffused
Diffused
Planar-diffused

The manufacture of both alloy-diffused and all-diffused p-n-p-n pellets starts with the preparation of large area *p-n-p wafers*. These are formed by gaseously diffusing p-type impurities simultaneously into both faces of a thin wafer of n-type silicon. Where specific device characteristics require it, a second diffusion step is used to complete the final p-n-p-n structure. To do this, each p-n-p wafer is selectively masked (on one side only), and subsequently diffused with n-type impurities through the windows in the mask. The finished p-n-p-n wafers are then diced into individual pellets. Triacs and other more complex structures are fabricated using similar techniques. In the manufacture of some higher current SCR's, where only a limited number of pellets (sometimes only one) can be obtained from each wafer, it is often more convenient to

pelletize the original p-n-p wafers *before* adding the final n-region. Where this is the case, precision alloying techniques are used after pelletizing to fuse a gold-antimony preform into each p-n-p pellet, thus forming the required p-n-p-n structures. Figure 1.9 shows the cross section of a typical all-diffused SCR structure, while Figure 1.10 is a pictorial of an alloy-diffused type.

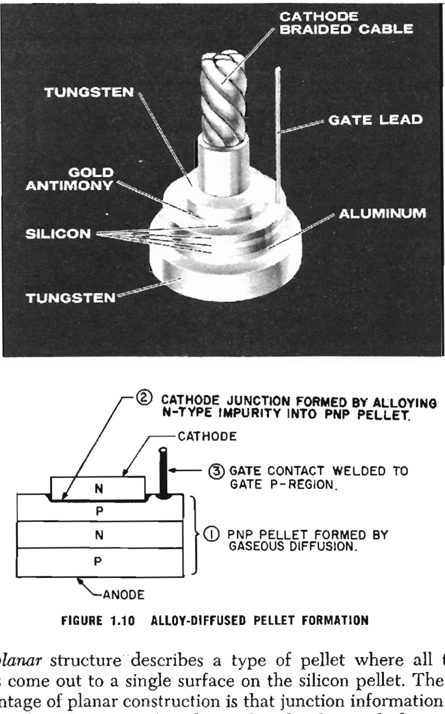


FIGURE 1.10 ALLOY-DIFFUSED PELLET FORMATION

A *planar* structure describes a type of pellet where all the p-n junctions come out to a single surface on the silicon pellet. The principal advantage of planar construction is that junction information always takes place (see Figure 1.11) underneath a thin layer of silicon dioxide grown over the silicon wafer before diffusion commences which prevents contamination of the silicon surfaces. As a result planar pellets are to a large degree protected from the outside environment — hence the term "planar-passivated." Disadvantages of planar construction are that more silicon is required per ampere of current carrying capability, and that more wafer processing steps are needed. Planar structures are best suited therefore to low current devices where many pellets can be obtained from a single wafer.

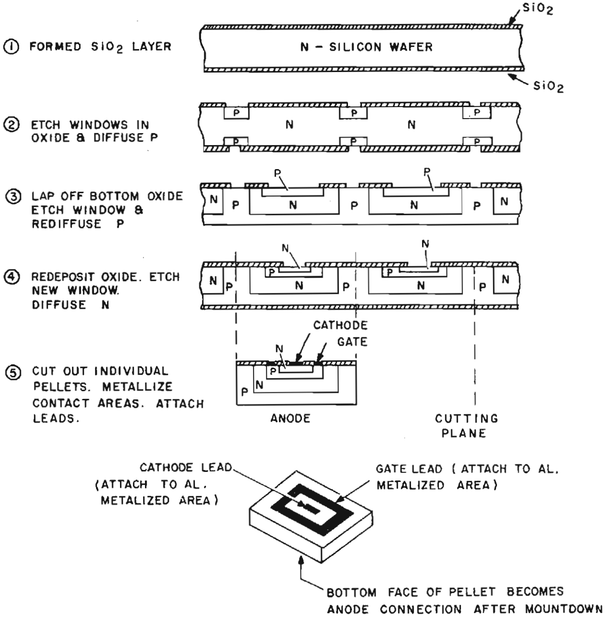


FIGURE 1.11 TYPICAL PLANAR PNPN PELLET FABRICATION (Geometry exaggerated for clarity)

1.9.2 Pellet Encapsulation

Pellet encapsulation methods vary widely, depending upon the in-service environment and circuit operating conditions imposed upon the finished device and on the type of pellet being encapsulated.

Two different encapsulation methods are used to house pellets which must operate over a very wide temperature range, or where severe thermal cycling is expected. The older, more traditional method is to hard solder the pellet between a pair of thermally matched back-up plates, one of which is then hard soldered to a copper stud. The copper stud serves as one terminal, the base for the device housing, and the thermal path for conducting heat losses to the ambient. For this latter reason the stud is usually threaded or bolted to a heatsink. Use of hard solder with this type of construction minimizes the possibility of thermal

fatigue destroying the joint between copper and back-up plate when the thyristor is subjected to the temperature induced stresses of wide and frequent thermal cycling. Hard solder is used for the joint between cathode-plate and cathode terminal for the same reason. Figure 1.12 shows a section through a typical thermal-fatigue-resistant high current SCR.

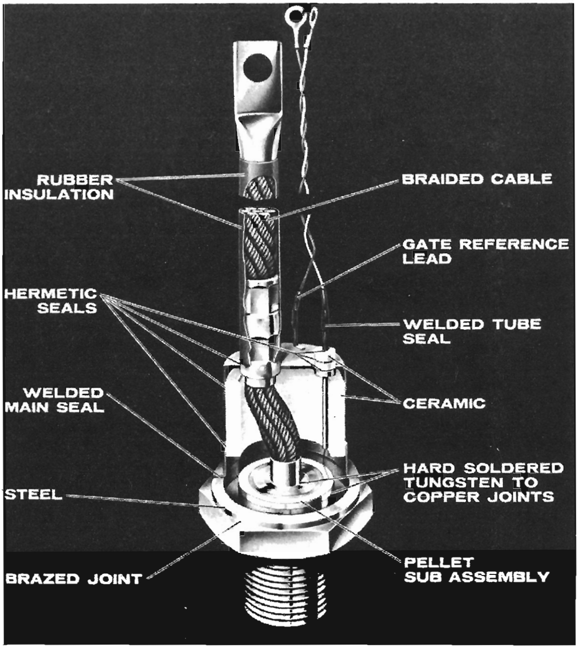


FIGURE 1.12 THERMAL FATIGUE RESISTANT SCR CONSTRUCTION

The second method of encapsulation involves replacement by pressure contacts[7] of the top solder joints between the copper, the tungsten (or molybdenum) back-up plate and the semiconductor pellet and the bottom copper-to-tungsten joint, shown in Figure 1.12. The elimination of the top hard solder joint between the silicon and the back-up plate relieves much of the thermally induced stress upon the pellet. This in turn makes the device much more thermal fatigue resistant and it is the only practical method to encapsulate pellets more than one inch in diameter.

The force required to develop the necessary pressure to ensure adequate electrical and thermal contacts at the joints may be either retained internally to the encapsulating housing or retained external to the encapsulation. A particular advantage to retaining the force externally is that this method allows cooling the semiconductor pellet assembly from both sides for improved heat transfer.

Figure 1.13 shows such a Press Pak encapsulation for a semiconductor pellet assembly suitable for double-sided air or water cooling.

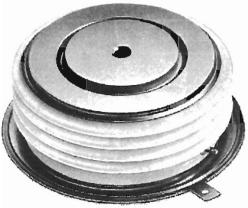


FIGURE 1.13(a) PRESS PAK ENCAPSULATION FOR A 550 AMPERE SEMICONDUCTOR PELLET ASSEMBLY

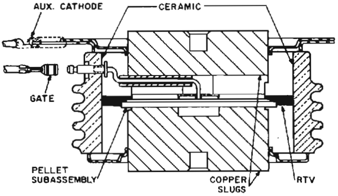


FIGURE 1.13(b) INTERNAL CONSTRUCTION DETAILS

When a thyristor is designed specifically for use in the light industrial and consumer markets, environments usually characterized by limited temperature excursions and an absence of wide range cyclical loading, the premium-type structures described above are not required. Here, the silicon pellet is mounted *directly* onto the copper stud, or case, with a special tin-lead solder alloy. The solder joint then absorbs the stresses set up by differential expansion between silicon and copper. *Providing these stresses are not too great,* this "soft solder" construction is satisfactorily thermal fatigue free. In addition to making possible a lower-cost device, the method allows better heat transfer from silicon to copper, which reduces cell heatsinking requirements.

The entire thyristor assembly is fabricated in a super-clean environment to assure long term stability of the SCR's electrical characteristics. To maintain the stability of these characteristics throughout the long life of the thyristor, the finished assembly is sealed off from the outside atmosphere by welded hermetic seals. Electrical connections are also made by welding. Extensive electrical and mechanical tests at room

temperature and both extremes of the operating temperature range assure that the individual thyristors meet their specification sheet ratings and characteristics. Cycled life tests on significant samples continuously monitor and control the long-term reliability of all devices coming off the production line.

Because planar or glassivated type pellet fabrication inherently give a large degree of environmental protection to the pellet electrical characteristics, hermetic glass-metal packaging is often not required for these type of devices. Pellets so passivated generally are encapsulated in a transfer-molded, silicone plastic package, which provides good mechanical integrity to the finished device. Figure 1.14(a) is a cutaway view of a four ampere planar SCR while Figure 1.14(b) shows a higher power plastic package used for glassivated triacs and SCR's.

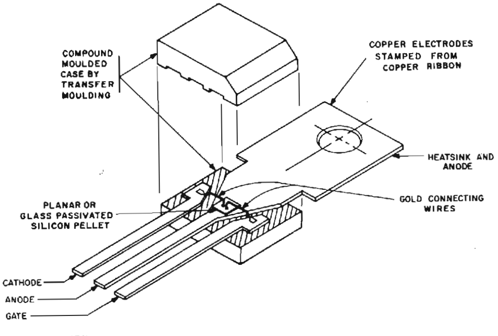


FIGURE 1.14(a) C106 PLANAR SCR IN THE POWER TAB PACKAGE

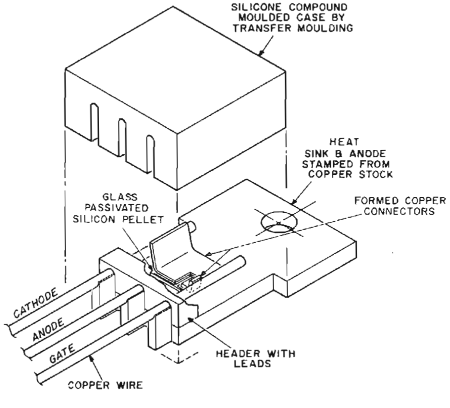


FIGURE 1.14(b) PICTORIAL VIEW OF THE POWER PAC ASSEMBLY

Another long sought for means of pellet passivation has recently become feasible — glass passivation. A thin coating of low temperature glass is fused onto the silicon chip and performs the same function as the SiO_2 layer mentioned above. Glass passivation is superior to SiO_2 (in actuality also a glass) since it can be applied in thicker coatings, thus giving superior passivation and allowing higher voltage ratings. Since glassivation is a *post-diffusion* passivation process, it can be readily applied to mesa-type pellet structures. In general, much higher blocking voltages can be obtained from mesa structures than from the planar process and additionally, silicon utilization (amps/sq cm) is much greater. Thus, mesa structures are more desirable for high voltage high current devices like large thyristors.

1.10 COMPARISON OF THYRISTORS WITH OTHER POWER SEMICONDUCTORS

It will be noted that the low current α of the p-n-p and n-p-n parts of a thyristor must be low in order to have the device block in the forward direction. In an ordinary three layer silicon power transistor, it is desirable to have α as high as possible in order to achieve a high current gain. Unfortunately, however, high α is obtained in most silicon transistors by using very thin base regions, and a thin base between two low resistivity regions is incompatible with high voltage. The wide base regions in the thyristor necessary to achieve low α are compatible with high voltages so that the thyristor is inherently a higher voltage device. The use of wide base regions is also an advantage from the standpoint of ease of manufacture and reproducibility of characteristics. An advantage of the thyristor over power transistors is the amount of drive necessary to full conduction. In many silicon power transistors, it is necessary to inject up to half an ampere of continuous base current in order to conduct 5 amperes from collector to emitter. In a thyristor, the amount of current conducted is dependent only on the external circuit once the device has been triggered. Thus a trigger current of 50 ma applied for only a few microseconds is all that is necessary to allow conduction of any current from a few milliamperes to hundreds of amperes. The high current capabilities of the thyristor, as contrasted to a transistor, are due to more effective use of junction area for current conduction.

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NOTES

2 SYMBOLS AND TERMINOLOGY

2.1 SEMICONDUCTOR GRAPHICAL SYMBOLS

Fig. 2.1 shows graphical symbols of the types of semiconductors discussed and employed in the circuits of this Manual. These symbols are mostly popular usage ones, and conform to existing and most probable future standards as much as possible. The symbols are circuit-oriented. The V-I characteristic of a device in four-quadrant representation relates the graphical symbol to its basic terminal electrical characteristic of interest to the circuit engineer rather than to its semiconductor device geometry.

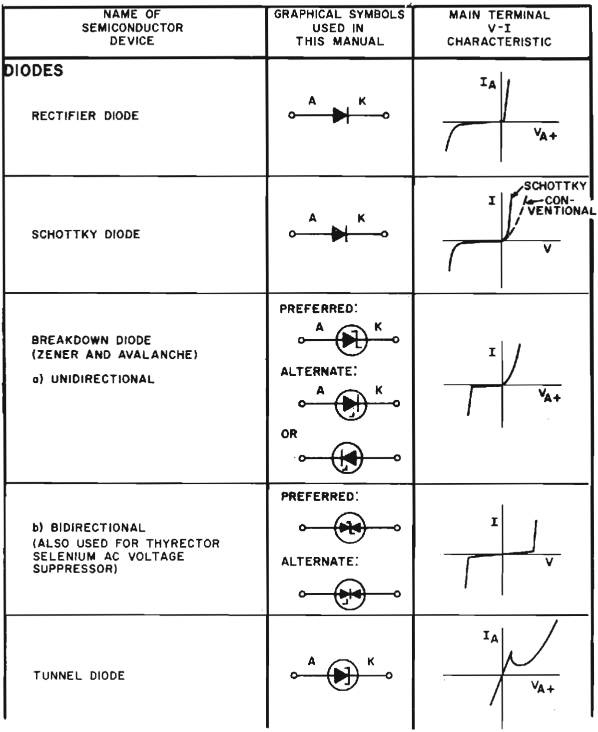


FIGURE 2.1 SEMICONDUCTOR GRAPHICAL SYMBOLS

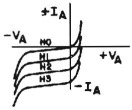
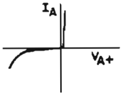
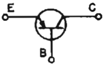
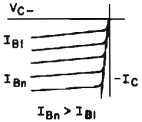
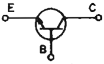
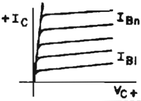
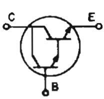
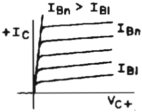
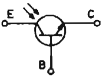
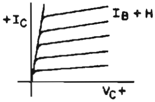
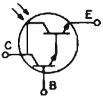
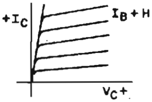
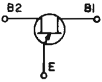
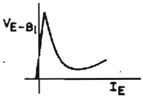
NAME OF SEMICONDUCTOR DEVICE	GRAPHICAL SYMBOLS USED IN THIS MANUAL	MAIN TERMINAL V-I CHARACTERISTIC
Diodes (cont.) PHOTO DIODE		
LIGHT EMITTING DIODE, OR SOLID STATE LAMP		
TRANSISTORS PNP		
NPN		
DARLINGTON AMPLIFIER		
LIGHT SENSITIVE TRANSISTOR (PHOTO TRANSISTOR)		
LIGHT SENSITIVE DARLINGTON PHOTO AMPLIFIER		
UJT (UNIJUNCTION TRANSISTOR) (N-TYPE BASE)		

FIGURE 2.1 SEMICONDUCTOR GRAPHICAL SYMBOLS

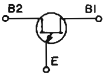
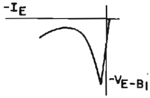
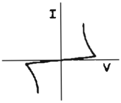
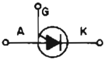
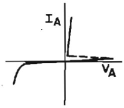
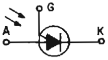
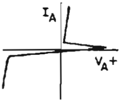
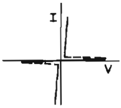
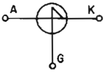
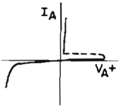
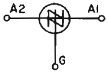
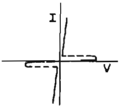
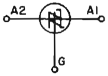
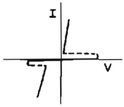
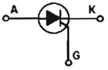
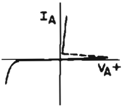
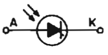
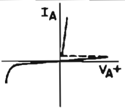
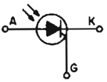
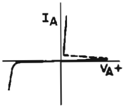
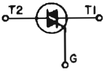
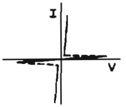
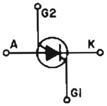
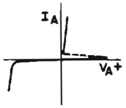
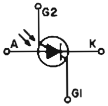
NAME OF SEMICONDUCTOR DEVICE	GRAPHICAL SYMBOLS USED IN THIS MANUAL	MAIN TERMINAL V-I CHARACTERISTIC
Transistors (cont.) CUJT (COMPLEMENTARY UNIJUNCTION TRANSISTOR) (P-TYPE BASE)		
BIDIRECTIONAL TRIGGER DIAC (NPN TYPE)		
THYRISTORS PUT (PROGRAMMABLE UNIJUNCTION TRANSISTOR)		
LAPUT (LIGHT ACTIVATED PROGRAMMABLE UNIJUNCTION TRANSISTOR)		
DIAC (BIDIRECTIONAL DIODE THYRISTOR)		
SUS (SILICON UNILATERAL SWITCH)		
SBS (SILICON BILATERAL SWITCH)		
ASBS (ASSYMMETRICAL SILICON BILATERAL SWITCH)		

FIGURE 2.1 SEMICONDUCTOR GRAPHICAL SYMBOLS

NAME OF SEMICONDUCTOR DEVICE	GRAPHICAL SYMBOLS USED IN THIS MANUAL	MAIN TERMINAL V-I CHARACTERISTIC
Thyristors (cont.) SCR (SILICON CONTROLLED RECTIFIER) REVERSE BLOCKING TRIODE THYRISTOR		
LAS (LIGHT ACTIVATED SWITCH) LIGHT ACTIVATED REVERSE BLOCKING DIODE THYRISTOR		
LASCR (LIGHT ACTIVATED SILICON CONTROLLED RECTIFIER) LIGHT ACTIVATED REVERSE BLOCKING TRIODE THYRISTOR		
TRIAC (BIDIRECTIONAL TRIODE THYRISTOR)		
SCS (SILICON CONTROLLED SWITCH) REVERSE BLOCKING TETRODE THYRISTOR		
LASCS (LIGHT ACTIVATED SILICON CONTROLLED SWITCH) LIGHT ACTIVATED REVERSE BLOCKING TETRODE THYRISTOR		

A – ANODE E – EMITTER
B – BASE G – GATE
C – COLLECTOR K – CATHODE

NOTE:

CIRCLES AROUND GRAPHICAL SYMBOLS ARE OPTIONAL EXCEPT WHERE OMISSION WOULD RESULT IN CONFUSION. IN THESE CASES CIRCLE DENOTES AN ENVELOPE THAT EITHER ENCLOSES A NON-ACCESSIBLE TERMINAL OR TIES A DESIGNATOR INTO SYMBOL.

FIGURE 2.1 SEMICONDUCTOR GRAPHICAL SYMBOLS

2.2 SCR TERMINOLOGY

The following tabulation defines the terminology used in SCR and triac specifications. As in the case of graphical symbols (Section 2.1) we try to conform to existing standards wherever possible.

2.2.1 Subscripts

The following letters are used as qualifying subscripts for thyristor letter symbols.

A	Anode, Ambient
(AV)	Average Value
(BO)	Breakover
(BR)	Breakdown
C	Case
D	Off-State, Non-Trigger
d	Delay
G	Gate
H	Holding
K	Cathode
L	Latching
M	Maximum Value
O	Open Circuit
q	Turn-off
R	Reverse or, as a second subscript, Repetitive
(RMS)	Total Root Mean Square Value
r	Rise
rr	Reverse Recovery
S	Short Circuit, or as a Second Subscript, Non-Repetitive (Infrequent)
T	On-State, Trigger
Θ	Thermal
W	Working

2.2.2 Characteristics and Ratings

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

A rating is a value which establishes either a limiting capability or a limiting condition (either maxima or minima) for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Principal Voltage-Current Characteristic (Principal Characteristic)	The function, usually represented graphically, relating the principal voltage to the principal current with gate current, where applicable, as a parameter.

Anode-to-Cathode Voltage-Current Characteristic (Anode Characteristic)	A function, usually represented graphically, relating the anode-to-cathode voltage to the principal current with gate current, where applicable, as a parameter. NOTE: This term does not apply to bidirectional thyristors.
On-State	The condition of the thyristor corresponding to the low-resistance, low-voltage portion of the principal voltage-current characteristic in the switching quadrant(s).
Off-State	The condition of the thyristor corresponding to the high-resistance, low-current portion of the principal voltage-current characteristic between the origin and the breakover point(s) in the switching quadrant(s).
Breakover Point	Any point on the principal voltage-current characteristic for which the differential resistance is zero and where the principal voltage reaches a maximum value.
Negative Differential Resistance Region	Any portion of the principal voltage-current characteristic in the switching quadrant(s) within which the differential resistance is negative.
Reverse Blocking State (of a Reverse Blocking Thyristor)	The condition of a reverse blocking thyristor corresponding to the portion of the anode-to-cathode voltage-current characteristic for reverse currents of lower magnitude than the reverse breakdown current.
Off-Impedance	The differential impedance between the terminals through which the principal current flows, when the thyristor is in the off-state at a stated operating point.
On-Impedance	The differential impedance between the terminals through which the principal current flows, when the thyristor is in the on-state at a stated operating point.
Reverse Blocking Impedance (of a Reverse Blocking Thyristor)	The differential impedance between the two terminals through which the principal current flows, when the thyristor is in the reverse blocking state at a stated operating point.

Principal Voltage	The voltage between the main terminals. NOTE: 1. In the case of reverse blocking thyristors, the principal voltage is called positive when the anode potential is higher than the cathode potential, and called negative when the anode potential is lower than the cathode potential. 2. For bi-directional thyristors, the principal voltage is called positive when the potential of main terminal 2 is higher than the potential of main terminal 1.
Anode-to-Cathode Voltage (Anode Voltage)	The voltage between the anode terminal and the cathode terminal. NOTE: 1. It is called positive when the anode potential is higher than the cathode potential, and called negative when the anode potential is lower than the cathode potential. 2. This term does not apply to bi-directional thyristors.
Forward Voltage (of a Reverse Blocking Thyristor)	A positive anode-to-cathode voltage.
Off-State Voltage	The principal voltage when the thyristor is in the off-state.
Working Peak Off-State Voltage	The maximum instantaneous value of the off-state voltage which occurs across a thyristor, excluding all repetitive and non-repetitive transient voltages.
Repetitive Peak Off-State Voltage	The maximum instantaneous value of the off-state voltage which occurs across a thyristor, including all repetitive transient voltages, but excluding all non-repetitive transient voltages.
Non-Repetitive Peak Off-State Voltage	The maximum instantaneous value of any non-repetitive transient off-state voltage which occurs across the thyristor.
Critical Rate of Rise of Off-State Voltage	The minimum value of the rate of rise of principal voltage which may cause switching from the off-state to the on-state.
Reapplied Rate of Rise of Voltage, Reapplied dv/dt (of Reverse Blocking Thyristor)	Rate of rise of forward voltage following turn-off, or commutation. (This is a test condition for turn-off time measurement.)

Critical Rate of Rise of Commutation Voltage (for Bidirectional Thyristors)	The minimum value of the rate of rise of principal voltage which may cause switching from the off-state to the on-state immediately following on-state current conduction in the opposite quadrant.
Breakover Voltage	The principal voltage at the breakover point.
On-State Voltage	The principal voltage when the thyristor is in the on-state.
Minimum On-State Voltage	The minimum positive principal voltage for which the differential resistance is zero with the gate open-circuited.
Principal Current	A generic term for the current through the collector junction. NOTE: It is the current through both main terminals.
On-State Current	The principal current when the thyristor is in the on-state.
Forward Current (of a Reverse Blocking Thyristor)	The principal current for a positive anode-to-cathode voltage.
Peak Repetitive On-State Current	The peak value of the on-state current including all repetitive transient currents.
Surge (Non-Repetitive) On-State Current	An on-state current of short-time duration and specified waveshape.
Critical Rate of Rise of On-State Current	The maximum value of the rate of rise of on-state current which a thyristor can withstand without deleterious effect.
Off-State Current	The principal current when the thyristor is in the off-state.
Breakover Current	The principal current at the breakover point.
Holding Current	The minimum principal current required to maintain the thyristor in the on-state.
Latching Current	The minimum principal current required to maintain the thyristor in the on-state immediately after switching from the off-state to the on-state has occurred and the triggering signal has been removed.
Reverse Voltage (of a Reverse Blocking Thyristor)	A negative anode-to-cathode voltage.
Working Peak Reverse Voltage (of a Reverse Blocking Thyristor)	The maximum instantaneous value of the reverse voltage which occurs across the thyristor, excluding all repetitive and non-repetitive transient voltages.
Repetitive Peak Reverse Voltage (of a Reverse Blocking Thyristor)	The maximum instantaneous value of the reverse voltage which occurs across the thyristor, including all repetitive transient voltages, but excluding all non-repetitive transient voltages.

Non-Repetitive Peak Reverse Voltage (of a Reverse Blocking Thyristor)	The maximum instantaneous value of any non-repetitive transient reverse voltage which occurs across a thyristor.
Reverse Breakdown Voltage (of a Reverse Blocking Thyristor)	The value of negative anode-to-cathode voltage at which the differential resistance between the anode and cathode terminals changes from a high value to a substantially lower value.
Reverse Current (of a Reverse Blocking Thyristor)	The current for negative anode-to-cathode voltage.
Reverse Breakdown Current (of a Reverse Blocking Thyristor)	The principal current at the reverse breakdown voltage.
Gate Voltage	The voltage between a gate terminal and a specified main terminal. NOTE: Gate voltage polarity is referenced to the specified main terminal.
Gate Current	The current that results from the gate voltage. NOTE: 1. Positive gate current refers to conventional current entering the gate terminal. 2. Negative gate current refers to conventional current leaving the gate terminal.
Gate Trigger Voltage	The gate voltage required to produce the gate trigger current.
Gate Non-Trigger Voltage	The maximum gate voltage which will not cause the thyristor to switch from the off-state to the on-state.
Gate Trigger Current	The minimum gate current required to switch a thyristor from the off-state to the on-state.
Gate Non-Trigger Current	The maximum gate current which will not cause the thyristor to switch from the off-state to the on-state.
Thermal Resistance (of a Semiconductor Device)	The temperature difference between two specified points or regions divided by the power dissipation under conditions of thermal equilibrium.
Transient Thermal Impedance (of a Semiconductor Device)	The change of temperature difference between two specified points or regions at the end of a time interval divided by the step function change in power dissipation at the beginning of the same time interval causing the change of temperature difference.

Gate Controlled Turn-On Time	The time interval between a specified point at the beginning of the gate pulse and the instant when the principal voltage (current) has dropped (risen) to a specified low (high) value during switching of a thyristor from off-state to the on-state by a gate pulse.
Gate Controlled Delay Time	The time interval between a specified point at the beginning of the gate pulse and the instant when the principal voltage (current) has dropped (risen) to a specified value near its initial value during switching of a thyristor from the off-state to the on-state by a gate pulse.
Gate Controlled Rise Time	The time interval between the instants at which the principal voltage (current) has dropped (risen) from a specified value near its initial value to a specified low (high) value during switching of a thyristor from the off-state to the on-state by a gate pulse. NOTE: This time interval will be equal to the rise time of the on-state current only for pure resistive loads.
Circuit-Commutated Turn-Off Time	The time interval between the instant when the principal current has decreased to zero after external switching of the principal voltage circuit, and the instant when the thyristor is capable of supporting a specified principal voltage without turning on.
Reverse Recovery Time (of a Reverse Blocking Thyristor)	The time required for the principal current or voltage to recover to a specified value after instantaneous switching from an on-state to a reverse voltage or current.
I squared t (I^2t)	This is a measure of maximum forward non-recurring overcurrent capability for very short pulse durations. The value is valid only for the pulse duration specified. I is in RMS amperes, and t is pulse duration in seconds. (I^2t is necessary for fuse co-ordination.)
Mounting Force	Range of mounting forces recommended for Press Pak packages to insure an adequate thermal and electrical path while avoiding mechanical damage.
Stud Torque	Recommended mounting torque for stud packages.

2.2.3 Letter Symbol Table

Quantity	Total RMS Value	DC Value, No Alternating Component	DC Value, With Alternating Component	Instantaneous Total Value	Maximum (Peak) Total Value
On-State Current	$I_{T(RMS)}$	I_T	$I_{T(AV)}$	i_T	I_{TM}
Repetitive Peak On-State Current					I_{TRM}
Surge (Non-Repetitive) On-State Current					I_{TSM}
Breakover Current		$I_{(BO)}$		$i_{(BO)}$	
Off-State Current	$I_{D(RMS)}$	I_D	$I_{D(AV)}$	i_D	I_{DM}
Repetitive Peak Off-State Current					I_{DRM}
Reverse Current	$I_{R(RMS)}$	I_R	$I_{R(AV)}$	i_R	I_{RM}
Repetitive Peak Reverse Current					I_{RRM}
Reverse Breakdown Current		$I_{(BR)R}$		$i_{(BR)R}$	
On-State Voltage	$V_{T(RMS)}$	V_T	$V_{T(AV)}$	v_T	V_{TM}
Breakover Voltage		$V_{(BO)}$		$v_{(BO)}$	
Off-State Voltage	$V_{D(RMS)}$	V_D	$V_{D(AV)}$	v_D	V_{DM}
Minimum On-State Voltage		$V_{T(MIN)}$			
Working Peak Off-State Voltage					V_{DWM}
Repetitive Peak Off-State Voltage					V_{DRM}
Non-Repetitive Peak Off-State Voltage					V_{DSM}
Reverse Voltage	$V_{R(RMS)}$	V_R	$V_{R(AV)}$	v_R	V_{RM}
Working Peak Reverse Voltage					V_{RWM}
Repetitive Peak Reverse Voltage					V_{RRM}

Quantity	Total RMS Value	DC Value, No Alternating Component	DC Value, With Alternating Component	Instantaneous Total Value	Maximum (Peak) Total Value
Non-Repetitive Peak Reverse Voltage					V_{RSM}
Reverse Breakdown Voltage		$V_{(BR)R}$		$v_{(BR)R}$	
Holding Current		I_H		i_H	
Latching Current		I_L		i_L	
Gate Current		I_G	$I_{G(AV)}$	i_G	I_{GM}
Gate Trigger Current		I_{GT}		i_{GT}	I_{GTM}
Gate Non-Trigger Current		I_{GD}		i_{GD}	I_{GDM}
Gate Voltage		V_G	$V_{G(AV)}$	v_G	V_{GM}
Gate Trigger Voltage		V_{GT}		v_{GT}	V_{GTM}
Gate Non-Trigger Voltage		V_{GD}		v_{GD}	V_{GDM}
Gate Power Dissipation		P_G	$P_{G(AV)}$	p_G	P_{GM}

2.2.4 General Letter Symbols

	Present Symbol	Former Symbol
Ambient Temperature	T_A	
Case Temperature	T_C	
Junction Temperature	T_J	
Storage Temperature	T_{stg}	
Thermal Resistance	R_θ	θ
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	$\theta_{J\text{-}C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	$\theta_{J\text{-}A}$
Thermal Resistance, Case-to-Ambient	$R_{\theta CA}$	$\theta_{C\text{-}A}$
Transient Thermal Impedance	$Z_{\theta(t)}$	$\theta_{(t)}$
Transient Thermal Impedance, Junction-to-Case	$Z_{\theta JC(t)}$	$\theta_{J\text{-}C(t)}$
Transient Thermal Impedance, Junction-to-Ambient	$Z_{\theta JA(t)}$	$\theta_{J\text{-}A(t)}$
Delay Time	t_d	
Rise Time	t_r	
Fall Time	t_f	
Reverse Recovery Time	t_{rr}	
Circuit-Commutated Turn-Off Time	t_q	

3 RATINGS AND CHARACTERISTICS OF THYRISTORS

The family of thyristor devices has in common a switching capability in one or two quadrants of its V-I characteristics. Thyristor devices used as power switches have in common the necessity for proper design and specification of their heat dissipation and heat transfer properties. Furthermore, thyristors are switched into the on-state either by applying a triggering signal to their gate or by increasing off-state voltage until it exceeds the breakover voltage characteristic. These and other common properties of thyristor devices allow a uniform approach to thyristor characterization which need differ only in detail when applied to a specific thyristor device like, for example, an SCR or a triac.

In the following sections of this chapter the discussion is largely in terms of SCR's. Most of this material is applicable, however, to other thyristor devices. Specialized characterization information is presented in Chapter 7 for triacs and in Chapter 14 for light-activated thyristors.

3.1 JUNCTION TEMPERATURE

The operating junction temperature range of thyristors varies for the individual types. A low temperature limit may be required to limit thermal stress in the silicon crystal to safe values. This type of stress is due to the difference in the thermal coefficients of expansion of the materials used in fabricating the cell subassembly. The upper operating temperature limit is imposed because of the temperature dependence of the breakover voltage, turn-off time and thermal stability considerations. The upper storage temperature limit in some cases may be higher than the operating limit. It is selected to achieve optimum reliability and stability of characteristics with time.

The rated maximum operating junction temperature can be used to determine steady-state and recurrent overload capability for a given heatsink system and maximum ambient temperature. Conversely, the required heatsink system may be determined for a given loading of the semiconductor device by means of the classic thermal impedance approach presented in Sections 3.3 and 3.4.

Transiently the device may actually operate beyond its specified maximum operating junction temperature and still be applied within its ratings. An example of this type of operation occurs within the specified forward non-recurrent surge current rating. Another example is the local temperature rise of the junction due to the switching dissipation during the turn-on of a thyristor under some conditions. It is impractical at this time to establish temperature limits for these types

of operating stresses from both a rating as well as an applications point of view. Therefore, such higher-than-rated temperature operation must remain implicit in other ratings established for the device.

3.2 POWER DISSIPATION

The power generated in the junction region in typical thyristor operation consists of the following five components of dissipation:

a. Turn-on switching
b. Conduction
c. Turn-off or Commutation
d. Blocking
e. Triggering

On-state conduction losses are the major source of junction heating for normal duty cycles and power frequencies. However, for very steep (high di/dt) current waveforms or high operating frequencies turn-on switching losses may become the limiting consideration. Such cases are discussed in Sections 3.7 and 3.8.

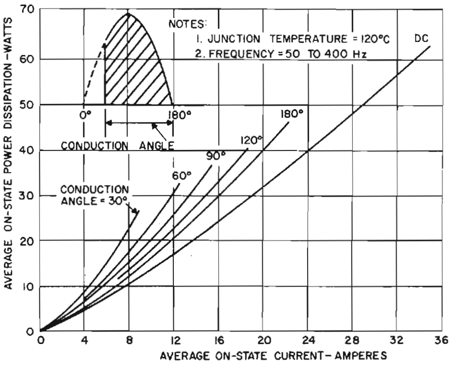


FIGURE 3.1 MAXIMUM AVERAGE ON-STATE POWER DISSIPATION FOR C137 SERIES SCR

Figure 3.1 gives on-state conduction loss in average watts for the C137 SCR as a function of average current in amperes for various conduction angles for operation up to 400 Hz. This type of information is given on the specification sheet for each type of SCR (with the exception of some inverter type SCR's). These curves are based on a current waveform which is the remainder of a half-sine wave which results when delayed angle triggering is used in a single phase resistive load circuit. Similar curves exist for rectangular current waveforms. These power curves are the integrated product of the instantaneous anode current and on-state voltage drop. This integration can be performed graphically or analytically for conduction angles other than those listed,

using the on-state voltage-current characteristic curves for the specific device.

Both the on-state and reverse blocking losses are determined by integration of the appropriate blocking E-I curves on the specification sheet.

Gate losses are negligible for pulse types of triggering signals. Losses may become more significant for gate signals with a high duty cycle, or for SCR's in a small package such as the TO-5, TO-18 or Power Tab type packages. The losses may be calculated from the gate E-I curves shown on the triggering characteristics for the specific type of SCR. Highest gate dissipation will occur for an SCR whose gate characteristics intersect the gate circuit load line at its midpoint. For a more detailed discussion of the gate characteristic and its load line, see Chapter 4.

Turn-on switching ratings are discussed in Section 3.8. Turn-off is discussed in Chapter 5.

3.3 THERMAL RESISTANCE

The heat developed at the junctions by the foregoing power losses flows into the case, then to the heatsink (if employed) and on to the surrounding ambient fluid. The junction temperature rises above the stud, or case, temperature in direct proportion to the amount of heat flowing from the junction and the thermal resistance of the device to the flow of heat. The following equation defines the relationship under steady-state conditions:

$$T_J - T_C = PR_{\theta JC} \tag{3.1}$$

where T_J = average junction temperature, °C
T_C = case temperature, °C
P = average heat generation at junction, watts
$R_{\theta JC}$ = steady-state thermal resistance between junctions and bottom face of hex or case, °C/watt

Equation 3.1 can be used to determine the allowable power dissipation and thus the continuous pure DC on-state current rating of an SCR for a given case temperature through use of the on-state E-I curves. For this purpose, T_J is the maximum allowable junction temperature for the specific device. The maximum values of $R_{\theta JC}$ and T_J are given in the specifications.

3.4 TRANSIENT THERMAL IMPEDANCE

3.4.1 Introduction

Equation 3.1 is not satisfactory for finding the peak junction temperature when the heat is applied in pulses such as the recurrent conduction periods in an AC circuit. Solution of Equation 3.1 using the peak value of P is over-conservative in limiting the junction temperature rise. On the other hand, using the average value of P over a full cycle will underestimate the peak temperature of the junction. The reason for this discrepancy lies in the thermal capacity of the semiconductor,

that is, its characteristic of requiring time to heat up, its ability to store heat, and its cooling before the next pulse.

Compared to other electrical components such as transformers and motors, semiconductors have a relatively low thermal capacity, particularly in the immediate vicinity of the junction. As a result, devices like the SCR heat up very quickly upon application of load, and the temperature of the junction may fluctuate during the course of a cycle of power frequency. Yet, for very short overloads this relatively low thermal capacity may be significant in arresting the rapid rise of junction temperature. In addition, the heatsink to which the semiconductor is attached may have a thermal constant of many minutes. Both of these effects can be used to good advantage in securing attractive intermittent and pulse ratings sometimes well in excess of the published continuous DC ratings for a device.

3.4.2 The Transient Thermal Impedance Curve

The thermal circuit of the SCR can be simplified to that shown in Figure 3.2. This is an equivalent network emanating in one direction from the junctions and with the total heat losses being introduced at the junctions only. This simplification is valid for current amplitudes at which I^2R losses are small in comparison with the junction losses. In Figure 3.2 the case of the power semiconductor is the reference level. If a small stud type device is mounted to an infinite heatsink, the heatsink temperature can be used as a reference. However, with larger devices, the case to heatsink thermal resistance is relatively large compared to the junction-case thermal resistance. In such cases the case or hex temperature should be used as a reference.

When a step pulse of heating power P is introduced at the junctions of the SCR (and of the thermal circuit) as shown in Figure 3.3A, the junction temperature will rise at a rate dependent upon the response of the thermal network. This is represented by the curve T_{heat} in Figure 3.3B. After some sufficiently long time t_1, the junction temperature will stabilize at a point $\Delta T = PR_{\theta JC}$ above the ambient (or case) temperature. This is the steady-state value which is given by Equation 3.1. $R_{\theta JC}$ is the sum of R_{θ_1} through R_{θ_N} in the equivalent thermal circuit of Figure 3.2. Chapter 20 gives specific instructions complete with circuit schematics for measuring SCR characteristics.

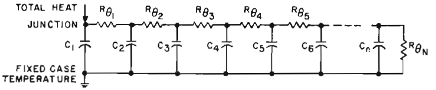


FIGURE 3.2 SIMPLIFIED EQUIVALENT THERMAL CIRCUIT FOR A POWER SEMICONDUCTOR

If the power input is terminated at time t_2 after the junction temperature has stabilized, the junction temperature will return to ambient along the locus indicated by T_{cool} in Figure 3.3B. It can be shown that curves T_{heat} and T_{cool} are conjugates of one another,[1] that is,

$$T_{cool} = \Delta T - T_{heat} = PR_{\theta JC} - T_{heat} \tag{3.2}$$

By dividing the instantaneous temperature rise of curve T_{heat} in Figure 3.3B by the power P causing the rise, the dimensions of the ordinate can be converted from °C to °C/watt. This latter set of dimensions is that of thermal resistance, or as it is more precisely termed: the transient thermal impedance $Z_{\theta(t)}$. Figure 3.4 shows a plot of transient thermal impedance for the C34 SCR both when mounted to an infinite heatsink and to a four-inch square copper fin.

Transient thermal impedance information for a device can be obtained by monitoring junction temperature at the end of a well-defined power pulse or after a known steady-state load has been removed. Junction temperature is measured by use of one of the temperature-sensitive junction characteristics such as on-state voltage drop at low currents. Conversion of heating data to cooling data, or vice versa, can be accomplished through the use of Equation 3.2.

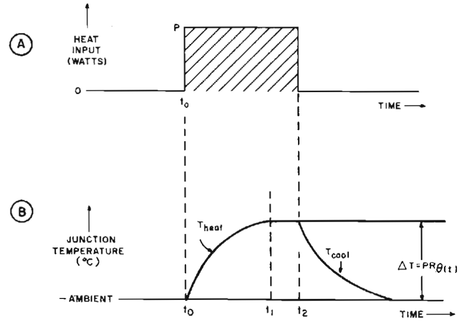


FIGURE 3.3 RESPONSE FOR SCR JUNCTION TO STEP PULSE OF HEATING POWER

In order that the transient thermal impedance curve may be used with confidence in equipment designs, the curve must represent the highest values of thermal impedance for each time interval that can be expected from the manufacturing distribution of the products.

The transient thermal impedance curve approaches asymptotic values at both the long time and short time extremes. For very long time intervals the transient thermal impedance approaches the steady-state thermal resistance $R_{\theta JC}$.

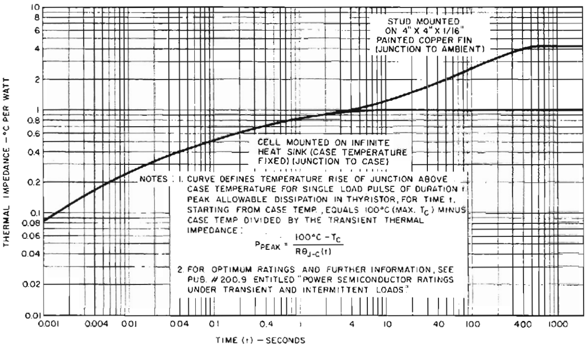


FIGURE 3.4 MAXIMUM TRANSIENT THERMAL IMPEDANCE OF C34 SCR

For times less than 1 millisecond the value at 1 millisecond may be extrapolated by $1/\sqrt{t}$. This is based on assuming that the time of interest is sufficiently small so that all heat generated at the semiconductor junction may be considered to flow by one-dimensional diffusion within the silicon pellet. This assumption is valid for times small compared to the thermal time constant of the path junction-to-face of the silicon pellet. For extremely short times, however, during which current density, and hence heating, is non-uniform, this approach is no longer valid.

For example the C34 transient thermal impedance at 40 μseconds may be estimated at

$$\frac{.083}{\sqrt{\dfrac{1 \times 10^{-3}}{4 \times 10^{-5}}}} = .0166°\text{C/Watt}$$

However, the extrapolated values are valid only for times after the SCR has turned on fully. These values should, in other words, not be used during the switching interval (see Section 3.8). In general the switching interval is between 20 and 200 μseconds for medium and high current SCR's respectively and a minimum of 10 μseconds for the very low current devices. The switching interval can be estimated by inspecting the energy per pulse data curves for the knee of the constant watt-seconds curves. For example, Figure 3.5 shows the knee to be at about 20 μseconds for the C141 SCR. Since the C34 has a similar current rating extrapolations down to 20 μseconds would seem to be in order. However due to differences in gate geometries 40 μseconds is a conservative lower limit. (See Chapter 1, Section 1.5 for further data on gate geometries.)

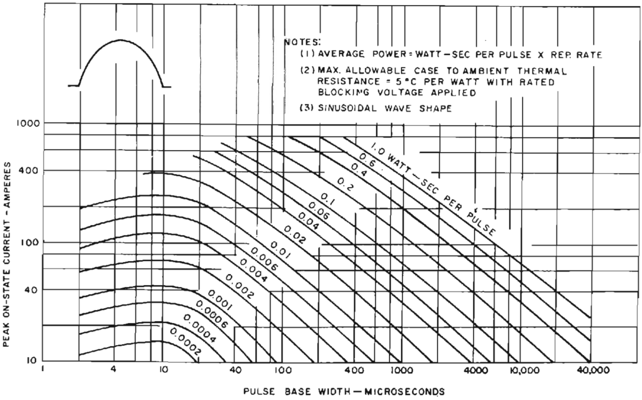


FIGURE 3.5 ENERGY PER PULSE FOR SINUSOIDAL PULSES FOR GE C141 SCR

For maximum utilization of semiconductor devices in the switching region additional factors must be considered and other methods of rating and life testing must be used. Consult Sections 3.7 and 3.8 for further information.

3.4.3 The Effect of Heatsink Design on the Transient Thermal Resistance Curve

Since the heatsink is a major component in the heat transfer path between junction and ambient, its design affects the transient thermal impedance curve (Figure 3.4) substantially. When a semiconductor is manufactured and shipped to the user the manufacturer has no control over the ultimate heatsink and can only provide data on the heat transfer system between junction and case which is the part he manufactured. These type of data are presented in Figure 3.4 as the "Cell Mounted to Infinite Heatsink" curve.

The equipment designer can use this curve in developing a transient thermal impedance curve for the cell when mounted to a particular heatsink of his own design by means of a few simple calculations. These calculations consist of first determining the heatsink time constant by deriving the relationship as shown in Chapter 18 (Mounting and Cooling The Power Semiconductor) and then adding the transient thermal relationship of the heatsink to that of the cell.

For example: From Chapter 18 we find that a 4″ x 4″ painted copper fin 1/16″ thick has a transient thermal resistance given by

$$Z_{\Theta(t)fin} = 3.1\ (1 - e^{-t/174})$$

Assume case to fin contact resistance is negligible for example simplification.

The values of $Z_{\theta(t)fin}$ are added to the infinite heatsink curve to secure the over-all $Z_{\theta(t)}$ of the system as indicated in Figure 3.4. Note that this fin makes a negligible contribution to the over-all thermal impedance of the cell-heatsink system at periods of time one second or less after application of power. In this area the fin behaves like an infinite heatsink, that is, one of zero thermal resistance. The fin-heatsink system reaches equilibrium around 1000 seconds. Thereafter the thermal capacity is no longer effective in holding down the junction temperature.

3.5 RECURRENT AND NON-RECURRENT CURRENT RATINGS

3.5.1 Introduction

The discussion under all parts of this section and Section 3.6 applies to the conventional rating system presently used for thyristors when turn-on switching dissipation is negligible. Turn-on switching characterization is discussed in Section 3.7; current ratings for high frequency operation which cannot neglect turn-on switching losses are discussed in Section 3.8.

When a semiconductor device is applied in such a manner that its maximum allowable peak junction temperature is not exceeded the device is applied on a *recurrent* basis. Any condition that is a normal and repeated part of the application or equipment in which the semiconductor device is used must meet this condition if the device is to be applied on a recurrent basis. Section 3.6 gives methods of checking peak junction temperature. These enable the designer to properly apply the device on a recurrent duty basis.

A class of ratings that makes the SCR and the triac truly power semiconductors are the *non-recurrent* current ratings. These ratings allow the maximum (recurrent) operating junction temperature of the device to be exceeded for a brief instant. This gives the device an instantaneous overcurrent capability allowing it to be coordinated with circuit protective devices such as circuit breakers, fuses,[2] etc. The specification bulletin gives these ratings in terms of surge current and I^2t. These ratings, then, should only be used to accommodate unusual circuit conditions not normally a part of the application, such as fault currents. Non-recurrent ratings are understood to apply to load conditions that will not occur more than a limited number of times in the course of the operating life of the equipment in which the SCR is finding application. (JEDEC* defines the number of times as equal to or exceeding 100 times.) Also, non-recurrent ratings are understood to apply only when they are not repeated before the peak junction temperature has returned to its maximum rated value or less. THE LENGTH OF THE INTERVAL BETWEEN SURGES DOES NOT CHANGE THE RATING. For example, if a garage door opener subjects a semiconductor device to its non-recurrent current rating, this is misapplying the device. As a result, the device may be subject to failure after 100 operations even though the device operates but once per 8 hour period.

*(JEDEC—Joint Electron Device Engineering Council—Semiconductor Standards Organization)

3.5.2 Average Current Rating (Recurrent)

Average current rating versus case temperature as it appears in the specification sheet as for the C380 series SCR is shown in Figure 3.6. These curves specify the maximum allowable average anode current ratings of the SCR as a function of case temperature and conduction angle. Points on these curves are selected so that the junction temperature under the stated conditions does not exceed the maximum allowable value. The maximum rated junction temperature of the C380 SCR is 125°C.

The curves of Figure 3.6 include the effects of the small contribution to total dissipation by reverse blocking, gate drive, and switching up to 400 Hz. For devices which are lead mounted or housed in small packages, like the TO-5 or Power Tab, the on-state current rating may be substantially affected by gate drive dissipation. Where this becomes important it is so indicated on the specification sheet.

The slope of the curves shown in Figure 3.6 is essentially dependent upon the $R_{\theta JC} \cdot P_D$ product. In some SCR's such as Press Paks and Power Tabs, $R_{\theta JC}$ is not fixed but is a function of the method used to cool it. Another family of curves would be needed in place of Figure 3.6 for single side cooling of the Press Pak package. Similarly, small packages such as the Power Tab may have more than one set of curves to take into account different mounting configurations and their corresponding effect on $R_{\theta JC}$.[3]

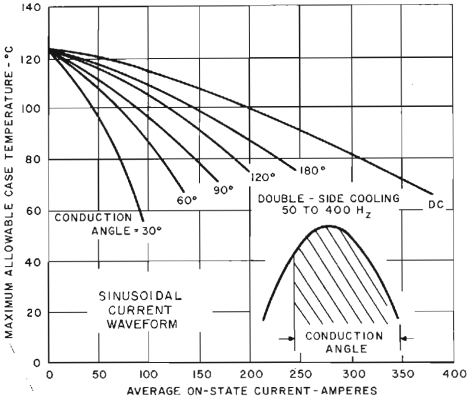


FIGURE 3.6 MAXIMUM AVERAGE CURRENT RATINGS FOR C380 SERIES SCR

If the C380 in a single phase resistive load circuit is triggered as soon as its anode swings positive, the device will conduct for 180 electrical degrees. If the case temperature is maintained at 80°C, or less, the C380 is capable of handling 235 amps average current as indicated in Figure 3.6. If the triggering angle is retarded by 120° the C380 will conduct for only the 60 remaining degrees of the half cycle. Under these conditions of 60° conduction, the maximum rated average current at 80°C stud temperature (double side cooled) is 115 amperes, substantially less than for 180° conduction angle. This leads us nicely into the next section.

3.5.3 RMS Current (Recurrent)

It will be noted in Figure 3.6 that the curves for the various conduction waveshapes have definite end points. These points represent identical RMS values, and as such an RMS rating is implicit in the curves of Figure 3.6.

For example, the C380 is rated 370 amperes DC or $\frac{370}{1.57} = 235$ amperes average in a half-wave, or 180° conduction angle, circuit. The factor 1.57 is the form factor giving the ratio of RMS to average values for a half wave sinusoidal waveform. By the definition of RMS values, the RMS and average values are identical for a direct current. The RMS current rating, as shown on the specification sheet for individual SCR's, is necessary to prevent excessive heating in resistive elements of the SCR, such as joints, leads, interfaces, etc.

The RMS current rating can be of importance when applying thyristors to high peak current, low duty cycle waveforms. Although the average value of the waveform may be well within the ratings, it may be that the allowable RMS rating is being exceeded.

The average current values shown as phase control ratings in Figure 3.6 for a given and fixed basic RMS device current rating are for the resistive current waveform shown in the figure. Since the current form factor for the case of resistive loading is greatest, and since inductance in the path of the thyristor current will reduce its form factor, the average current ratings in Figure 3.6 are conservative for inductive current waveforms.

For inductive waveforms in which the thyristor current waveform is essentially rectangular, such as may occur in a phase-controlled rectifier operating near full output, most specification sheets show separate rating curves to reflect the improvement in form factor. However, such current waveforms are, of course, subject to the restriction of the allowable turn-on current rating of the device.

In other cases in which the current waveform may be half-sinusoidal in shape but of a base width less than half a period of the supply frequency as, for example, with discontinuous AC line current in an AC switch application[4] at large phase retard, greater utilization of the thyristor in terms of its average current versus temperature ratings (like in Figure 3.6) can be obtained by taking into account the improvement of form factor due to decreasing load power factor (greater inductance) when applying the device within its RMS current rating. See also Section 9.2.1.

3.5.4 Arbitrary Current Waveshapes and Overloads (Recurrent)

Recurrent application of arbitrary waveshapes, varying duty cycles, and overloads requires that the maximum peak allowable junction temperature of the SCR not be exceeded. Section 3.6 gives information for determining this.

3.5.5 Surge and I^2t Ratings (Non-Recurrent)

In the event that a type of overload or short circuit can be classified as non-recurrent, the rated junction temperature can be exceeded for a brief instant, thereby allowing additional overcurrent rating. Ratings for this type of non-recurrent duty are given by the Surge Current and I^2t rating curves.

Figure 3.7 shows the maximum allowable non-recurrent multicycle surge current at rated load conditions. Note that the junction temperature is assumed to be at its maximum rated value (125°C for the C398); it is therefore apparent that the junction temperature will exceed its rated value for a short time during and immediately following operation within the non-recurrent ratings. Therefore many of the SCR's ratings and characteristics will not be valid until the junction temperature cools back down to within its rated value. The reader is thus reminded that off-state blocking capability, dv/dt and turn-off time, to name just a few device parameters, are not specified or guaranteed immediately following device operation in the non-recurrent current mode.

The data shown by the solid curve "A" are values of peak rectified sinusoidal waveforms on a 60 Hz basis in a half-wave circuit. The "one-cycle" point, therefore, gives an allowable non-recurrent half sine wave of 0.00834 seconds' duration (half period of 60 Hz frequency) of a peak amplitude of 7,300 amperes. The "20 cycle" point shows that 20 rectified half sine waves are permissible (separated by equal "off" times), *each* of an *equal* amplitude of 5,100 amperes.

The data shown by the dotted curve "B" for 50 Hz operation has been added to the curve and is not regularly part of the published data sheet. The curve is constructed by connecting two points on the curve with a straight line. The current value for the first point at 1 cycle is obtained from Figure 3.8 at 10 ms, the base width of a 50 Hz sine wave. The second point coincides with the 60 Hz, one second (60 cycles) value. Beyond the one second value the curves for 50 and 60 Hz waveforms are the same and are extensions of the 60 Hz curve.

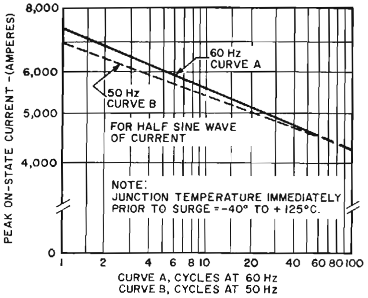
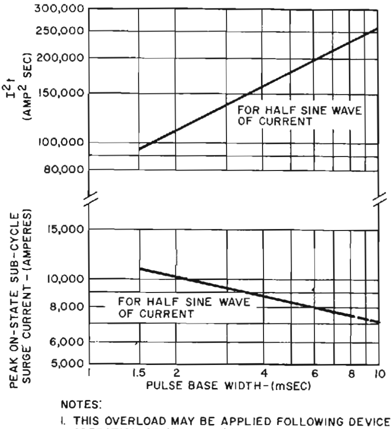


FIGURE 3.7 MAXIMUM ALLOWABLE MULTICYCLE, NON-RECURRENT, PEAK SURGE ON-STATE CURRENT FOR THE C398 SERIES SCR

The lower half of Figure 3.8 shows the maximum allowable non-recurrent sub-cycle surge current at rated load conditions. Like its sister multicycle curve of Figure 3.7, it is apparent that the junction temperature will again exceed its rated value for a short time.



NOTES:

1. THIS OVERLOAD MAY BE APPLIED FOLLOWING DEVICE OPERATION AT ANY VOLTAGE OR CURRENT WITHIN ITS STEADY STATE RATING LIMITS.
2. THIS OVERLOAD MAY NOT BE REPEATED UNTIL DEVICE JUNCTION TEMPERATURE HAS COOLED DOWN TO WITHIN STEADY STATE RATED VALUE.
3. NO BLOCKING VOLTAGE RATING IS IMPLIED DURING OR IMMEDIATELY FOLLOWING THE OVERLOAD CURRENT INTERVAL.
4. JUNCTION TEMPERATURE IMMEDIATELY PRIOR TO OVERLOAD = −40° TO +125°C.

FIGURE 3.8 SUB-CYCLE SURGE ON-STATE CURRENT AND I^2t RATING FOR THE C398 SERIES SCR

The I^2t rating is derived from the sub-cycle surge current curve of Figure 3.8 and is plotted directly above the current curve. The I in the I^2t value is the RMS value of current over an interval t corresponding to the pulse base width of Figure 3.8. For test and evaluation a half-sinusoidal pulse shape is generally employed.

Both the sub-cycle surge current and I^2t ratings assume that the SCR is already in the conducting state. If the SCR is turned on into a fault, the current-time relationships (di/dt) during the turn-on interval must be within the device's switching capabilities. Section 3.7 discusses turn-on switching dissipation in greater detail.

Provided the above precautions are observed, fault and overcurrent protection can be approached in the same manner as for power rectifier diodes. Protection methods are discussed in Chapter 15.

3.6 BASIC LOAD CURRENT RATING EQUATIONS

3.6.1 INTRODUCTION

In order for a device to be properly applied for recurrent load duty, its maximum allowable peak operation junction temperature must not be exceeded. By knowing the dissipation of a semiconductor device and its thermal response it is possible to meet this requirement by the method shown in Section 3.4.

The information given on the G-E specification sheet, in conjunction with the proper equation in Figure 3.9, allows the designer to calculate power semiconductor ratings for a variety of conditions.[1]

3.6.2 Treatment of Irregularly Shaped Power Pulses—Approximate Method

In the preceding section solutions for junction temperature were given in response to step functions of power input. In many practical applications, the power pulse is not of this ideal shape for computation, and appropriate approximations must be made to convert the actual waveshape into a rectangular form if the subsequent calculations are to be made as outlined.

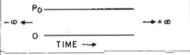
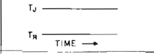
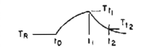
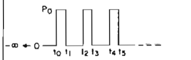
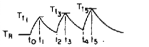
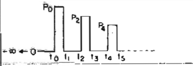
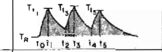
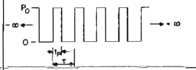
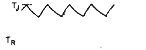
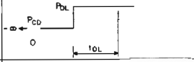
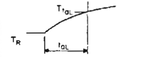
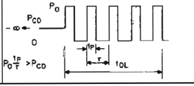
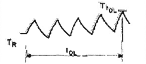
	LOAD CONDITION	WAVEFORM OF POWER LOSS AT JUNCTION	WAVEFORM OF JUNCTION TEMPERATURE RISE (T_R =REFERENCE TEMP.)	SOLUTION FOR JUNCTION TEMPERATURE AND POWER LOSS R_θ=STEADY-STATE THERMAL RESISTANCE $R_{\theta(t_1)}$=TRANSIENT THERMAL IMPEDANCE AT TIME t_1 $R_{\theta(t_2-t_1)}$=TRANSIENT THERMAL IMPED. AT TIME (t_2-t_1), ETC.
(a)	CONTINUOUS LOAD			$T_J - T_R = P_O R_\theta$ $P_O = \frac{T_J - T_R}{R_\theta}$
(b)	SINGLE LOAD PULSE			$T_{t_1} - T_R = P_O Z_{\theta(t_1)}$ $T_{t_2} - T_R = P_O \left[Z_{\theta(t_2)} - Z_{\theta(t_2-t_1)}\right]$ $P_O = \frac{T_{t_1} - T_R}{Z_{\theta(t_1)}}$
(c)	SHORT TRAIN OF LOAD PULSES (EQUAL AMPLITUDE)			$T_{t_1} - T_R = P_O Z_{\theta(t_1)}$ $T_{t_3} - T_R = P_O\left[Z_{\theta(t_3)} - Z_{\theta(t_3-t_1)} + Z_{\theta(t_3-t_2)}\right]$ $T_{t_5} - T_R = P_O\left[Z_{\theta(t_5)} - Z_{\theta(t_5-t_1)} + Z_{\theta(t_5-t_2)} - Z_{\theta(t_5-t_3)} + Z_{\theta(t_5-t_4)}\right]$ ETC.
(d)	TRAIN OF UNEQUAL AMPLITUDE LOAD PULSES			$T_{t_1} - T_R = P_O Z_{\theta(t_1)}$ $T_{t_3} - T_R = P_O Z_{\theta(t_3)} - P_O Z_{\theta(t_3-t_1)} + P_2 Z_{\theta(t_3-t_2)}$ $T_{t_5} - T_R = P_O Z_{\theta(t_5)} - P_O Z_{\theta(t_5-t_1)} + P_2 Z_{\theta(t_5-t_2)} - P_2 Z_{\theta(t_5-t_3)} + P_4 Z_{\theta(t_5-t_4)}$
(e)	LONG TRAIN OF EQUAL AMPLITUDE LOAD PULSES (APPROX SOLUTION)			$T_J - T_R = P_O\left[\frac{t_p R_\theta}{\tau} + \left(1 - \frac{t_p}{\tau}\right) Z_{\theta(\tau+t_p)} - Z_{\theta(\tau)} + Z_{\theta(t_p)}\right]$ $P_O = \frac{T_J - T_R}{\frac{t_p R_\theta}{\tau} + \left(1 - \frac{t_p}{\tau}\right) Z_{\theta(\tau+t_p)} - Z_{\theta(\tau)} + Z_{\theta(t_p)}}$
(f)	OVERLOAD FOLLOWING CONTINUOUS DUTY (NON-PULSED)			$T_{t_{OL}} - T_R = P_{CD} R_\theta + (P_{OL} - P_{CD}) Z_{\theta(t_{OL})}$ $P_{OL} = \frac{T_{t_{OL}} - T_R - P_{CD} R_\theta}{Z_{\theta(t_{OL})}} + P_{CD}$
(g)	OVERLOAD FOLLOWING CONTINUOUS DUTY (PULSED) (APPROX SOLUTION)	 $P_O \frac{t_p}{\tau} > P_{CD}$		$T_{t_{OL}} - T_R = P_{CD} R_\theta + P_O\left\{\left[\frac{t_p}{\tau} - \frac{P_{CD}}{P_O}\right] Z_{\theta(t_{OL})} + \left(1 - \frac{t_p}{\tau}\right) Z_{\theta(\tau+t_p)} - Z_{\theta(\tau)} + Z_{\theta(t_p)}\right\}$ $P_O = \frac{T_{t_{OL}} - T_R - P_{CD}(R_\theta - Z_{\theta(t_{OL})})}{\frac{t_p}{\tau} Z_{\theta(t_{OL})} + \left(1 - \frac{t_p}{\tau}\right) Z_{\theta(\tau+t_p)} - Z_{\theta(\tau)} + Z_{\theta(t_p)}}$

FIGURE 3.9 BASIC LOAD CURRENT RATING EQUATIONS

Figure 3.10A illustrates the arbitrary waveshape of a power pulse that re-occurs at a period of τ seconds and has a peak value of P_{pk} watts and a full-cycle average of P_{avg} watts. For the purpose of calculating peak junction temperatures, this waveshape can be approximated by the rectangular waveshape of Figure 3.10B. This rectangular waveshape is selected to have the identical values of peak power P_{pk} and average power P_{avg} as Figure 3.10A by altering the pulse duration by a constant N to maintain the peak to average relationship. β is defined as the ratio of P_{avg} to P_{pk}.

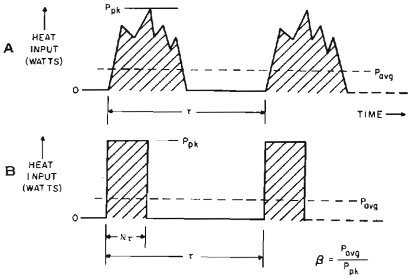


FIGURE 3.10 APPROXIMATING IRREGULARLY SHAPED HEATING PULSE WITH RECTANGULAR WAVESHAPES

This translation into rectangular pulses of power ensures a "worst case" approximation since a rectangular pulse of power will always have an effect on temperature rise which is equal to or greater than the effect of any other pulse having the same peak and average power. In other words, a rectangular power pulse will raise the junction temperature higher than any other waveshape with the same peak and average values since it concentrates its heating effects into a shorter period of time, thus minimizing cooling during the pulse.

Figure 3.11 illustrates a case where a similar type of approximation can be used to shorten the calculations for peak junction temperature when the problem would otherwise be too laborious for manual calculation. Computer programs are available for calculations of this general form. Detailed information on computed generated solutions are found in Reference 5. It involves the case where a sequence of current bursts is periodically interrupted by a longer "off" period of zero power. This is typical of any repetitive or cyclical on-off type of load, such as found in spot resistance welding duty. Each burst of pulses can be represented by a single square-wave with introduction of only a relatively small error. This error will always yield a junction temperature higher than actual, and will thus provide a conservative application. In the equivalent waveshape shown in Figure 3.11C, the peak value of power P_{pk} is maintained the same as in Figure 3.11B. The duration of the equivalent rectangular waveshape is reduced to βt_p where β is defined as P_{avg}/P_{pk}.

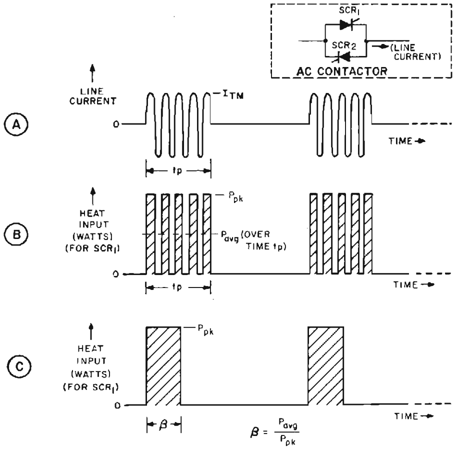


FIGURE 3.11 APPROXIMATING BURSTS OF PULSES WITH SINGLE RECTANGULAR PULSE OF POWER

Sample Problem: Half wave sinusoidal current flows through a C35 SCR at 60 Hz. The full cycle average value of this current is 10 amperes. Approximate the heating effect of a sequence of four cycles of current by a single rectangular wave of power.

Solution:

$I_{TM} = \pi I_{avg} = 10\pi = 31.4$ amperes

$V_{DM} = 1.7$ volts at 31.4 amps from published specifications on C35

$P_{peak} = I_{TM} \times V_{DM} = 31.4 \times 1.7 = 53.4$ watts

Full cycle average P = 16 watts at 10 amps average current from published specifications on C35

P_{avg} over 3½ cycles (actual duration of heating) $= 16 \times \frac{4}{3\frac{1}{2}} = 18.3$ watts

$$\beta = P_{avg}/P_{peak} = 18.3/53.4 = 0.34$$
$$t = 3.5 \text{ cycles} \times 1/60 \text{ cps} = .0585 \text{ second}$$
$$\beta t = 0.34 \times .0585 = 0.020 \text{ second}$$

Thus the heating effect of the four cycles of current can be approximated by a single rectangular pulse of power with amplitude of 53.4 watts and a duration of 0.020 second. This is a conservative approximation.

3.6.3 Resistance Welding Ratings for Recurrent Pulse Bursts

Recurrent waveforms similar to those shown for Figure 3.11 are required for SCR's used in welding service as AC contactors. In order to aid the application of SCR's for this special application[6] a rating format has been developed and is shown in Figure 3.12.

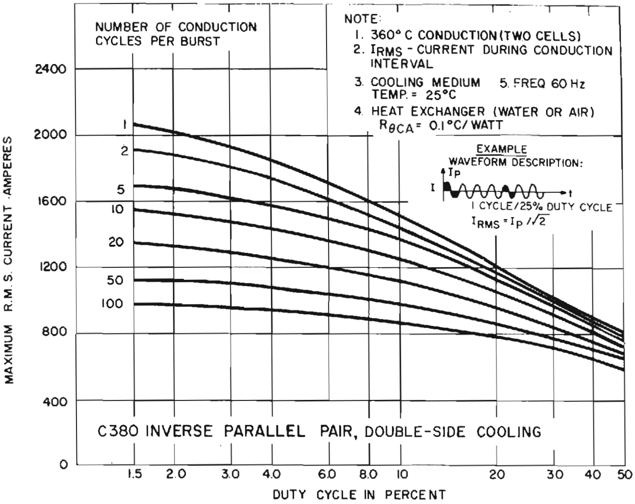


FIGURE 3.12 RESISTANCE WELDING RATINGS FOR THE C380 SERIES SCR PAIR

The welding ratings relate the maximum RMS line current, for the conduction interval, of a pair of SCR's (shown in Figure 3.11A) to the number of cycles in the burst and the burst duty cycle. In addition cooling variables such as ambient temperature and case to sink thermal path are taken into consideration by providing a family of curves such as Figure 3.12 for different values of T_A and $R_{\theta JC}$.

Sample problem: Pair of C380's are used as a resistance welding ac contactor. Welder duty cycle and burst cycles are to be set at ten percent and two cycles, as shown in Figure 3.13A. Assuming the cooling conditions of Figure 3.12, maximum allowable RMS current during the conduction interval is 1450 amperes.

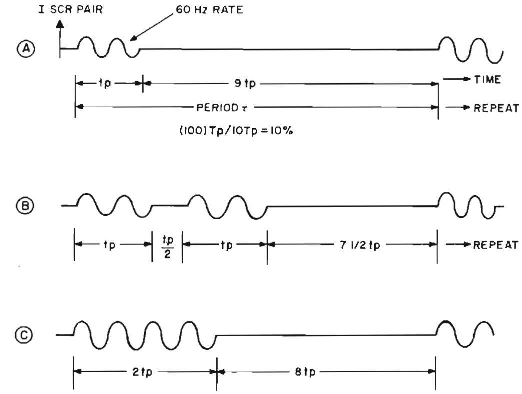


FIGURE 3.13 SIMPLIFIED RESISTANCE WELDING WAVEFORMS

Figure 3.13B displays another example welding waveform which does not fit the rating format of Figure 3.12. By use of the principle depicted in Section 3.6.2 and Figures 3.10 and 3.11 the waveform of Figure 3.13B can be made to fit the format as shown in Figure 3.13C where the waveform of Part B is bunched together resulting in a "worst case" approximation. The resulting on-state RMS line current using a pair of C380's with the cooling conditions as stated in Figure 3.12 is 1150 amperes RMS at the equivalent translated duty cycle of 20% and 4 cycle burst.

3.7 RECURRENT AND NON-RECURRENT di/dt RATINGS

3.7.1 Introduction

In many cases the SCR may be assumed to turn on instantaneously. This assumption is valid if the rate of rise of anode current (di/dt) is slow compared to the time required for the semiconductor junctions to reach a state of full on-state conduction at uniform current density.

The current ratings discussed in the preceding sections are based on such a condition of uniform current density. In other words, the peak junction temperature, on which the recurrent and non-recurrent current ratings are based, is assumed to occur uniformly across the entire junction.

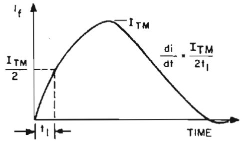
In cases where the rate of rise of anode current (di/dt) is very rapid compared to the spreading velocity of the turn-on process across the junctions, local "hot spot" heating will occur due to high current density in those junction regions that have started to conduct.[7,8] Particularly, if the SCR is switched from a high blocking voltage at a very

large value of di/dt, turn-on switching dissipation in localized regions of the SCR may lead to an excessive temperature rise at a "hot spot" exceeding the device temperature rating.

In a manner analogous to Section 3.5.1 the rate of rise of anode current ratings are subdivided into two industry classifications; recurrent and non-recurrent ratings. In addition to the industry standard, General Electric uses a more stringent recurrent rating method called a concurrent rating, which is part of a comprehensive high frequency rating technique discussed in Section 3.8.

3.7.2 Industry Standard di/dt Rating (Recurrent)

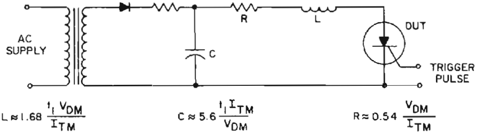
The rating includes a standard waveform and accompanying set of test conditions as outlined in Figure 3.14. The rating guarantees that the device will block voltage but does not guarantee maintenance of device dynamic characteristics such as turn-off time and dv/dt capability.



(a) TEST CURRENT WAVEFORM

TEST PARAMETER		RECOMMENDED VALUES
I_{TM}	–	≥ TWICE DEVICE CURRENT RATING
t_1	–	≥ 1µs
TEST REP RATE		≥ 60 PPS
TEST TEMPERATURE	–	MAX RATED VALUE
OFF-STATE VOLTAGE	–	RATED VALUE
GATE TRIGGER PULSE	–	20V/20Ω, t_r = 1µs, t_p = 3µs
TEST DURATION	–	≥ 1000 HOURS

(b) TEST CONDITIONS



(c) TEST CIRCUIT

FIGURE 3.14 INDUSTRY STANDARD DI/DT TEST CIRCUIT

Both turn-off time and dv/dt capability are limited by the hottest spot of the silicon junction during the commutation interval. Figure 3.15 shows the resulting higher hot spot temperatures which may be generated during high frequency operation due to turn-on di/dt heating. Therefore it is concluded that the industry standard test, while valid for low frequency operation, is not adequate for high frequency characterization.

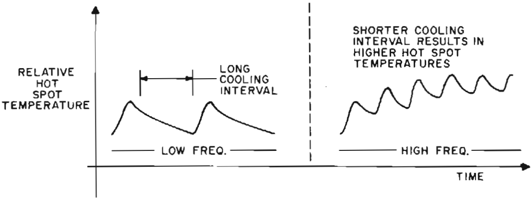


FIGURE 3.15 HOT SPOT TEMPERATURE VS REPETITION RATE

3.7.3 Concurrent di/dt Rating (Recurrent)

To overcome the limitations of the above rating method General Electric's di/dt rating concurrently takes into account the following parameters as test conditions.

1. Turn-off time guarantee specifying reapplied dv/dt and reverse voltage.
2. Snubber circuit discharge.
3. Gate drive.
4. Switching voltage.
5. Case temperature.
6. Complete load current waveform, square wave and sine wave.
7. Above rated over full operating frequency range of device capability.
8. Test duration ≧ 1000 hours.

Figure 3.16 details the definition of the di/dt waveform. The rated di/dt of the device is in addition to the discharge of the RC snubber circuit (when employed) shown connected in parallel with the SCR. For all high-frequency ratings, the SCR shunted by the snubber has been considered as the device under test.

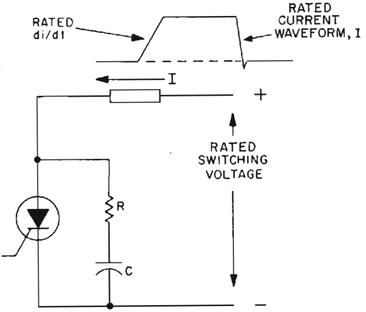


FIGURE 3.16 di/dt WAVEFORM DEFINITION

3.7.4 Industry Standard di/dt Rating (Gate Triggered—Non-Recurrent)

This rating is useful in conjunction with protective devices such as fuses and circuit breakers. The test condition is identical to the recurrent industry standard test except that the test duration is five seconds minimum. Furthermore, immediately after each current pulse, off-state (blocking) voltage capability may be temporarily lost for durations less than the period of the applied pulse repetition rate.

3.7.5 Industry Standard di/dt Rating ($V_{(BO)}$ Triggered—Non-Recurrent)

The same conditions as the rating described in Section 3.7.4 are used except that the device is triggered on by slowly exceeding the device's forward breakover voltage. Generally the di/dt capability for $V_{(BO)}$ breakover is limited to a small fraction of its gate triggered value.

3.7.6 Turn-On Voltage

A convenient indirect relative measure of an SCR's di/dt performance is the value of its turn-on voltage characteristic at a given current and time and under specified test conditions. Figure 3.17 shows a frequently used sinusoidal anode test current waveform i_A and the simultaneous fall of SCR anode to cathode voltage v_F. Turn-on voltage V_{TON} is defined as the value of voltage at the time of peak current I_{TM}. Common values used for current pulse width t_p are 10 microseconds, peak current 150 A, with typical values of V_{TON} in the range of 3 to 30 volts.

The significance of V_{TON} lies in the fact that it is a measure of the current density in the device at the time it is measured. A lower voltage drop indicates a greater amount of active device area turned on, and thus better turn-on switching, or di/dt, performance. Relative tests of this nature can be conducted in the test circuit shown in Figure 3.14.

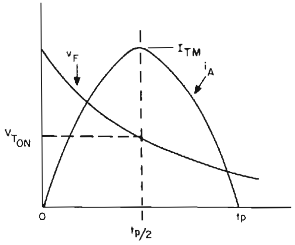


FIGURE 3.17 DEFINITION OF TURN-ON VOLTAGE

This test is most useful for short pulses. For wider pulses, and a comprehensive measurement of switching performance, the user is urged to refer to watt-second loss data as described in the next section.

3.8 HIGH FREQUENCY CURRENT RATINGS

As the frequency of switching is increased, the contribution of the per cycle turn-on switching loss integrated over the period of one cycle of operation becomes an increasingly significant part of the total average power dissipation of the thyristor. In order to properly apply the device under this condition switching losses must be considered.

The following discusses the two major types of high frequency current ratings which account for switching losses.

3.8.1 High Frequency Sinusoidal Waveshape Current Ratings

Sinusoidal current waveshapes are commonly seen by all SCR's used in medium to high frequency inverter circuits, used both as the main switch, and as the companion auxiliary commutating switch. In addition there is a large requirement for SCR's used as auxiliary commutating switches in low frequency inverters where the main current handling switch (SCR) sees basically a rectangular current waveshape. Sinusoidal waveforms are used so extensively for two reasons. First, at high frequencies and/or narrow pulse widths the SCR switching stresses are considerably lower for sinusoidal pulses than for rectangular shaped pulses having the same base width, frequency and RMS current. This results in a higher RMS current handling capability at high frequencies for the sinusoidal waveform operation as shown in Figure 3.18 for the GE C158/C159 SCR.

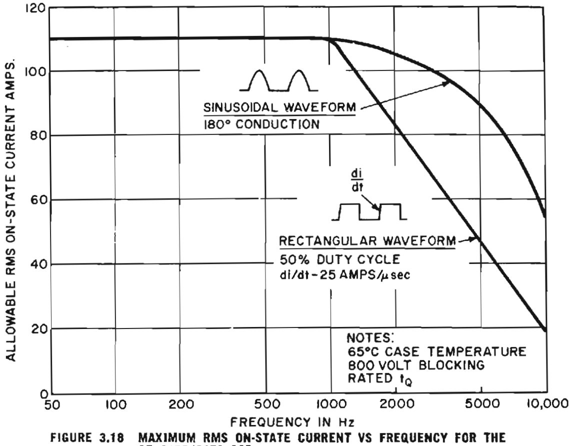


FIGURE 3.18 MAXIMUM RMS ON-STATE CURRENT VS FREQUENCY FOR THE GE C158/C159 SCR

Secondly, forced commutation circuits are generally composed of L-C reactive components which force nearly sinusoidal currents through the commutating switch.

Rating data is given by providing plots of maximum allowable RMS current vs pulse width over the operating frequency range of the device as shown in Figure 3.19 for the GE C158/C159 type SCR.

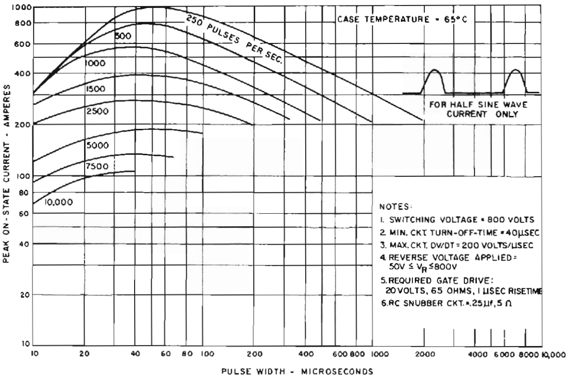


FIGURE 3.19 MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS PULSE WIDTH ($T_C = 65°C$) FOR THE GE C158/C159 SCR

The ratings[9] of Figure 3.19 reflect General Electric's concurrent rating concept by specifying all circuit conditions, thus insuring device commutation under the highest stress conditions. The device's di/dt capability is an inherent part of the rating being reflected in the rate of rise of the sinusoidal waveform. Curve sets are provided for case temperatures other than 65°C to allow extrapolations of current based on the designer's individual application.

The curves are generated by empirical life testing in combination with computer models. UNLIKE THE LOW FREQUENCY CURRENT RATING CURVES, THE HIGH FREQUENCY RATING DATA IS NOT DIRECTLY OBTAINED FROM AVERAGE POWER DISSIPATION AND MAXIMUM JUNCTION TEMPERATURE LIMITATIONS IN COMBINATION WITH THERMAL RESISTANCE DATA. The reason for this departure in rating technique is fundamental to the difference between high and low frequency device operation. At low frequency the device is assumed to have its power losses spread evenly across the silicon wafer and consequently to be at a uniform temperature. At high frequencies device losses tend to concentrate near the turn-on region of the silicon wafer resulting in high power densities even at relatively low average dissipation levels.

Average device power dissipation must be known if the heatsink is to be sized properly to keep the case temperature maintained at the

value required by Figure 3.19. Average power is determined by use of Figure 3.20 for the C158/C159 type SCR.

The energy loss data curves continue the concurrent rating concept mentioned earlier in this section and in Section 3.7.3, by including total device losses comprised of the following components:

a) Blocking losses
b) Switching* and conduction losses
c) Reverse recovery losses
d) Gate power dissipation losses

*Including component due to snubber discharge.

The average power is found by multiplying the watt second/pulse found from Figure 3.20 for the current waveshape the device is switching with the switching repetition rate.

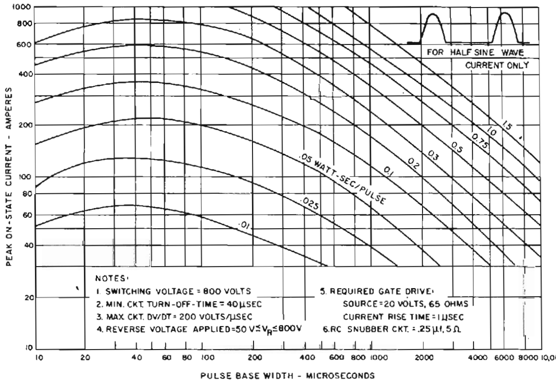


FIGURE 3.20 ENERGY PER PULSE FOR SINUSOIDAL PULSES FOR THE GE C158/C159 SCR

3.8.2 High Frequency Rectangular Waveshape Current Ratings

Rectangular[10] current waveforms are the mainstay of switching SCR's operating in low to medium frequency power conversion systems. Popular examples of circuitry imposing this type of duty on the main power switches are pulse width modulated inverters for AC motor speed control and DC choppers for DC motor speed control.

To fully characterize an SCR under rectangular current waveform conditions, four parameters are needed to define the operating waveform as shown in Figure 3.21 and a fifth, case temperature, is needed to specify thermal conditions.

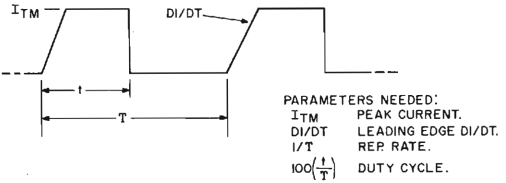


FIGURE 3.21 RECTANGULAR CURRENT WAVEFORM DEFINITION

An example of a current rating curve for the C398 SCR is shown in Figure 3.22. Additional curves are given in the data sheet for 25% and 10% duty cycle operation to allow for interpolation between 75% and 5% duty cycle operation. Like the sine wave rating curves, data is also provided for other case temperatures to again allow for data interpolation.

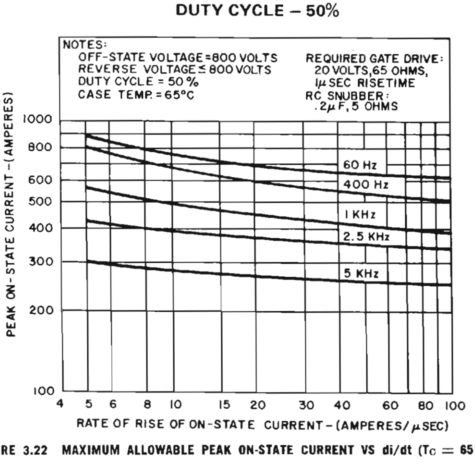


FIGURE 3.22 MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS di/dt ($T_C = 65°C$)

Switching loss data for heatsink selection is given in the form of watt-seconds/pulse data as shown in Figure 3.23. Because of the additional parameter, di/dt, needed to characterize the rectangular waveform, three such charts are needed where a single chart was adequate for the sinusoidal waveform case. The two additional charts characterize the losses for 25 and 5 amps/μsecond respectively; again, interpolation is employed to determine losses for di/dt's in between those given.

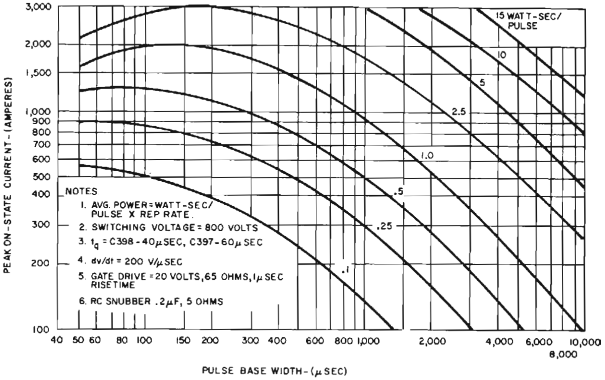


FIGURE 3.23 ENERGY PER PULSE FOR RECTANGULAR PULSES FOR THE C397/C398 SCR ($di/dt = 100$ A/μsec)

3.9 VOLTAGE RATINGS

The voltage ratings of SCR's have been traditionally designated by a single suffix letter, or single letter group, in the model number of the device (e.g., C35B) or are an integral part of its JEDEC registration. The designation is translated in the specifications and defines the thyristor's rated peak voltage which the device will safely withstand in both the off-state and reverse directions without breaking down. The off-state was formerly referred to as the forward direction, i.e., anode positive with respect to the cathode of an SCR. It is applicable to any junction temperature within the specified operating range. This symmetry of off-state and reverse voltage ratings is characteristic of all standard low frequency SCR's. Symmetry does not always exist for high frequency, inverter type SCR's. Where symmetry fails to exist the device voltage grade may be specified by more than one letter group separated by a number, dash or slash. An example is the C138N10M with a V_{DM} of 600 volts and a V_{DRM} of 800 volts. This particular device type also has a V_{RRM} rating of 50 volts which is not described in the type number designation.

Voltage ratings are related to several device parameters and characteristics. Of primary concern is the blocking current and its relationship to device junction temperature. Blocking current approximately doubles with every 10°C rise in T_J. Since junction temperature is a direct function of total device power dissipation, it is possible to have regenerative thermal runaway of an SCR if the SCR's heatsink is above a critical value.[11] Generally this value is many times higher than typically used to dissipate the SCR's losses due to current conduction. This is certainly true of all the low frequency, slow turn-off SCR's currently made. For fast turn-off, high frequency operation blocking

current is traded off against enhanced turn-off time performance. The higher blocking losses that result require a special rating format for such devices if full advantage is to be taken of the device's inherent voltage capability. The following discussion first considers the standard voltage ratings which are applicable to both low and high frequency SCR's. Later the special requirements of some high frequency SCR's are discussed.

3.9.1 Reverse Voltage (V_{RRM}) and (V_{RSM})

In the reverse direction (anode negative with respect to cathode), the SCR behaves like a conventional rectifier diode. General Electric assigns two types of reverse voltage ratings: repetitive peak reverse voltage with gate open, V_{RRM} (formerly designated by "$V_{ROM(rep)}$"); and non-repetitive peak reverse voltage with gate open, V_{RSM} (formerly designated "$V_{ROM(non\text{-}rep)}$").

If these ratings are substantially exceeded, the device will go into breakdown and may destroy itself. Where transient reverse voltages are excessive, additional V_{RRM} margin may be built into the circuit by inserting a rectifier diode of equivalent current rating in series with the controlled rectifier to assist it in handling reverse voltage. For a detailed discussion on voltage transients, see Chapter 16; for series operation, see Chapter 6.

3.9.2 Peak Off-State Blocking Voltage (V_{DRM}) (Formerly Peak Forward Blocking Voltage (V_{FXM}))

The peak off-state blocking voltage V_{DRM} is given on the specification bulletin at maximum allowable junction temperature (worst case) with a specified gate bias condition. The larger SCR's are specified for a peak off-state blocking voltage rating with the gate open; smaller SCR's are usually characterized for a peak off-state blocking voltage with a specified gate-to-cathode bias resistor. The SCR will remain in the off-state if its peak off-state voltage rating is not exceeded.

3.9.3 Peak Positive Anode Voltage (PFV)*

An SCR can be turned on in the absence of gate drive by exceeding its off-state breakover voltage characteristic $V_{(BO)}$ at the prevailing temperature conditions. Although SCR's, in contrast to diode thyristors, are designed to be brought into conduction by means of driving the gate, breakover in the off-state direction is generally not damaging provided the allowable di/dt under this condition is not exceeded (see Section 3.7).

Some SCR's are assigned a PFV rating. This rating is usually at or above the V_{DRM} rating. Off-state voltage which causes the device to switch from a voltage in excess of its PFV rating may cause occasional degradation or eventual failure. Figure 3.24 illustrates the relationship between PFV and peak off-state blocking voltage rating V_{DRM}.

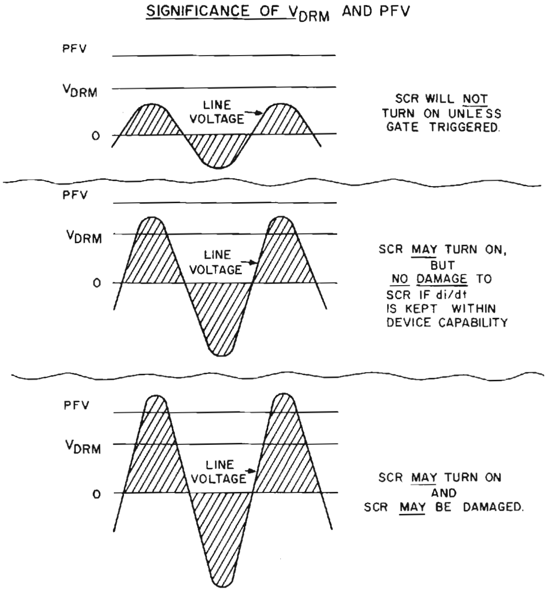


FIGURE 3.24 SIGNIFICANCE OF V_{DRM} AND PFV RATINGS

The PFV rating is often of practical importance when SCR's are tested for their actual breakover voltage characteristic $V_{(BO)}$ at room temperature; often a unit will have a $V_{(BO)}$ beyond its PFV rating at temperatures lower than maximum rated junction temperature. A proper test for $V_{(BO)}$ under these circumstances would be to conduct it at elevated temperature provided that $V_{(BO)}$ is lower than PFV.

In applications where the PFV rating of an SCR may be exceeded it is suggested that a network be connected anode to gate so that the device will trigger by gate drive rather than by off-state breakover. A zener diode may be used to effect gate triggering at a predetermined level, or a Thyrector diode may be used to obtain a similar action.

*Previously referred to as peak forward voltage. PFV is used as an abbreviation.

3.9.4 Voltage Ratings for High Frequency, Blocking Power Limited SCR's

Inverter circuits frequently impose short time repetitive peak off-state and reverse voltages upon SCR's. These transients are often induced by the forced commutation circuits. Typically these transients

are in the 5 to 100 microsecond range and occupy less than 33% of the blocking interval. In some circuits feedback diodes placed across the SCR limit the reverse blocking voltage to only a few volts, typically 2 volts and always less than 50 volts.

In order to allow high frequency SCR's to block these short time repetitive transients and yet not arbitrarily limit their voltage rating due to high blocking losses at the high voltage levels a new rating definition has been introduced as shown in Figure 3.25.

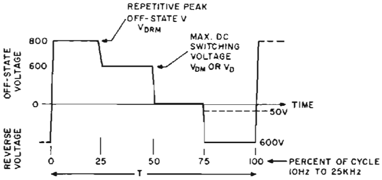


FIGURE 3.25 ALLOWABLE VOLTAGE ENVELOPE FOR C138N10M AND C139N10M SCR'S

Basically the difference between this rating and the conventional is the limitation on the duty cycle of V_{DRM} to confined limits. The V_{DRM} value is specified by the first letter code of the C139. The second letter code indicates the V_{DM} value. Any voltage envelope may be applied to the device providing it is held to within the envelope prescribed in Figure 3.25 for the C139N10M and within the same envelope with the addition of the 50 volt reverse limit for the C138N10M.

Furthermore, the C139N10M case to ambient thermal resistance must not exceed 3.0°C/watt. Should the designer choose to operate outside the voltage envelope shown, the factory must be consulted and a lower value of R_θ (case to ambient) may have to be used in order to maintain device thermal equilibrium. As the state of the art advances and as experience is obtained with this rating philosophy, it is expected that additional information will be provided the designer to enable direct calculation of both the blocking losses and the related maximum R_θ (case to ambient) for maintenance of device thermally stability.

3.10 RATE OF RISE OF OFF-STATE VOLTAGE (dv/dt)

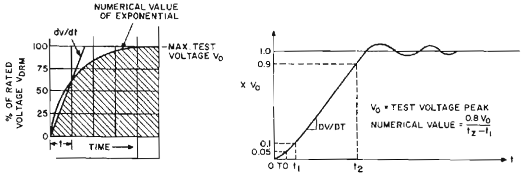
A high rate of rise of off-state (anode-to-cathode) voltage may cause an SCR to switch into the "on" or low impedance conducting state. In the interest of circuit reliability it is, therefore, of practical importance to characterize the device with respect to its dv/dt withstand capability.

The circuit designer may often limit the maximum dv/dt applied to an SCR by means of added suppressor or "snubber" networks placed across a device's terminals. Chapter 16 includes useful design information for the design of such networks.

General Electric SCR's and triacs are characterized with respect to dv/dt withstand capability in the following contexts:

3.10.1 Static dv/dt Capability

This specification covers the case of initially energizing the circuit or operating the device from an anode voltage source which has superposed fast rise-time transients. Such transients may arise from the operation of circuit switching devices or result from other SCR's operating in adjacent circuits. Interference and interaction phenomena of this type are discussed further in Chapter 17. The industry standard dv/dt definitions are defined by the waveforms shown in Figure 3.26.



(a) Exponential Waveform Test (b) Linear Waveform Test

FIGURE 3.26 dv/dt WAVEFORM DEFINITION

Either a linear ramp or the exponential waveform may be used. When the exponential ramp is used the slope is defined as shown by the linear ramp of Figure 3.26(a) intersecting the single time constant value as shown. The linear waveform definition of Figure 3.26(b) is self explanatory. The following discussion applies to the exponential case used for industry registration purposes.

Some specification sheets give the time constant τ under specified conditions rather than a numerical value for dv/dt.

It will be noted that

$$\tau = \frac{0.632 \times \text{Rated SCR Voltage } (V_o)}{dv/dt} \tag{3.5}$$

The initial dv/dt withstand capability will be recognized as being greater than the value defined in Figure 3.26(a). In terms of specified minimum time constant it is

$$\left. dv/dt \right|_{t=0+} = \frac{\text{Rated SCR Voltage } (V_o)}{\tau} \tag{3.6}$$

In terms of specified maximum dv/dt capability, the allowable initial dv/dt withstand capability is

$$\left. dv/dt \right|_{t=0+} = \frac{1}{0.632}\, dv/dt = 1.58\, dv/dt \tag{3.7}$$

The shaded areas shown in Figure 3.26 represent the area of dv/dt values that will not trigger the SCR. These data enable the circuit designer to tailor his circuitry in such a manner that reliable circuit operation is assured.

Static dv/dt capability is an inverse function of device junction temperature as well as a complex function of the transient waveform shape. Figure 3.27 shows one example of how wave shape can greatly change the withstand capability of a typical SCR.

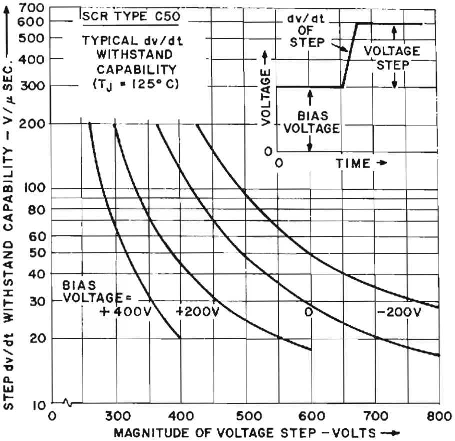


FIGURE 3.27 TYPICAL dv/dt WITHSTAND CAPABILITY OF C50 SCR

Reverse biasing of the gate with respect to the cathode may increase dv/dt withstand capability beyond that shown on an SCR's data sheet. This increase is generally limited to medium and low current SCR's. The reader is referred to Chapter 1 for further discussion.

3.10.2 Reapplied dv/dt

This specification generally forms part of an SCR's turn-off time specification and is really a turn-off time condition, rather than a specification in its own right. It is defined as: the maximum allowable rate of reapplication of off-state blocking voltage, while the SCR is regaining its rated off-state blocking voltage V_{DRM}, following the device's turn-off time t_q under stated circuit and temperature conditions. The waveform is defined in Figure 3.28. For further information consult Chapter 5.

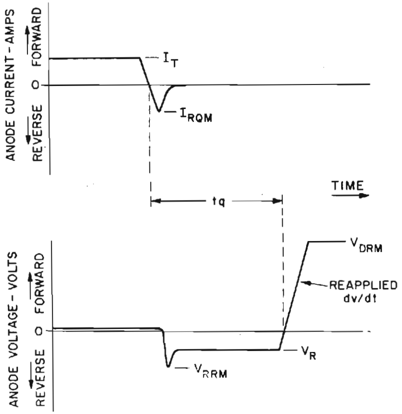


FIGURE 3.28 REAPPLIED dv/dt WAVEFORMS

3.10.3 Triac Commutating dv/dt

Commutating dv/dt[12] differs from both the static and reapplied dv/dt in that it presupposes device commutation immediately prior to application of off-state voltage as shown in Figure 3.29. Commutating dv/dt is generally substantially below a triac's static dv/dt rating. Commutating di/dt, case temperature and RMS on-state current are all conditions for the commutating dv/dt specification.

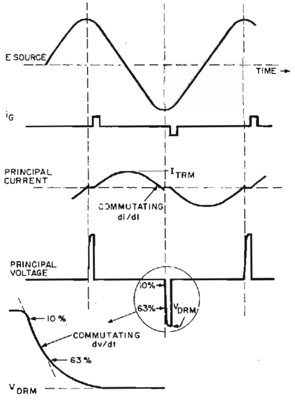


FIGURE 3.29 WAVEFORM OF COMMUTATING dv/dt

Since commutating dv/dt varies with commutating di/dt, the factory should be consulted for operation of triacs beyond 60 Hz. Standard selections are available for 400 Hz operation upon request. Figure 3.30 shows the typical variation of triac commutating dv/dt with commutating di/dt. Consult Chapter 7 for additional detail.

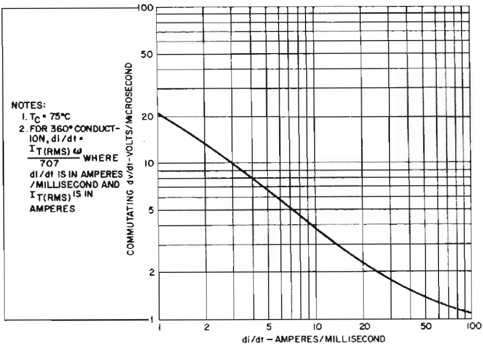


FIGURE 3.30 TYPICAL RATE OF REMOVAL OF CURRENT (di/dt) EFFECT UPON COMMUTATING dv/dt

3.11 GATE CIRCUIT RATINGS

Maximum ratings for the gate circuit are discussed in Chapter 4.

3.12 HOLDING AND LATCHING CURRENT

Somewhat analogous to the solenoid of an electromechanical relay, an SCR requires a certain minimum anode current to maintain it in the "closed" or conducting state. If the anode current drops below this minimum level, designated as the holding current, the SCR reverts to the forward blocking or "open" state. The holding current for a typical SCR has a negative temperature coefficient; that is, as its junction temperature drops its holding current requirement increases. This increase in both holding and latching current may be limiting in military applications where −65°C operation is required. THE DESIGNER IS URGED TO TAKE SPECIAL PRECAUTIONS TO INSURE AGAINST LATCHING AND HOLDING CURRENT PROBLEMS AND BY CONSULTING THE FACTORY WHERE DOUBT MAY EXIST.

A somewhat higher value of anode current than the holding current is required for the SCR to initially "pickup." If this higher value of anode latching current is not reached, the SCR will revert to the blocking state as soon as the gate signal is removed. After this initial pickup action, however, the anode current may be reduced to the holding current level. Where circuit inductance limits the rate of rise

of anode current and thereby prevents the SCR from switching solidly into the conducting state, it may be necessary to make alterations in the circuit. This is discussed further in Chapter 4.

A meaningful test for the combined effects of holding and latching current is shown in Figure 3.31. The SCR under test is triggered by a specified gate signal, under specified conditions of voltage, anode current, pulse width and junction temperature.

The test circuit allows the SCR to latch into conduction at a current level I_{F1}. The test circuit then reduces the current to a continuously variable level I_{F2}. The current I_{F2} at which the SCR reverts to the off-state is the desired value of holding current. See Chapter 20 for details of a suitable test circuit.

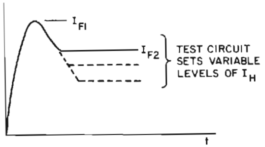


FIGURE 3.31 HOLDING CURRENT TEST WAVEFORM

3.13 REVERSE RECOVERY CHARACTERISTICS

During commutation SCR's display a transient reverse current that far exceeds the maximum rated blocking current. This reverse current is called reverse recovery current and its time integral is termed recovered charge. Figure 3.32 defines the salient reverse recovery parameters. The cross-hatched area represents a common industry method of defining recovered charge (Q_{RR}), along with a method for defining recovery time (t_{rr}). T_4 is arbitrarily chosen to occur at intersection of the dotted line drawn from i_R through the $i_{R/4}$ point, intersecting with the zero current value. Thus defining recovery time as $T_4 - T_1$. Attempts at using lower values than ($i_{R/4}$) for the definition run into the problem of measuring T_3 accurately for very soft recovery devices where the recovery current slope may be very gradual.

Recovered charge is often specified in preference to t_{rr} due to its strong application orientation. Specifically where the voltage across the device must be limited by an R-C snubber network in series applications, the size of the capacitor required is determined by the SCR's recovered charge characteristics (see Chapter 6 for details).

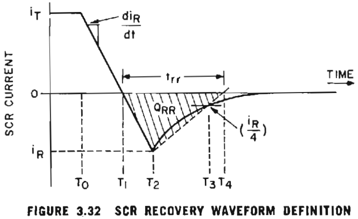


FIGURE 3.32 SCR RECOVERY WAVEFORM DEFINITION

Figure 3.33 shows an SCR's typical recovered charge characteristics.

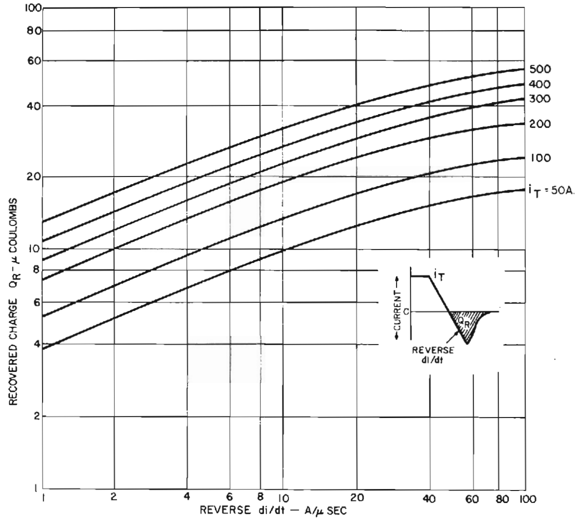


FIGURE 3.33 TYPICAL RECOVERED CHARGE (125°C) C158 SCR

It is to be noted that both Q_{RR} and t_{rr} are strongly circuit dependent as well as device dependent. Both the peak-on-state current prior to commutation as well as the commutation di/dt are significant circuit variables. Additionally recovered charge has a positive temperature coefficient requiring a fixed junction temperature as part of the test conditions.

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*Refer to Chapter 23 for availability and ordering information.

4 GATE TRIGGER CHARACTERISTICS, RATINGS, AND METHODS

The ability of the triode thyristor (SCR or triac) to switch from nonconducting to conducting state in response to a small control signal is the key factor in its widespread utility for control of power. Proper triggering of the thyristor requires that the source of the trigger signal should supply adequate gate current and voltage, without exceeding the thyristor gate ratings, in accordance with the characteristics of the thyristor and the nature of its load and supply. The trigger source impedance, time of occurrence and duration of the trigger signal, and off-state conditions are also important design factors. Since all applications of thyristors require some form of triggering, this chapter is devoted to the fundamentals of the gate triggering process, gate characteristics and ratings, interaction with the load circuit, characteristics of active trigger-circuit components, and basic examples of trigger circuits. This chapter will be devoted mostly to SCR's, while Chapter 7 contains more details on triac triggering. Specific trigger circuits for performing various control functions are shown in subsequent chapters.

4.1 THE TRIGGERING PROCESS

Section 1.3 of Chapter 1 and Section 7.1.3 of Chapter 7 describe the two-transistor analogy of the SCR, the junction gate and remote gate operation of the triac, and the remote-base transistor action of the SCR. From those discussions, it can be seen that the transition of a thyristor from the non-conducting to the conducting state is determined by internal transistor-like action.

The switching action, with slowly increasing DC gate current, is preceded by symmetrical transistor action in which anode current increases proportionally to gate current. As shown in Figure 4.1, with a positive anode voltage, the anode current is relatively independent of anode voltage up to a point where a form of avalanche multiplication causes the current to increase. At this point, the small-signal (or instantaneous) impedance (dV/dI) of the thyristor changes rapidly, but smoothly, from a high positive resistance to zero resistance, and thence to increasing values of negative resistance as increasing current is accompanied by decreasing voltage. The negative resistance region continues until saturation of the "transistors" is approached, wherein the impedance smoothly reverts from negative, to zero, to positive resistance.

The criteria for triggering depends upon the nature of the external anode circuit impedance and the supply voltage, as well as the gate current. This can be seen by constructing a load line on the curves of Figure 4.1, connecting between the open-circuit supply voltage, V_L,

and the short-circuit load current, I_A. With zero-gate current, the thyristor characteristic curve intersects the load line at a stable point (1). At a gate current of I_{G1}, the characteristic curve becomes tangential to the load line at a point (2) where the negative resistance of the thyristor is equal in magnitude to the external load resistance. Since this condition is unstable, the thyristor switches to the low-impedance state at stable operating (3). The gate current may now be removed and conduction will be maintained at point (3). If the supply voltage is reduced to V_{L2} the load line will shift and the operating point (3) will move toward the origin. When the load line becomes tangential to the characteristic curve at point (4), the condition is again unstable, and the thyristor reverts back to the high-impedance "off state."

The anode current at point (4) is the "holding" current for this set of conditions. If, instead of reducing supply voltage to reach point (4), the load resistance were increased, the point (5) at which the characteristic curve becomes tangential to the load line occurs at a lower current, which is the holding current for that set of conditions. If the gate current I_{G1} were maintained while supply voltage was reduced to V_{L3}, turn-off would have occurred at point (6), at a lower anode current. A higher gate current, I_{G2} would then be required to trigger the SCR, but reduction of this gate signal below I_{G1} would allow it to switch off, hence the SCR would not have been truly latched in the on-state. The latching current is at least as high as the holding current (at $I_G = 0$), and is higher in some SCR's because of non-uniform areas of conduction at low currents. In those cases, the triggering criterion is not only meeting a negative-resistance intercept condition such as point (2), but also reaching a certain minimum anode current at point (3).

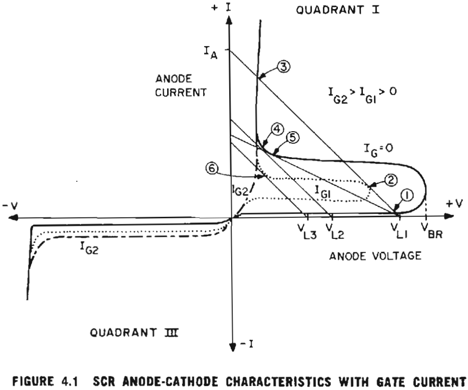


FIGURE 4.1 SCR ANODE-CATHODE CHARACTERISTICS WITH GATE CURRENT

The triac gate characteristics in quadrants I and III appear similar to that of the SCR in quadrant I. It should be remembered that the triac can be triggered with either a positive or negative gate signal

but that the turn-on process will not be perfectly symmetrical for all possible biasing and triggering conditions.

Thyristor triggering requirements are dependent on both anode and gate conditions. Therefore, specifications on a given thyristor's requirements for gate voltage and gate current to trigger (V_{GT} and I_{GT}) also define the anode circuit voltage and load resistance conditions.

4.2 SCR GATE-CATHODE CHARACTERISTICS

Trigger circuits must be designed to produce proper current flow between the gate and cathode terminals of the SCR. The nature of the impedance which these two terminals present to the trigger circuit is a determining factor in circuit design.

From basic construction and theory of operation, it can be seen that the electrical characteristics presented between the gate and cathode terminals are basically those of a p-n junction—a diode. This is not the whole story.

4.2.1 Characteristics Prior to Triggering

Figure 4.2 shows the low-frequency full and simplified equivalent circuits of the gate-to-cathode junction with no anode current flowing (open anode circuit) for both conventional as well as for amplifying gate SCR's. The series resistance R_L represents the lateral resistance of the p-type layer to which the gate terminal is connected. The shunt resistance R_S represents any intentional or inadvertent "emitter short" that may exist in the structure. The magnitudes of R_L and R_S are variables resulting both from structure design and manufacturing process. For example, R_S is extremely high in the C5 type SCR and quite low in the C180 type which features emitter "shorts" to increase its V_{DRM} rating and dv/dt characteristic. The diodes are shown as avalanche ("zener") diodes because the reverse avalanche voltages of SCR gate junctions are typically in the range from 5 to 20 volts, a condition easily encountered in trigger circuits.

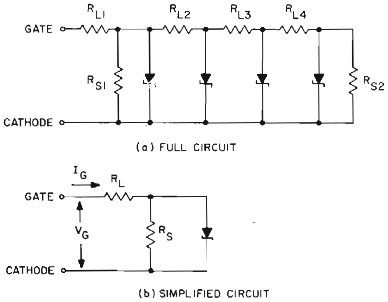


FIGURE 4.2(a) GATE-CATHODE EQUIVALENT CIRCUIT FOR THE CONVENTIONAL SCR

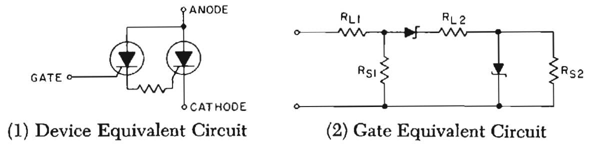


FIGURE 4.2(b) GATE-CATHODE EQUIVALENT CIRCUIT FOR THE AMPLIFYING GATE SCR

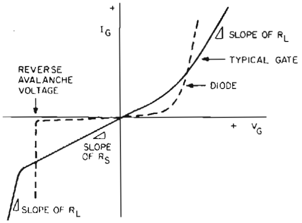


FIGURE 4.3 GATE-CATHODE CHARACTERISTIC CURVE ($I_A = 0$)

The difference between a typical gate characteristic and an ordinary diode junction is shown in Figure 4.3. The relative effects of R_L and R_S are apparent in different regions of the curve.

The equivalent circuit and characteristics shown here are valid only when anode current is zero or small as compared with gate current. This information is, therefore, useful for reverse gate bias, for very low forward gate current, and for examination of trigger circuits with anode disconnected.

4.2.2 Characteristics at Triggering Point

With the anode supply connected, the equivalent gate circuit must be modified, Figure 4.4, to include the anode current flow across the gate junction. Since anode current is a function of gate current (see Chapter 1), the total current through the junction and the voltage drop across the junction will increase more rapidly than with gate drive alone. As anode current increases (Figure 4.5), the small-signal impedance between the gate and cathode terminals changes smoothly from positive, to zero, to negative resistance. When the characteristic curve becomes tangential with the load line of the gate signal source impedance at point (1), the anode current becomes regenerative and the SCR can then trigger. For specification purposes, "I_{GT}" is the maximum gate supply current required to trigger, hence is measured at the peak of the curve (refer to Chapter 20 for test method).

Thus it is apparent that the impedance of the gate signal source is another factor in the criteria for thyristor triggering.

4.2.3 Characteristics After Triggering

After the thyristor has been triggered and anode current flow

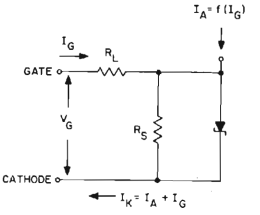


FIGURE 4.4 GATE-CATHODE EQUIVALENT CIRCUIT [$I_A = f(I_G)$]

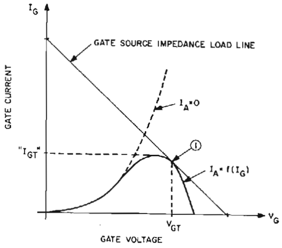


FIGURE 4.5 GATE CHARACTERISTICS, ANODE CONNECTED

across the gate-cathode junction is sufficient to maintain conduction, the gate impedance changes. Figure 4.4, shows that it behaves like a source, having a voltage equal to the gate-cathode junction drop (at the existing anode current) and an internal impedance R_L. This voltage is very nearly equal to the voltage drop between anode and cathode. The characteristics under this condition are shown in Figure 4.6. The curvature in the fourth quadrant is effectively the result of an increasing R_L as more current is taken out of the gate. This is the result of the distributed nature of the gate junction as shown in Figure 4.2. As the gate-to-cathode terminal voltage is reduced by withdrawing current, the current flow through the lateral resistance of the p-type layer causes current to cease flowing through that portion of the p-n junction nearest the gate terminal. This causes an increase in current density in areas remote from the gate terminal. The higher current density and power dissipation in the lateral resistance can cause thermal damage to the thyristor.

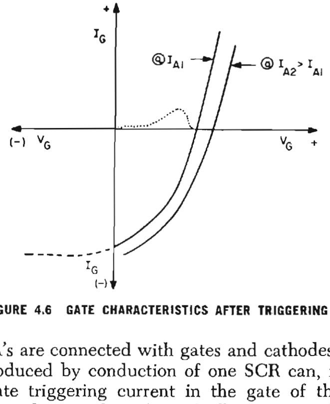


FIGURE 4.6 GATE CHARACTERISTICS AFTER TRIGGERING

If two SCR's are connected with gates and cathodes common, the gate voltage produced by conduction of one SCR can, in some cases, produce adequate triggering current in the gate of the other SCR. In many instances, this may be a desired effect—turning both SCR's on

simultaneously. In other cases, however, as when the anode supply voltages of the two are 180 degrees out of phase, the existence of gate current in the reverse-biased SCR can cause triggering at the instant it becomes forward-biased because of stored charge in the p-type layer. It can also cause excessive reverse current by the remote-base transistor action.

4.3 EFFECTS OF GATE-CATHODE IMPEDANCE AND BIAS

The preceding sections have shown that the criteria for triggering involves the gate current, gate signal source impedance, and anode supply (load) impedance. The interaction between gate and anode circuits demands examination in some depth.

4.3.1 Gate-Cathode Resistance

The two-transistor analogy shows that a low external resistance between gate and cathode bypasses some current around the gate junction, thus requiring a higher anode current to initiate and maintain conduction. Low-current, high sensitivity SCR's are triggered by such a low current through the gate junction that a specified external gate-cathode resistance is required in order to prevent triggering by thermally generated leakage current. This resistance also bypasses some of the internal anode current caused by rapid rate-of-change of anode voltage (dv/dt, see Chapter 3). It raises the forward breakover voltage by reducing the efficiency of the n-p-n "transistor" region, thus requiring a somewhat higher avalanche multiplication effect to initiate triggering. The latching and holding anode currents are also affected by the current which bypasses the gate junction.

The relative effect of the external resistance is dependent upon the magnitudes of the internal resistances, R_L and R_S of Figure 4.2. For low-current thyristors, the type of construction used generally leads to high values of R_S (virtually no emitter shorting) and low values of R_L because of the small pellet size. Figure 4.7 shows the effect of external gate-to-cathode resistance upon holding current for the type C106 low-current SCR. The spread between maximum and minimum values represents production variations of the internal resistances and variations in current-gain of the equivalent "transistor" regions.

External shunt gate resistance also slightly reduces the turn-off time of the SCR by assisting in recovering stored charge, by raising the anode holding current, and by requiring higher anode current to initiate re-triggering.

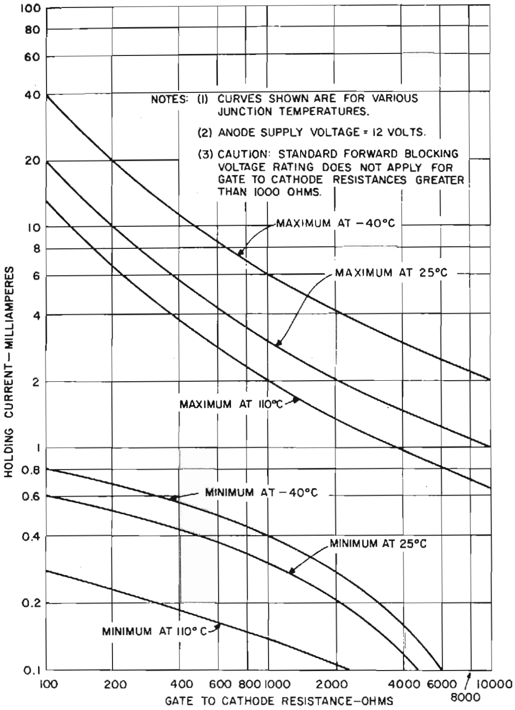


FIGURE 4.7 MAXIMUM AND MINIMUM HOLDING CURRENT VARIATION WITH EXTERNAL GATE-TO-CATHODE RESISTANCE FOR C106 SCR

4.3.2 Gate-Cathode Capacitance

A low shunt capacitive reactance at high frequencies can reduce the sensitivity of a thyristor to dv/dt effects (see Chapter 3), in much the same manner as a resistor, while maintaining higher sensitivity to DC and low frequency gate signals. This integrating effect is particularly useful where high-frequency "noise" is present in either the anode or gate circuits.

At the point of triggering, however, the gate voltage (see Figure 4.5) must increase as anode current increases. Therefore, a capacitor connected between gate and cathode will tend to retard the triggering process, yielding longer delay-time and rise-time of anode current. This action can be detrimental when a high di/dt of anode current is required (see Chapters 3 and 5).

After the SCR has been turned on, the gate acts as a voltage source, charging the capacitor to the voltage drop across the gate junction. Since this voltage (depending on value of anode current) is generally higher than the gate voltage required to trigger the SCR (V_{GT}), the energy stored in the capacitor can supply triggering current for a period of time after removal of anode current, thereby possibly causing the SCR to fail to commutate. In low-current SCR's, a capacitor on the order of 10 microfarads can maintain gate current for over 10 milliseconds, hence can prevent commutation in half-wave, 50 or 60 Hz circuits.

If the gate triggering signal is a low-impedance pulse generator in series with a capacitor, the capacitor can be charged by gate current during the pulse and the polarity will be such that at the end of the pulse the SCR gate will be driven negative. For low values of anode current at this instant, the negative drive may raise the holding current requirement above the anode current and turn off the SCR.

4.3.3 Gate-Cathode Inductance

Inductive reactance between gate and cathode reduces sensitivity to slowly changing anode current or gate source current while maintaining sensitivity to rapid changes. This differentiating effect is useful in improving thermal stability since changes in thermal leakage current are slow. When used with the light-activated SCR, it provides sensitivity to a flash of light with insensitivity to steady-state ambient light (see Chapter 14).

With anode current flowing, the gate voltage causes current to flow out of the gate, through the inductance. The rate at which this current builds up after triggering is a function of the L/R ratio of the inductance to both internal and external resistance. As this negative gate current rises, the holding current of the thyristor also rises. If anode current is low, or increasing more slowly than negative gate current, the thyristor may drop out of conduction.

After the SCR anode current ceases, negative gate current will continue for a period of time, decaying according to the L/R time-constant. This negative gate current during the turn-off condition can reduce turn-off time (by nearly 10:1 in small SCR's) and can permit a faster rate of re-applied off-state voltage (higher dv/dt).

If a triggering current pulse is applied in parallel with an inductor and the gate, the pulse can produce a current flow through the inductor. At the termination of the pulse, the inductor current will continue to flow as a negative gate current, thereby raising holding current and possibly causing turn-off of the SCR.

4.3.4 Gate-Cathode LC Resonant Circuit

A parallel LC resonant circuit connected between gate and cathode can provide a frequency-selective response, and can also produce a condition of oscillation.

The oscillating condition is obtained by making the anode current value intermediate between the normal ($I_G = 0$) holding current and the holding current with maximum negative gate current flowing through the inductor. As explained in Section 4.3.3, the SCR can be turned on, then negative gate current will increase until the SCR turns off. After turn-off, inductor current will charge the capacitor to a negative voltage, then the capacitor will discharge into the inductor in a resonant manner. When the capacitor voltage swings positive again, it can re-trigger the SCR and the process will repeat indefinitely. Damping is required to avoid such oscillation.

4.3.5 Positive Gate Bias

The presence of positive current in the gate when reverse voltage is applied to the anode may increase reverse blocking (leakage) current through the device substantially. As a result, the SCR must dissipate additional power. Therefore it is necessary either to make provision for this additional loss or to take steps to limit it to a negligible value.

Figure 4.8 gives the temperature derating for different SCR lines at various gate drive duty cycle (percent of full cycle or 360 electrical degrees) for values of peak positive gate voltage. For proper application, this loss must be included in the total device dissipation. The temperature derating, ΔT, found from Figure 4.8, must be subtracted from the maximum allowable stud temperature (found from the device rating curve) for the proper cell type and conduction angle. For lead mounted devices, subtract from the ambient temperature curve. Derating becomes negligible if the gate voltage is less than 0.25 volt or the temperature derating turns out to be 1°C or less.

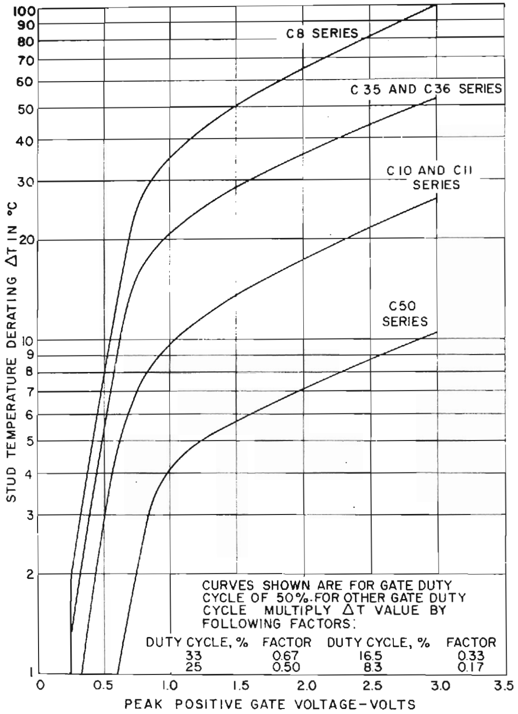


FIGURE 4.8 TEMPERATURE DERATING CURVE FOR SIMULTANEOUS APPLICATION OF POSITIVE GATE PULSE WHEN ANODE IS NEGATIVE

A means of limiting the additional reverse dissipation to a negligible value is given by a gate clamping circuit of the type shown in Figure 4.9 for low and medium current SCR's (C10 and C35 series). Resistor R_A and a diode are connected from gate to anode to attenuate positive gate signals whenever the anode is negative. For a given peak value of open circuit gate source voltage, Figure 4.9 gives the maximum ratio of the value of R_A to R_G that will safely clamp the gate for all values of reverse voltage within the reverse voltage rating of the SCR.

An alternate way to limit additional reverse leakage dissipation due to positive gate voltage is to insert in series with the SCR a recti-

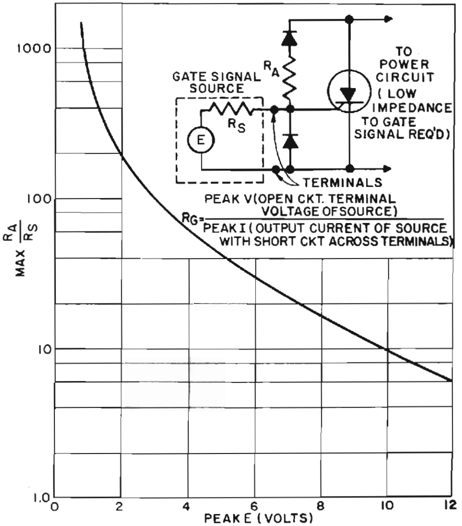


FIGURE 4.9 GATE CLAMP CIRCUIT FOR CONTROLLED RECTIFIER

fier diode that has a lower reverse blocking current. In this manner the diode will assume the greater share of the reverse voltage applied to the series string, significantly reducing reverse dissipation in the SCR.

4.3.6 Negative Gate Bias

The gate should never be allowed to become more negative with respect to the cathode than is indicated on the specification bulletin. For example, the gate of the C35 (2N681) type has a rated peak reverse voltage of 5 volts. If there is a possibility that the gate will swing more negative than the rated value, a diode should be connected either in series with the gate, or from cathode to gate to limit the reverse gate voltage. A considerable negative gate current (conventional current flow out of the gate) can be caused to flow if the cathode circuit between cathode and gate is opened for any reason while the SCR is conducting forward load current (conventional current flow from anode to cathode). This current would initially be limited only by the impedance of the gate circuit and could cause the allowable gate dissipation to be exceeded, thus leading to possible failure of the SCR.

When the anode is positive, negative gate bias tends to increase the forward breakover voltage $V_{(BO)}$ (Section 1.9.1) and the dv/dt withstand capability (Section 1.5) at a given junction temperature for small SCR's without internal emitter shorting. For example, the C5 types (2N1595, C106, etc.) have V_{DRM} specified for a certain value of

gate-to-cathode resistance (R_{GK} = 1000 ohms) and at a specified junction temperature. For more detail on the effect of negative gate bias on small SCR's the reader is referred to Reference 1.

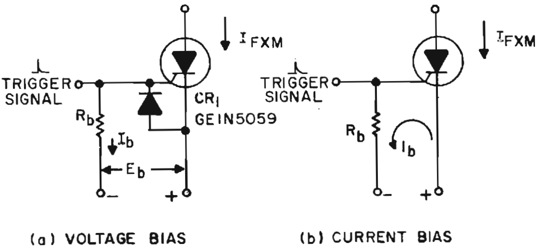


FIGURE 4.10 NEGATIVE GATE BIAS ARRANGEMENTS

Figure 4.10(a) shows a voltage bias arrangement. Resistor R_b is taken to a negative supply instead of being merely returned to the cathode. The voltage source E_b establishes a current $I_b \cong \frac{E_b - D}{R}$, where D is the voltage drop across diode CR1 (typical value 0.7 volt). The diode provides a fixed negative bias voltage gate-to-cathode for the SCR. The disadvantage of this approach, however, is the loss of input sensitivity due to resistor R_b.

Figure 4.10(b) shows a current bias scheme useful for smaller junction diameter SCR's. Resistor R_b and the bias source are selected so that a bias current $I_b \cong I_{FXM}$ is established through resistor R_b in the direction indicated; I_{FXM} is the maximum forward blocking (leakage) current of the SCR under the prevailing junction temperature and anode voltage. Selection of I_b in this manner yields a "worst case" design on the assumption that most, if not all, of I_{DRM} will be diverted from the SCR emitter (gate-cathode junction). This approach is limited to SCR's which have sufficient reverse gate power ratings to handle reverse current I_b at its associated reverse gate voltage. The scheme of Figure 4.10(b) is suitable, for example, for General Electric C5 type SCR's which allow operation of the gate-to-cathode junction in reverse avalanche.

The improvement in dv/dt withstand capability that can be achieved by negative gate biasing is shown in Figure 4.11 for a typical C35 type SCR. It shows the effect of gate bias on the allowable time constant of application of forward blocking voltage without having the SCR switch on. The zero gate voltage curve corresponds to the time constant values given on the C35 specification sheet for the open gate condition. Figure 4.11 extends the usefulness of this information for different values of gate bias.

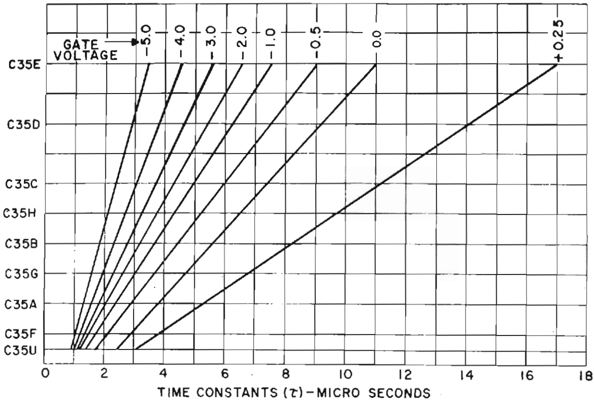


FIGURE 4.11 EFFECT OF GATE BIAS ON ALLOWABLE TIME CONSTANT OF APPLICATION OF FORWARD BLOCKING VOLTAGE

It is possible to design circuits which apply a negative gate bias or short the gate to the cathode only while dv/dt is being applied. These circuits do not degrade the gate signal as much as in Figure 4.10 but are expensive for most applications.

The basic idea is to differentiate the dv/dt applied to the anode, invert the polarity and apply it to the gate. Figure 4.12 shows a transistorized dynamic snubber. R_1C supplies base current to Q_1 turning it on when anode voltage is rising. Gate triggering would be lost during the time of rising dv/dt since the gate is being shunted. However, the insertion of Q_2 avoids this problem since now the gate signal not only triggers the SCR but first shunts the base drive to Q_1. Both Q_1 and Q_2 should be epitaxial transistors with low saturation voltages.

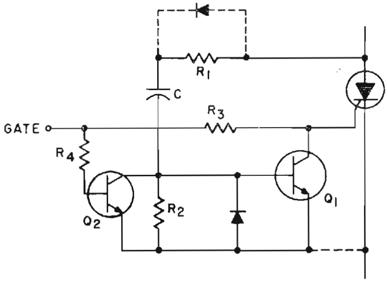


FIGURE 4.12 TRANSISTOR SNUBBER TO IMPROVE dv/dt

Large area devices and devices with emitter shorting are influenced little by gate shorting because of the shunting effects of R_S (Figure 4.2(a)). Unless $V_{(BO)}$ is specified with a bias resistor, conservative circuit design practice should not depend upon increasing $V_{(BO)}$ by negative gate biasing. Some types of SCR's that feature n-type gate structures (C501, C601, etc.) as well as triacs can be triggered by either positive or negative gate signals. Under no circumstances should negative gate vias be used with these types to enhance blocking stability.

The influence of turn-off time by different gate bias techniques seems to be very limited because it is mainly a function of carrier lifetime in an area not accessible by the gate.

4.4 EFFECTS OF ANODE CIRCUIT UPON GATE CIRCUIT

In Section 4.1 it was shown that the anode circuit voltage and impedance were determining factors in triggering. The effect of anode current was discussed in Section 4.2.3. Two other effects are worth noting. Junction capacitance in the SCR can couple high-frequency signals from the anode to the gate circuit which, although they may not cause triggering in themselves, may interfere with normal operation of the trigger circuit.

When the anode voltage of the SCR reaches either the forward breakover or reverse avalanche voltage, a voltage will appear at the gate terminal. In the case of forward breakover voltage, a forward anode current starts flowing which produces a positive gate voltage, as in normal conduction (see Section 4.2.3). When the reverse avalanche voltage is reached, the gate junction becomes reverse biased. Depending on the magnitude of R_S (Figure 4.2) the negative voltage appearing at the gate terminal may rise to the avalanche voltage of the gate junction. If a reverse voltage transient on the anode exceeds reverse avalanche, the reverse-blocking junction of the SCR no longer blocks, thereby applying the transient energy to the gate junction in reverse. The gate junction and any external circuit connected to the gate may then receive excessive voltage and current from this process.

When the SCR is conducting, its gate is essentially at the same potential as its anode. When the SCR is non-conducting, the gate potential is not related to anode potential within the normal operating range. However, during the commutating transition from conduction to non-conduction, the gate goes through an intermediate phase which can result in a large negative voltage appearing at the gate terminal. If an SCR is commutated, as in a DC chopper or flip-flop circuit, by the step application of a reverse bias, the gate voltage will initially be the normal forward gate-cathode junction drop until that junction recovers, whereupon both anode and the gate will go negative. The gate voltage will then follow anode voltage until the main reverse-blocking (p-n) junction recovers, at which time the gate reverts to its normal characteristics. These transitions are readily observed on small SCR's in particular. On larger SCR's, the effects are somewhat masked by lower values of internal shunt resistance R_S. The negative transient at the gate can cause malfunction or damage in the external gate circuit.

4.5 DC GATE TRIGGERING SPECIFICATIONS

The DC gate trigger characteristics of an SCR are presented in the form of a graph similar to Figure 4.13 which applies to the C35 (2N681) type SCR. The graph shows gate-to-cathode voltage as a function of positive gate current (flow from gate to cathode) between limit lines (A) and (B) for all SCR's of the type indicated. These data apply to a zero-anode-current condition (anode open).

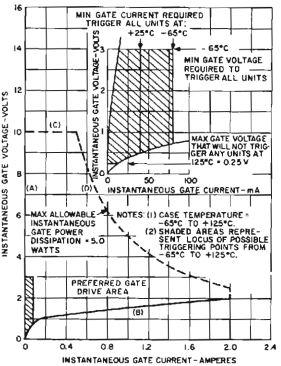


FIGURE 4.13 DC GATE TRIGGERING CHARACTERISTICS (FOR C35 TYPE SCR)

The basic function of the trigger circuit is to simultaneously supply the gate current to trigger I_{GT} and its associated gate voltage to trigger V_{GT}. The shaded area shown in Figure 4.13 contains all the possible trigger points (I_{GT}, V_{GT}) of all SCR's conforming to this specification. The trigger circuit must, therefore, provide a signal (I_G, V_G) *outside* of the shaded area in order to reliably trigger all SCR's of that specification.

This area of SCR gate operation is indicated as the "preferred gate drive area." It is bounded by the shaded area in Figure 4.13 which represents the locus of all specified triggering points (I_{GT}, V_{GT}), the limit lines (A) and (B), line (C) representing rated peak allowable forward gate voltage V_{GF}, and line (D) representing rated peak power dissipation P_{GM}. Some SCR's may also have a rated peak gate current I_{GFM} which would appear as a vertical line joining curves (B) and (D).

The insert in the upper right hand portion of Figure 4.13 shows the detail of the locus of all specified trigger points, and the temperature dependence of the minimum gate current to trigger $I_{GT_{min}}$. The lower the junction temperature, the more gate drive is required for triggering. (Some specifications may also show the effect of forward anode voltage on trigger sensitivity. Increased anode voltage, particularly with small SCR's, tends to reduce the gate drive requirement.) Also shown is the small positive value of gate voltage below which no SCR of the particular type will trigger.

The reverse quadrant of the gate characteristic is usually specified in terms of maximum voltage and power ratings. The application of reverse bias voltage and the extraction of reverse gate current for SCR off-state stability was discussed in Section 4.3.6.

4.6 LOAD LINES

The trigger circuit load line must intersect the individual SCR

gate characteristic in the region indicated as "preferred gate drive area" in Figure 4.13. The intersection, or maximum operating point, should furthermore be located as close to the maximum applicable (peak, average, etc.) gate power dissipation curve as possible. Gate current rise times should be in the order of several amperes per microsecond in the interest of minimizing anode turn-on time particularly when switching into high currents. This in turn results in minimum turn-on anode switching dissipation and minimum jitter.

Construction of a "load line" is a convenient means of placing the maximum operating point of the trigger circuit-SCR gate combination into the preferred triggering area. Figure 4.14(a) illustrates a basic trigger circuit of source voltage e_s and internal resistance R_S driving an SCR gate. Figure 4.14(b) shows the placement of the maximum operating point well into the "preferred trigger" area close to the rated dissipation curve. The load line is constructed by connecting a straight line between the trigger circuit open circuit voltage E_{oc}, entered on the ordinate, and the trigger circuit short circuit current $I_{sc} = \frac{E_{oc}}{R_S}$ entered on the abscissa.

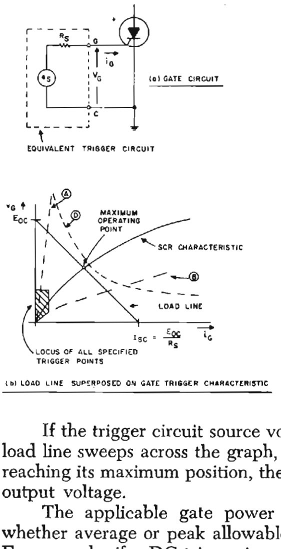


FIGURE 4.14 GATE CIRCUIT AND CONSTRUCTION OF LOAD LINE

If the trigger circuit source voltage is a function of time e_s (t), the load line sweeps across the graph, starting as a point at the origin and reaching its maximum position, the load line, at the peak trigger circuit output voltage.

The applicable gate power curve is selected on the basis of whether average or peak allowable gate power dissipation is limiting. For example, if a DC trigger is used, the average maximum allowable gate dissipation (0.5 watt for C35) must not be exceeded. If a trigger pulse is used the peak gate power curve is applicable (for the C35, the 5 watt peak power curve labeled D in Figure 4.13). For intermediate gate trigger waveforms the limiting allowable gate power dissipation curve is determined by the duty cycle of the trigger signal according to: peak gate drive power $\times$ pulse width $\times$ pulse repetition rate $\leqq$ allowable average gate power.

Inverter type SCR's that require a stiff gate signal because of high di/dt and high frequency operation often have peak pulse gate power curves (Figure 4.15). These pulse curves take advantage of the transient thermal resistance of the gate in order to achieve higher power pulses. But again it must be remembered that the average gate power dissipation should not be exceeded.

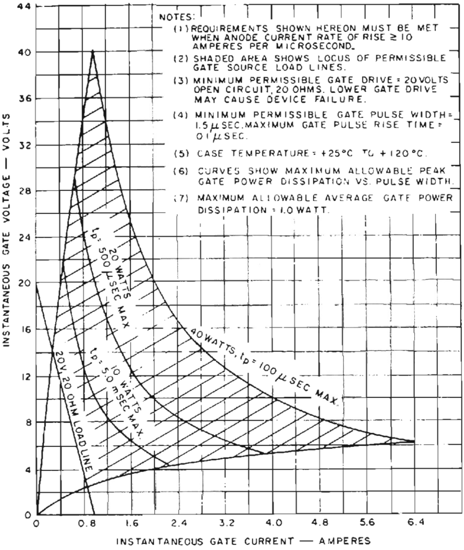


FIGURE 4.15 GATE TRIGGER REQUIREMENTS FOR HIGH FREQUENCY AND HIGH di/dt OPERATION

4.7 POSITIVE GATE VOLTAGE THAT WILL NOT TRIGGER SCR

Figure 4.13 also indicates the maximum gate voltage that will not trigger the SCR. For example, for the C35 (2N681) type, Figure 4.13 shows that at 125°C junction temperature this value is 0.25 volt. This limit is important when designing a trigger circuit which has a standby leakage current when no trigger signal is present. Examples of this are saturable reactors and directly coupled unijunction transistor trigger circuits. To prevent false triggering under these circumstances, a resistor should be connected across the output of the trigger circuit. Its value of resistance in ohms should not exceed the maximum gate voltage that will not trigger divided by the maximum trigger circuit standby current.

4.8 PULSE TRIGGERING

Thyristors are commonly specified in terms of the continuous DC gate voltage and current required to trigger. For trigger pulse widths down to 100 microseconds, the DC data apply. For shorter pulse widths, V_{GT} and I_{GT} increase.

On a short-time basis, thyristors may be generally considered to be charge controlled, as are transistors. The free charge stored within the gate p-type layer of an SCR may be considered to be the difference between the incoming charge flow rate ($dq/dt = I_G$) and the internal recombination rate. Under DC conditions and for a given recombination rate, the free charge is directly a function of gate current. When the free charge reaches a certain level, the device triggers. To get the required charge into the gate in a time that is short compared with the recombination time requires higher current (hence higher voltage) than for DC triggering.

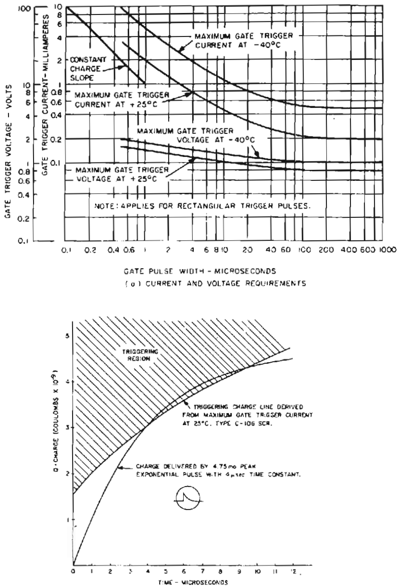


FIGURE 4.16 EFFECT OF TRIGGER PULSE WIDTH (C-106 SCR)

Figure 4.16(a) shows the relationship between pulse width and peak current for a rectangular pulse to trigger the C-106 type SCR. Note that the current curves approach a constant-charge slope at the smaller pulse-widths. The point at which the pulse current curve departs from the DC current level is about 200 microseconds for this small thyristor. Other SCR types, with shorter recombination times, can be triggered with pulse current equal to the DC level down to about 20 microseconds.

It should not be inferred from Figure 4.16(a) that only rectangular pulses are acceptable. Any unidirectional waveshape which does not exceed gate current, voltage, and power ratings may be used if the total charge is adequate. Proper charge criteria may be determined by plotting, as in Figure 4.16(b), the integral of the actual current wave and the integral of the rectangular pulse current. If the two curves cross, the triggering charge is adequate.

Figure 4.17 shows the increase in gate drive required for triggering four types of SCR's with trigger signals of short pulse duration. In order for the SCR to trigger, the anode current must be allowed to build up rapidly enough so that the latching current of the SCR is reached before the pulse is terminated. (Latching current may be assumed to be three times the value of the holding current given on the specification sheet.) For highly inductive anode circuits one must use a maintained type of trigger signal which assures gate drive until latching current has been attained.

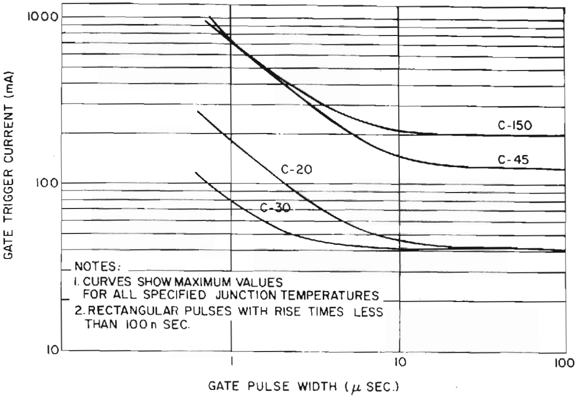


FIGURE 4.17 GATE DRIVE REQUIRED FOR SHORT TRIGGER PULSE DURATION

One situation encountered frequently is that which exists when a capacitor is discharged to provide a latching current pulse in a highly inductive circuit. This situation is depicted in Figure 4.18 of on-state current.

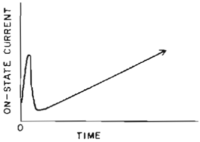


FIGURE 4.18 CURRENT WAVEFORM FOR CAPACITIVE AND INDUCTIVE LOAD

The latching pulse from the capacitor discharge is followed by a slowly rising anode current determined primarily by inductance in the circuit. Very often, confusion exists regarding holding current and latching current in such cases. If the gate trigger pulse ends before the end of the initial current pulse, the device must remain in the on-state at the valley point where the main circuit takes over.

If the device has a holding current higher than the valley current level provided, it will go out of conduction and the circuit will not latch. This is, however, a result of high device holding current rather than latching current. However, if the gate trigger signal lasts beyond the valley point before it is ended and the device still fails to latch, then it is a latching current problem rather than a holding current problem.

The DC gate trigger characteristics are measured on a 100% basis in production for all SCR's, but the pulse trigger characteristics are measured only on a sampling basis. For applications where the pulse trigger characteristics are critical, a special specification should be requested so that satisfactory pulse triggering will be assured.

4.9 ANODE TURN-ON INTERVAL CHARACTERISTICS

Figure 4.19 shows the turn-on, or switching, characteristics of a typical C10 type SCR. It is representative of other SCR types as well. Percent anode voltage is shown as a function of time, following application of the trigger signal at zero time, for switching from 500 volts and from 100 volts for two different circuit current levels.

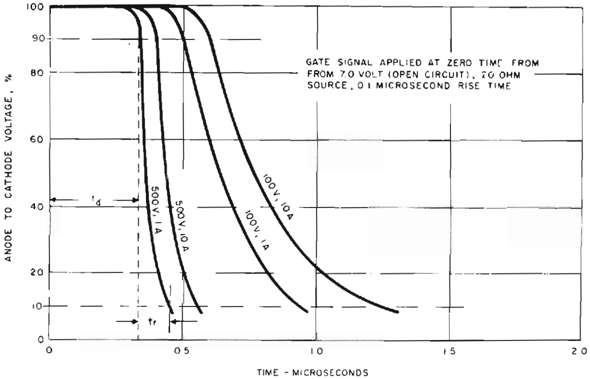


FIGURE 4.19 TYPICAL TURN-ON CHARACTERISTICS OF C10 TYPE SCR

Delay time t_d is shown for the 500 volt/1 ampere switching characteristic. It is defined as the time between the 10% point of the leading edge of the gate current pulse and the 10% point of the anode voltage waveform. The delay time decreases as the amplitude of the

gate current pulse is increased, but approaches a minimum value of 0.2 to 0.5 μsec for gate current pulses of 500 ma or more.

Rise time t_r is defined as the time required for the anode voltage to drop from 90% of its initial value to 10%, as indicated for the 500 volt/1 ampere curve in Figure 4.19. The rise of current as the voltage across the SCR falls is determined largely by the circuit. In a purely resistive circuit the current will rise in the same manner as the voltage falls; hence the term rise time. It is important that the instantaneous voltage-current product during the turn-on interval not exceed the dissipation capability of the SCR. For this reason, the rate of rise of anode current (di/dt) must be limited (see Chapter 3). Rise time, as well as delay time, tends to be reduced by a large gate drive within the allowable gate dissipation ratings of the SCR. Therefore, in order to minimize turn-on switching dissipation, the gate should be driven in the area of "preferred triggering" close to the allowable gate power dissipation curve shown in Figure 4.13. Amplifying gate SCR's do not require as stiff a gate source as conventional thyristors, and therefore, allow the designer greater latitude in selection of a gate drive circuit.

Total turn-on time is defined as $t_{on} = t_d + t_r$. It is important to note that large turn-on switching dissipation can still occur after the termination of the turn-on time as defined above. Particularly, when switching from a high voltage into a large current, applicable switching ratings such as discussed in Chapter 3 should be consulted.

The jitter, or variation of switching time from one cycle to the next, is usually less than 2 mμsec at constant temperature if the gate is driven at two to three times the minimum amplitude required for triggering.

4.10 SIMPLE RESISTOR AND RC TRIGGER CIRCUITS

It is sometimes required to find the simplest and most economical means for triggering an SCR when some performance compromise can be made, particularly with regard to repeatibility over a temperature range. The reader is referred to Reference 2 for a more detailed treatment of simple and low cost SCR trigger circuits.

Figure 4.20 shows a simple method of obtaining gate current for triggering the SCR from the main AC supply whenever the anode is positive with respect to the cathode. As soon as the SCR has triggered, the anode voltage drops to the conduction value and the gate current decreases to zero. Resistor R limits the peak gate current. The diode in the gate circuit is provided to prevent reverse voltage from being applied between cathode and gate during the reverse part of the cycle. If desired, the diode can be connected between gate and cathode rather than in series with R. Conduction is initiated by closing contact S_1 in Figure 4.20(a) or by opening contact S_2 in Figure 4.20(b). Interruption of load current occurs within one-half cycle after opening S_1 or closing S_2 due to line voltage reversal. For more complete static switching circuits, see Chapter 8.

Simple resistor-capacitor-diode combinations will trigger and control SCR's over the full 180 electrical degree range, giving very good

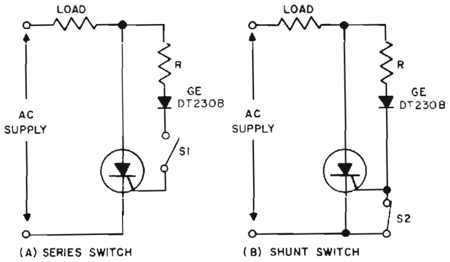
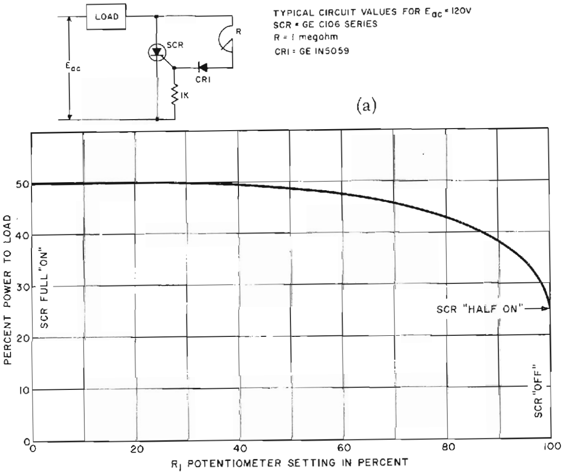


FIGURE 4.20 HALF-WAVE STATIC SWITCH

performance at commercial temperatures. Since in a scheme of this type a resistor will have to supply all of the gate drive required to turn on the SCR, these types of circuits operate most satisfactorily with SCR's having fairly good gate sensitivities. The less sensitive the gate, the lower the resistance must be, and the greater power rating.

A very simple variable resistance half-wave circuit is shown in Figure 4.21. It provides phase retard from essentially zero (SCR full "on") to 90 electrical degrees of the anode voltage wave (SCR half "on"). Diode CR1 blocks reverse gate voltage on the negative half cycle of anode supply voltage. It must be rated to block at least the peak value of the AC supply voltage. The retard angle cannot be



(b) Transfer Function

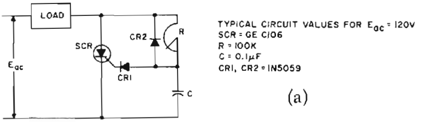
FIGURE 4.21 SIMPLE HALF-WAVE VARIABLE RESISTOR PHASE CONTROL (LIMITED RANGE OF CONTROL)

extended beyond the 90 degree point because the trigger circuit supply voltage and the trigger voltage producing the gate current to fire, I_{GF}, are in phase. When $e_{ac} = E_m$, at the peak of the AC supply voltage, the SCR can still be triggered with the maximum value of resistance between anode and gate. Since the SCR will trigger and latch into conduction the first time I_{GT} is reached, its conduction cannot be delayed beyond 90 electrical degrees with this circuit.

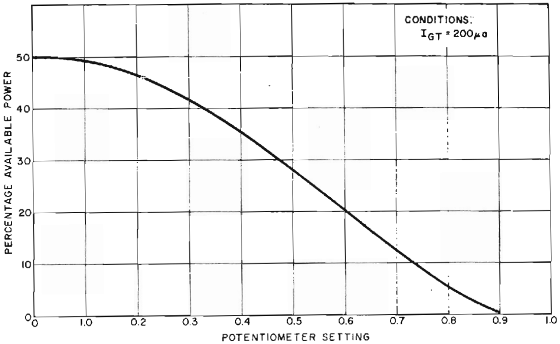
The transfer function of this circuit has also been plotted in the same figure. It assumes that the potentiometer R has been chosen so that the SCR just does not fire at the maximum setting. The transfer function is very non-linear and repeatibility of setting is not possible either with different SCR's or with temperature due to I_{GT} variation.

Figure 4.22 shows an R-C-Diode circuit giving full half-cycle control (180 electrical degrees). On the positive half-cycle of SCR anode voltage the capacitor will charge to the trigger point of the SCR in a time determined by the RC time constant and the rising anode voltage. On the negative half-cycle, the top plate of the capacitor charges to the peak of the negative voltage cycle through diode CR2, thus resetting it for the next charging cycle.

Since triggering current must be supplied by the line voltage through the resistor, the capacitor must be selected such that its charging current is high compared with I_{GT}, at the instant of the latest desired firing angle. Conversely, select the maximum value of R to produce I_{GT} at the latest desired firing angle, using the line voltage



(a)



(b) Transfer Function

FIGURE 4.22 SIMPLE HALF-WAVE RC-DIODE PHASE CONTROL (FULL 180° CONTROL RANGE) AND ITS ASSOCIATED TRANSFER FUNCTION

less IR drop in the load at that point, then select C to produce V_{GT} at that point in time. But similar to all simple RC triggering methods, non-linear output results as the transfer characteristic (Figure 4.22) shows. Again it should be reiterated that since the output depends so heavily on I_{GT}, it will vary with temperature and different devices.

Figure 4.23 illustrates a slave circuit arrangement in which an independent half-wave circuit (SCR_2) is triggered on one half-cycle at a predetermined phase angle. On the following half-cycle the slave circuit will trigger SCR_1 at the same phase angle relative to that half-cycle. When SCR_2 does not trigger, capacitor C will charge and discharge to the same voltage at the same time constant. The voltage across C will not be sufficient to trigger SCR_1. As SCR_2 is triggered, capacitor C on discharging sees a time integral of line voltage that is different from the one on charging by the time integral of voltage appearing across the load. This action resets the capacitor to a voltage level related to the trigger delay angle of SCR_2. On the next half-cycle, when the anode of SCR_1 swings positive, it will trigger at the end of this delay angle.

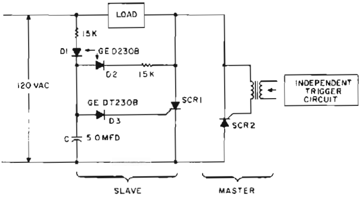


FIGURE 4.23 THREE TERMINAL, FULL WAVE, RC-DIODE SLAVING CIRCUIT FOR FULL-WAVE PHASE CONTROL

4.11 TRIGGERING SCR WITH A NEGATIVE PULSE

Some applications may make it desirable to trigger an SCR with a negative pulse rather than with one of the conventional positive polarity. In low power level SCR circuits a diode connected in series with the SCR allows negative triggering conveniently and economically. Figure 4.24 shows this arrangement for a C103 type SCR.

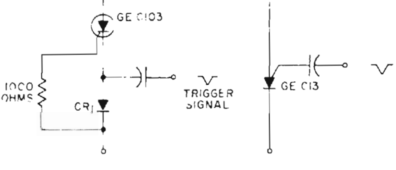


FIGURE 4.24 NEGATIVE PULSE TRIGGERING

A complementary SCR, like the C13, is designed for negative voltage triggering. Therefore, this device should be used in low voltage applications (< 40 V) where negative voltage triggering is a must.

4.12 AC THYRATRON-TYPE PHASE SHIFT TRIGGER CIRCUITS

Figure 4.25 illustrates a full-wave phase controlled rectifier employing an R-C or R-L phase shift network to delay the gate signal with respect to the anode voltage on the SCR's. Many variations of this type of phase shift circuit have been worked out for thyratrons.

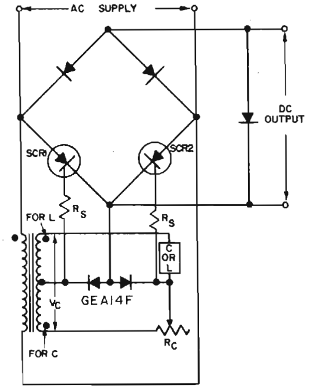


FIGURE 4.25 R-C OR R-L PHASE SHIFT NETWORK CONTROL OF SINGLE PHASE BRIDGE OUTPUT

When using SCR's (C8, C10, C11, C35, C36, and C50 series), the following criteria should be observed to provide the maximum range of phase shift and positive triggering over the particular SCR's temperature range without exceeding the gate voltage and current limitations:

A. The peak value of V_c should be greater than 25 volts.

B. $\frac{1}{2\pi fC}$ or $2\pi fL \leqq \frac{V_c}{2} - 9$

where C = capacitance in farads
L = inductance in henries
V_c = peak end-to-end secondary voltage of control transformer
f = frequency of power system

C. $R_s = \frac{V_c - 20}{0.2}$

where R_s = series resistance in ohms

D. $R_c \geqq \frac{10}{2\pi fC}$ or $10\,(2\pi fL)$

Because of the frequency dependence of this type of phase shift circuit the selection of adequate L or C components becomes easier at higher operating frequencies.

4.13 SATURABLE REACTOR TRIGGER CIRCUITS

Saturable reactors can provide a fairly steep wavefront of gate

current together with a convenient means of control from a low level DC or AC signal. This type of control is adaptable to feedback systems and provides the additional advantage of multiple, electrically-isolated inputs and outputs for more complex circuits.

4.13.1 Continuously Variable Control

A typical half-wave magnetic amplifier type trigger circuit is shown in Figure 4.26. The gate signal for triggering the SCR is obtained from winding 3-4 of transformer T_1. When the core of T_2 is unsaturated, the winding 3-4 of T_2 presents a high impedance to the gate signal so that only a small voltage is developed across R_3. When the core of T_2 saturates, the impedance of winding 3-4 of T_2 decreases by several orders of magnitude so that a large voltage appears at the gate of the SCR, causing it to trigger. Resistor R_2 limits the gate current to the rated value and resistor R_3 limits the gate voltage produced by the magnetizing current of winding 3-4 of T_2 so that the SCR will not trigger before the core of T_2 saturates. Diode CR_2 serves the dual purpose of preventing a reverse voltage on the gate of the SCR and preventing any reverse current through winding 3-4 which would produce an undesired reset of the core T_2.

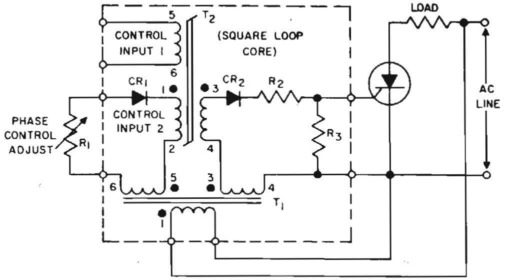


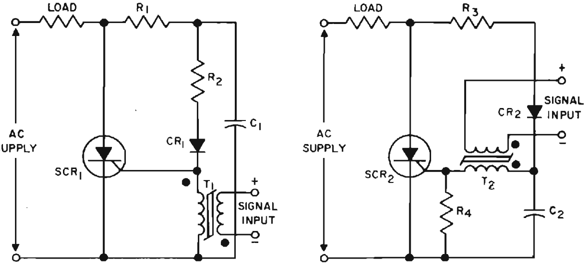
FIGURE 4.26 TYPICAL HALF-WAVE MAGNETIC TRIGGER CIRCUIT

Control signals can be applied to either input 1 or input 2 or both. Input 2 operates in the reset mode by controlling the reset voltage on winding 1-2 of T_2 during the negative half cycle. The setting of the potentiometer R_1 determines the amount of reset of the core during the negative half cycle, which in turn determines the phase angle of the SCR conduction during the positive half cycle. Other control circuits, such as a transistor amplifier stage, can be used in place of R_1. Since power is furnished by winding 5-6 of T_1, no auxiliary power supply is needed. Input 1 operates in the MMF (magnetomotive force) made by controlling the current through the winding 5-6 and the core flux level, which in turn determines the trigger angle. The current for input 1 must be obtained from an external power supply or from a current generating type of transducer.

Additional output windings can be added to T_2 for triggering several SCR's in parallel or in series. Also, additional control windings of the reset or MMF type can be added to T_2. Full wave and multiple phase operation can be achieved by combining two or more half wave circuits.

4.13.2 On-Off Magnetic Trigger Circuits

Magnetic trigger circuits designed for phase control applications such as the one shown in Figure 4.26 require the use of saturable cores which are large enough to allow the output winding to sustain the gate voltage signal for a full half cycle without saturating. For simple on-off control applications, the magnetic trigger circuits shown in Figure 4.27 permit the use of smaller and less expensive cores since the output winding is not required to sustain the gate voltage signal for a full half cycle. In addition, these circuits have the advantage of not requiring the use of an auxiliary supply transformer.



(A) SHUNT CONFIGURATION (B) SERIES CONFIGURATION

FIGURE 4.27 HALF-WAVE ON-OFF MAGNETIC TRIGGER CIRCUITS

In Figure 4.27(a), one winding of saturable transformer T_1 is connected in shunt with the gate of SCR_1. If T_1 is unsaturated, the current through R_1, R_2 and CR_1 will flow into the gate of SCR_1 during the first part of the positive half cycle and cause SCR_1 to turn on. If T_1 is saturated, the current through R_1, R_2 and CR_1 will be diverted from the gate by the low saturated impedance of the winding on T_1. When T_1 is saturated it can be reset, and the SCR can be made to trigger by a positive voltage on the signal input. Capacitor C_1 provides filtering for the gate signal to prevent undesired triggering due to fast transients on the AC supply.

In Figure 4.27(b), one winding of saturable transformer T_2 is connected in series with capacitor C_2 and the gate of SCR_2. If T_2 is unsaturated the current through R_3 and CR_2 will charge C_2 during the initial part of the positive half cycle. T_2 will saturate after a few degrees of the positive half cycle and permit a rapid discharge of C_2 into the gate of SC_2, thus causing SCR_2 to trigger. If T_2 is initially saturated at the beginning of the positive half cycle, the winding of T_2 will divert the current from C_2 and prevent C_2 from being charged. Resistor

R_4 prevents the voltage at the gate of SCR_2 produced by the current through R_3 from exceeding the maximum gate voltage that will not trigger the SCR. When T_2 is saturated, it can be reset and the SCR can be made to trigger by a positive voltage at the signal input.

The circuits of Figure 4.27 permit the SCR to perform the function of an AC contactor with an isolated DC control winding. Modifications of these circuits permit full wave operation with normally open, normally closed or latching operation. The reader is referred to Chapter 8 for further discussion of static switching circuits.

4.14 SEMICONDUCTOR TRIGGER-PULSE GENERATORS

The simple resistor and capacitor triggering circuits described in Sections 4.12 and 4.13 depend heavily on the specific triggering characteristic of each SCR used. In addition, the power level in the control circuit is high because the entire triggering current must flow through the resistance. Furthermore, they do not readily lend themselves to automatic, self-programmed, or feedback control systems.

Pulse triggering, on the other hand, can accommodate wide tolerances in triggering characteristics by overdriving the gate. The power level in pulse control circuits may also be quite low since the required triggering energy (I_{GT} V_{GT} t) can be stored slowly, then discharged rapidly at the desired instant of triggering. The use of pulse triggering enables small, low power, signal-type components and transducers to control large, high-current thyristors, as shown in later chapters.

While there are a multitude of semiconductors and circuits which can produce adequate triggering pulses, this chapter will consider only those most adept at performing this function.

4.14.1 Basic Relaxation Oscillation Criteria

Most devices used to produce trigger pulses (such as: the unijunction transistor, diac trigger diode, the silicon unilateral and bilateral switches, programmable unijunction transistors, neon lamps, etc.) operate by discharging a capacitor into the thyristor gate. They function in a basic relaxation oscillator circuit by means of a negative resistance characteristic. Specifications for these devices usually include the voltage and current required to achieve negative resistance when approached from either the conducting or non-conducting states. (See also Section 4.1.)

To relate these specifications to the criteria for oscillation, consider the elementary relaxation oscillator circuit of Figure 4.28(a) using a trigger device with voltage to switch V_S, current to switch I_S, holding voltage V_H, and holding current I_H. The device characteristic curve is plotted in Figure 4.28(b), along with load lines representing R_1 and R_2. If R_1 is increased to the maximum value which will sustain oscillations, we will find that its load line intersects the device curve at a point (1) where the negative resistance slope of the device curve is equal to the load line for R_2. This point (1) is very close to I_S and V_S, but not quite the same since the specification of these values is made at the point where the slope of the curve is vertical, representing zero dynamic resistance.

When the triggering point (1) is reached, the operating point transfers to point (2), discharging the capacitor with a peak pulse current, i_p, and producing a peak pulse voltage e_p, across the load resistor R_2 (which includes the thyristor gate impedance). The discharge of the capacitor follows the device curve from point (2) to point (3), where the negative resistance slope is once again tangential with the R_2 load line. The operation then transfers from point (3) to point (4), the capacitor re-charges through R_1 and the oscillation continues.

If R_1 is changed to the minimum value which will sustain oscillation, its new load line will intersect the device curve at point (3). Any smaller value will cause the device to remain conducting at some stable

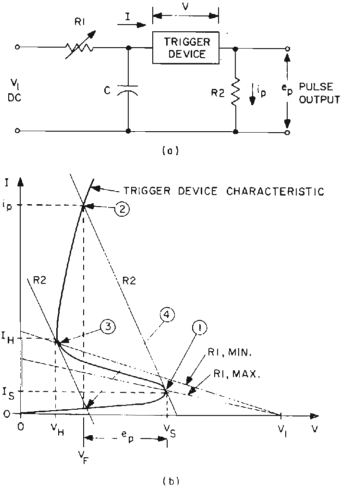


FIGURE 4.28 BASIC RELAXATION OSCILLATOR CIRCUIT AND CHARACTERISTICS

operating point between (2) and (3). Increasing R_1 beyond the maximum oscillating value causes operation to cease at some point between (1) and the origin.

A very important factor not apparent in Figure 4.28, and often not specified for a device, is switching time, or rise time. A device which slowly switches from point (1) to point (2) will never get there since it is discharging the capacitor as it goes and will reach the device curve somewhere between points (2) and (3). This switching time can be a limiting factor if it is a significant fraction of the discharge time-constant, R_2C.

The magnitude of pulse voltage, e_p, and pulse current, i_p, appearing at the load, resistor R_2 in this circuit, is dependent upon the characteristic curve of the device and the relation between its switching

time and the discharge time-constant, R_2C. For values of R_2C large ($>$ 10X) in comparison with the switching time of the device, the peak pulse voltage, e_p, is simply the difference between the switching voltage V_S and the conduction voltage drop V_F. The peak pulse current under this condition is found from the intersection of the R_2 load line and the characteristic curve.

When R_2C is smaller, approaching the switching time, both e_p and i_p are reduced by the effective device resistance during switching. As was shown in Section 4.8, reducing peak current, and extending the pulse time accordingly, decreases the probability of triggering a thyristor.

Since the effect of switching time is not readily apparent from the characteristic curve, devices intended for thyristor triggering generally specify the peak pulse voltage across R_2 (where the value of R_2 is chosen to represent typical gate impedance) when discharging a given size capacitor typical for its application.

The following table shows the correlation of the parameter terminologies used in various switching devices with the points on the general characteristic curve:

TABLE 4.1

Terminology On Figure 4.28	Unilateral Devices			Bilateral Devices			
	UJT	SUS	PUT	SBS	ST4	Diac	Neon
V_S	V_P	V_S	V_P*	V_S	V_S	$V_{(BR)}$	V_f
I_S	I_P	I_S	I_P*	I_S	I_S	$I_{(BR)}$	
V_H	V_V	V_H	V_V*	V_H			V_e
I_H	I_V	I_H	I_V*	I_H			
e_p	V_{OB1}	V_O	e_p	V_O	V_O	e_p	
i_p							i_p

*Determined Externally by Circuit

4.14.2 Unijunction Transistor

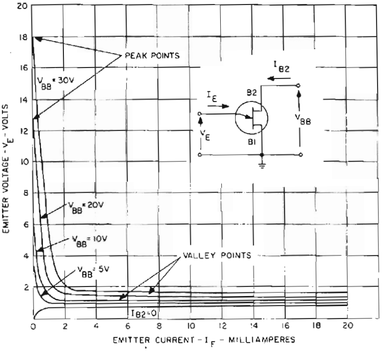


FIGURE 4.29 GE 2N2646 UNIJUNCTION TRANSISTOR SYMBOL AND EMITTER INPUT CHARACTERISTICS

The UJT has three terminals which are called the emitter (E), base-one (B_1), and base-two (B_2). Between B_1 and B_2 the unijunction has the characteristics of an ordinary resistance. This resistance is the interbase resistance (R_{BB}) and at 25°C has values in the range from 4.7K to 9.1K.

The normal biasing conditions for a typical UJT are indicated in Figure 4.29. If the emitter voltage, V_E, is less than the emitter peak point voltage, V_P, the emitter will be reverse biased and only a small reverse leakage current, I_{EO}, will flow. When V_E is equal to V_P and the emitter current, I_E, is greater than the peak point current, I_P, the UJT will turn on. In the on condition, the resistance between the emitter and base-one is very low and the emitter current will be limited primarily by the series resistance of the emitter to base-one external circuit.

The peak point voltage of the UJT varies in proportion to the interbase voltage, V_{BB}, according to the equation:

$$V_P = \eta V_{BB} + V_D \tag{4.1}$$

The parameter η is called the intrinsic standoff ratio. The value of η lies between 0.51 and 0.82, and the voltage V_D, the equivalent emitter diode voltage, is in the order of .5 volt at 25°C, depending on the particular type of UJT. It is found that V_P decreases with temperature, the temperature coefficient being about −3mv/°C for the 2N2646-47 (−2mv/°C for 2N489 series). The variation of the peak point voltage with temperature may be ascribed to the change in V_D (also η for 2N2646-47 series). It is possible to compensate for this temperature change by making use of the positive temperature coefficient of R_{BB}. If a resistor R_{B2} is used in series with base-two as shown in Figure 4.30, the temperature variation of R_{BB} will cause V_{BB} to increase with temperature. If R_{B2} is chosen correctly, this increase in V_{BB} will compensate for the decrease in V_P in Equation 4.1. Over a temperature range of −40°C to 100°C, Equation 4.3(a) gives an approximate value of R_{B2} for the majority of 2N2646 and 2N2647 UJT's. Equation 4.3(b) gives R_{B2} for the 2N489 MIL series, 2N1671A and B, and the 2N2160.

$$R_{B2} \approx \frac{10000}{\eta V_1} \tag{4.3a}$$

$$R_{B2} \approx \frac{0.40R_{BB}}{\eta V_1} + \frac{(1-\eta)R_{B1}}{\eta} \tag{4.3b}$$

For a more detailed discussion of the characteristics of the various types of UJT's the reader is referred to Reference 8. Quantitative data and techniques for temperature compensation on an individual and general basis in very high performance circuits over extreme temperature ranges are discussed in Reference 9.

4.14.2.1 Basic UJT Pulse Trigger Circuit

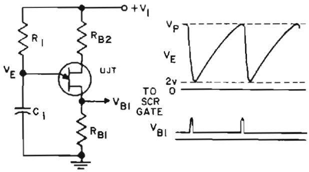


FIGURE 4.30 BASIC UNIJUNCTION TRANSISTOR RELAXATION OSCILLATOR-TRIGGER CIRCUIT WITH TYPICAL WAVEFORMS

The basic UJT trigger circuit used in applications with the SCR is the simple relaxation oscillator shown in Figure 4.30. In this circuit, the capacitor C_1 is charged through R_1 until the emitter voltage reaches V_P, at which time the UJT turns on and discharges C_1 through R_{B1}. When the emitter voltage reaches a value of about 2 volts, the emitter ceases to conduct, the UJT turns off and the cycle is repeated. The period of oscillation, T, is fairly independent of the supply voltage and temperature, and is given by:

$$T = \frac{1}{f} \approx R_1 C_1 \ln \frac{1}{1-\eta} = 2.3\, R_1 C_1 \log_{10} \frac{1}{1-\eta} \qquad (4.4)$$

For an approximate nominal value of intrinsic standoff ratio of $\eta = 0.63$, $T = R_1 C_1$.

The design conditions of the UJT triggering circuit are very broad. In general, R_{B1} is limited to a value below 100 ohms although values up to 2 or 3K are possible in some applications. The resistor R_1 is limited to a value between 3K and 3 Meg. The lower limit on R_1 is set by the requirement that the load line formed by R_1 and V_1 intersect the emitter characteristic curve of Figure 4.29 to the left of the valley point, otherwise the UJT in Figure 4.30 will not turn off. The upper limit on R_1 is set by the requirement that the current flowing into the emitter at the peak point must be greater than I_P for the UJT to turn on. The recommended range of supply voltage V_1 is from 10 volts to 35 volts. This range is determined on the low end by the acceptable values of signal amplitude and at the high end by the allowable power dissipation of the UJT.

If the pulse output (V_{B1}) of the circuit of Figure 4.30 is coupled directly, or through series resistors, to the gates of the SCR's, the value of R_{B1} should be low enough to prevent the DC voltage at the gate due to interbase current from exceeding the maximum voltage that will not trigger the SCR's (see Figure 4.13) V_{GT} (max) at the maximum junction temperature at which the SCR's are expected to operate. To meet this criterion, R_{B1} should be chosen in accordance with the following inequality:

$$\frac{R_{B1} V_1}{R_{BB}(\text{min}) + R_{B1} + R_{B2}} < V_{GT(\text{max})} \qquad (4.5)$$

For the C35 (2N681) types at a maximum junction temperature of 125°C, V_{GT} (max) is 0.25 volt, hence for a supply voltage of 35 volts or less, R_{B1} should be 50 ohms or less. If the pulse output from the UJT triggering circuit is coupled to the gates of the SCR's by means of transformers or capacitors, these limitations do not apply.

4.14.2.2 Designing the Unijunction Transistor Trigger Circuit

The type 2N2646 and 2N2647 UJT's are specifically characterized for SCR trigger circuits and are factory tested to ensure reliable operation with all types of G-E SCR's over their respective temperature ranges. Their condensed specifications are given in Chapter 22.

The design of a suitable UJT trigger circuit can be achieved rapidly and easily by using the design curves given in Figures 4.31(a) and 4.31(b) for the 2N2646 and 2N2647, respectively. These curves give the minimum supply voltage V_1 required to guarantee triggering of various types of SCR's over the indicated temperature range as a function of the UJT emitter capacitor C_1 and the base-one coupling resistor R_{B1} or base-one coupling transformer. The value of resistor R_1 is not important for the purposes of the design provided that it is within the limits required for the UJT to oscillate. If R_{B2} is significantly greater than 100 ohms the minimum supply voltage which is required V_1' should be calculated from the minimum supply voltage V_1 given by Figures 4.31(a) and 4.31(b) using the equation:

$$V_1' = \frac{(2200 + R_{B2})\,V_1}{2300} \tag{4.6}$$

It is recommended in all cases that a resistance of 100 ohms or greater be used in series with either base-two or in series with the power supply to protect the UJT from possible thermal runaway. This is particularly important when operating at high ambient temperatures, at high supply voltages, or with large values of emitter capacitance.

As an example of the use of Figure 4.31 in the practical design of an SCR trigger circuit, consider the following problem:

Example: A circuit is required to trigger a C11 type (2N1773 series) SCR at the lowest possible supply voltage with a 2N2646 UJT and pulse transformer coupling. The value of capacitance, chosen on the basis of operating frequency, is 0.1 μf, and temperature compensation is desired. Assume $\eta = 0.66$ for a nominal value.

Solution: From the chart in Figure 4.31(a) it can be seen that Curve I should be considered and that the supply voltage V_1 should not exceed $V_{1(max)} = 35$V. On Curve I the minimum supply voltage for a value of $C_1 = 0.1\ \mu$f is about $V_1 = 12$ volts. The value for R_{B2} is determined from Equation 4.3(a) as

$$R_{B2} \approx \frac{10000}{(.66)\,(12)} = 1260 \approx 1000 \text{ ohms (nearest standard}$$

value). With this value of R_{B2} the supply voltage must be increased to a value V_1' in accordance with Equation 4.6

from which $V_1' = \frac{2300}{(2200 + 1000)}$ (12) $\approx$ 17 volts. Thus, a suitable design for this example would be $C_1 = 0.1\ \mu f$, $R_{B2} = 1$ K ohms, and $V_1' = 17$ volts.

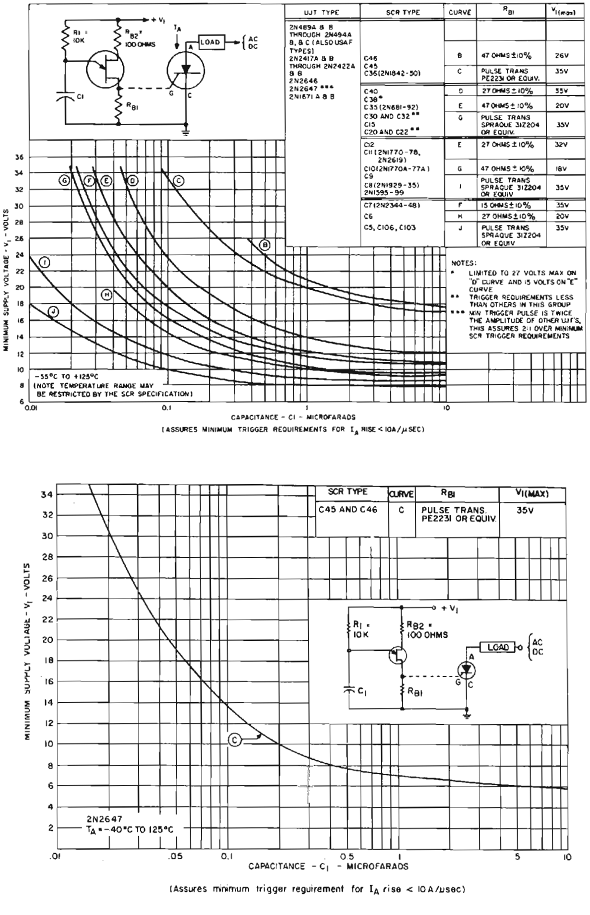


FIGURE 4.31 UJT TRIGGER CIRCUIT DESIGN CURVES

If, in the case of the 2N2646 and 2N2647 UJT's, R_{B2}, as determined from Equation 4.3(a) causes V_1' (from Equation 4.6) to be larger than can be attained practically or economically, the use of the 2N489 series, the 2N1671A or the 2N1671B is suggested. [Equation 4.3(b) yields a lower value of R_{B2}] alternatively, if extreme temperature compensation is not required, or if the temperature range to which the 2N2646/47 UJT's are subjected is not great, a value of $R_{B2} \geqq 100$ ohms may be used.

It is not recommended that a UJT be used to trigger an SCR larger than a C45 type. A PUT trigger circuit (Section 4.14.3) can be used or else a pulse amplifier must boost the UJT output into the gate.

4.14.3 Programmable Unijunction Transistor (PUT)

The PUT trigger device is a small thyristor with an anode gate as shown in Figure 4.32. If the gate is maintained at a constant potential, the device will remain in its off state until the anode voltage exceeds the gate voltage by one diode forward voltage drop. At this voltage the peak point is achieved and the device turns on. In the relaxation oscillator shown in the same figure, the gate voltage of the PUT is maintained from the supply voltage by the resistor divider, R_1 and R_2. This voltage determines the peak point voltage, V_p. The peak point current, I_p and the valley point current, I_v, both depend upon the equivalent impedance on the gate, $R_1 R_2/(R_1 + R_2)$, and the source voltage, E_S. R_T and C_T controls the frequency along with R_1 and R_2 since the period of oscillation is approximately:

$$t \approx R_T C_T \ln\left(\frac{E_s}{E_s - V_p}\right) \tag{4.7}$$

$$t \approx R_T C_T \ln\left(1 + \frac{R_2}{R_1}\right) \tag{4.8}$$

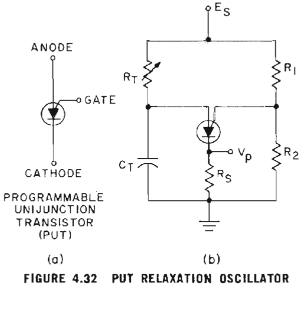


FIGURE 4.32 PUT RELAXATION OSCILLATOR

The primary difference between the two available PUT's (2N6027 and 2N6028) is in the peak point current. The 2N6028 is specifically characterized for long interval timers and other applications requiring low leakage and low peak point current. The 2N6027 has been char-

acterized for general use where the low peak point current of the 2N6028 is not essential. Applications of the 2N6027 include timers, high gain phase control circuits and relaxation oscillators. The other important asset of the PUT, which makes them particularly suitable for triggering high current SCR's is its high peak pulse current output. Due to the PNPN nature of this device (as opposed to conductivity modulation), the forward conductance is high and the rise time is fast. The dynamic resistance of the PUT in the saturation region is approximately 3 ohms. Rate of rise of V_o is typically 10 nsec (a maximum of 80 nsec is specified). Healthy output pulses are available from capacitors as low as .01 μfd. References 14 and 15 have more details on device operation and trigger circuit design using this particular device.

4.14.3.1 Designing the PUT Relaxation Oscillator and Timer Circuits

A systematic approach to the design of a PUT oscillator circuit appears complex precisely because it is such a versatile device. A further complication arises because so much performance variation can be programmed into the circuit by the voltage divider R_1 and R_2.

Consider the following key guide posts:

1. Peak Point Control, $I_p - I_p$ need only be considered in the case of a very long interval timer. Both R_T and C_T are large, the latter having low equivalent parallel resistance.
2. Valley Current, I_v – this is a key parameter in free running relaxation oscillators operating from a DC supply. Most trigger circuits derive their supply voltage from the "off-state" SCR. When the PUT triggers this SCR, its supply voltage collapses and it commutates off.
3. Offset Voltage, V_T – the minimum value of R_1 is determined by V_T and so V_T only plays a role in long interval timers.

Design Problem: A free running relaxation oscillator is wanted, which is capable of triggering a C20 flasher from a 12 V supply. The operating frequency must be adjustable from 5 to 50 pulses per minute.

Solution: Refer to Figure 4.32 for the basic circuit. No problem is anticipated with I_p since the frequencies are relatively high, but I_v may be troublesome.

The selection of C_T is crucial since too small a value will not fire the SCR and too large a value leads straight to I_v problems.

One may determine the value of V_p and C_T to trigger the C20 from Figure 4.17.

The time integral of current pulse to be used and the time integral of the trigger current pulses required by Figure 4.33 are plotted on the same graph. These curves represent the charge to be delivered to the gate and the charge required to trigger as a function of time. If the charge delivered exceeds the charge required, at any time, the device turns on. This technique is demonstrated in this figure for the C20 SCR and a decaying exponent current pulse with a peak of 80 ma and an R-C constant of 8 μseconds. Since the two curves intersect at 3.6 μseconds after the start of the pulse, the device will turn on. If no intersection had occurred, then either the peak current or the capacitor value could have been increased.

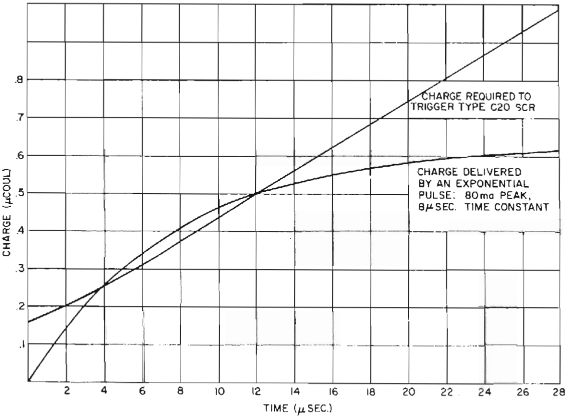


FIGURE 4.33 CHARGE TO TRIGGER AN EXPONENTIAL PULSE

The above technique provides a useful indication of SCR pulse triggering requirements. However, it is important that a reasonable safety factor be incorporated in the trigger circuit design, since there are sizable variations in this characteristic.

Let $R_s = 39$ ohms. Then since $R_s C_T = 8$ μseconds, $C_T \approx 0.2$ μf. The peak triggering current of 80 ma determines V_p, namely:

$$V_p = I_p \cdot R_s + 1\text{ V}$$
$$= (80\text{ ma})(39\,\Omega) + 1\text{ V} = 4.1$$

where 1 V is the approximate PUT on-state voltage

The computed value of η is:

$$\eta = \frac{V_p}{E_s} = \frac{4.1}{12} \approx 1/3$$

The timing pot R_T can be found from Formula 4.7.

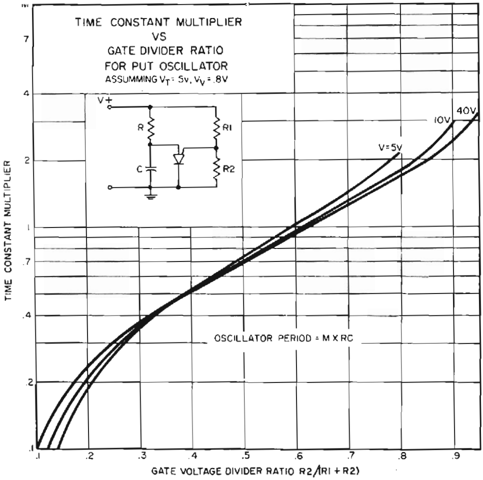
$$R_{T(max)} = \frac{1}{C_T \ln\left(\frac{1}{12 - 4.1}\right) f_{min}} = 2.5\text{ Meg}$$

$$R_{T(min)} = \frac{1}{C_T \ln\left(\frac{12}{12 - 4.1}\right) f_{max}} = 250\text{ K}$$

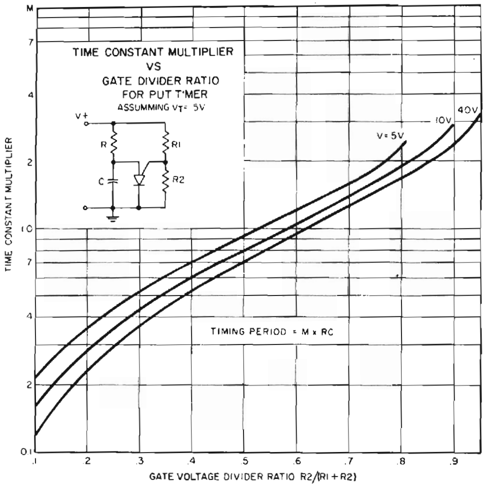
The maximum valley current occurs at the maximum frequency when R_T is a minimum:

$$I_{v(max)} \approx \frac{E_s}{R_{T(min)}} \approx \frac{12}{250}\text{ ma} \approx 48\ \mu\text{a}$$

$I_{v(min)}$ of the 2N6027 is 70μa for $R_G = 10$ K. Therefore, to find R_1 and R_2, the following two simultaneous equations must be solved:



(a)



(b)

FIGURE 4.34 EFFECT OF $R_2/(R_1 + R_2)$ ON OSCILLATOR FREQUENCY

$$R_G = \frac{R_1 R_2}{R_1 + R_2}$$

$$\frac{R_2}{R_1 + R_2} = \frac{V_p}{E_s} = \eta$$

The solutions for R_1 and R_2 are:

$$R_1 = \frac{R_G}{\eta} \qquad R_2 = \frac{R_G}{1 - \eta} \tag{4.9}$$

Since $\eta = 1/3$, then $R_1 = 30$ K and $R_2 = 15$ K.

If other frequency ranges had been desired, either different capacitors could have been switched in for C_T or else R_2 could have been varied to achieve the same result.

Figure 4.34 shows the effect of the voltage divider ratio $R_2/(R_1 + R_2)$ on the period of oscillation.

4.14.4 Silicon Unilateral Switch (SUS)[12]

The SUS, such as the type 2N4987, is essentially a miniature SCR having an anode gate (instead of the usual cathode gate) and a built-in low-voltage avalanche diode between the gate and cathode. The symbol for the SUS and its equivalent circuit are shown in Figure 4.35. Its anode-to-cathode electrical characteristic is shown in Figure 4.36 for no external connection to the gate terminal.

The SUS is usually used in the basic relaxation oscillator circuit shown in Figure 4.28(a) and its characteristics follow the same criteria for oscillation. The type 2N4987 has the following specifications:

Switching Voltage, V_S	6 to 10 volts
Switching Current, I_S	0.5 ma, maximum
Holding Voltage, V_H	Not specified ($\approx$ 0.7 V at 25°C)
Holding Current, I_H	1.5 ma, maximum
Forward Voltage, V_F (at I_F = 175 ma)	1.5 volts
Reverse Voltage Rating, V_R	30 volts
Peak Pulse Voltage, V_O	3.5 volts minimum

The Peak Pulse Voltage, V_O, specification is very important for thyristor triggering applications since it is the only realistic figure-of-merit that indicates the ability of the triggering device to transfer charge from the capacitor to the thyristor gate. This voltage is measured with the SUS operating in the circuit of Figure 4.28(a), where $V_1 = 15$ volts, $R_1 = 10$ K ohms, $C = 0.1\ \mu f$, and $R_2 = 20$ ohms. The peak pulse voltage is measured across resistor R_2. The magnitude of the pulse voltage depends both upon the difference between V_S and V_F and upon switching time, as explained in Section 4.14.1. The component values used in the pulse test are adequate for triggering most thyristors.

The major difference in function between the SUS and the UJT is that the SUS switches at a fixed voltage, determined by its internal avalanche diode, rather than a fraction (η) of another voltage. It should also be noted that I_S is much higher in the SUS than in the UJT, and

is also very close to I_H. These factors restrict the upper and lower limits of frequency or time-delay which are practical with the SUS.

For synchronization, lock-out, or forced switching, bias or pulse signals may be applied to the gate terminal of the SUS. For these purposes, treat the SUS as an N-gate SCR.

4.14.5 Silicon Bilateral Switch (SBS)[12]

The SBS, such as the type 2N4991, is essentially two identical SUS structures arranged in inverse-parallel, as shown in Figures 4.37 and 4.38. Since its operates as a switch with both polarities of applied volttage, it is particularly useful for triggering the bidirectional triode thyristors (triacs) with alternate positive and negative gate pulses. This operation is obtained by using an alternating voltage supply for V_1 of Figure 4.28, rather than the DC supply shown.

Specifications for the SBS type 2N4991 are identical to those of the SUS type 2N4987 with the exception of reverse voltage rating, which is not applicable to the SBS.

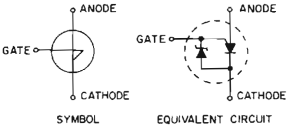


FIGURE 4.35
THE SILICON UNILATERAL SWITCH (SUS)

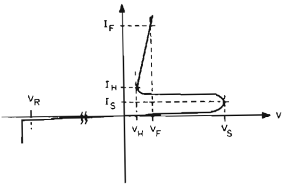


FIGURE 4.36
SUS CHARACTERISTIC CURVE

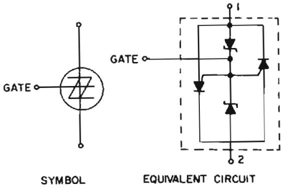


FIGURE 4.37
THE SILICON BILATERAL SWITCH (SBS)

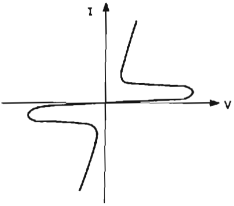


FIGURE 4.38
SBS CHARACTERISTIC CURVE

4.14.6 Bilateral Trigger Diode (Diac)

The diac, such as the type ST2 is essentially a transistor structure, Figure 4.39, which exhibits a negative resistance characteristic above a given switching current $I_{(BR)}$. The characteristic curve of Figure 4.40 shows that this negative resistance region extends over the full operating range of currents above $I_{(BR)}$ hence the concept of a holding current I_H does not apply.

The diac is used in the simple relaxation oscillator circuit of Figure 4.28, and the criteria for oscillation are the same. For alternating pulse output, the supply voltage for the oscillator circuit, V_1, may be an alternating voltage.

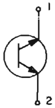


FIGURE 4.39 SYMBOL OF BILATERAL TRIGGER DIODE (DIAC)

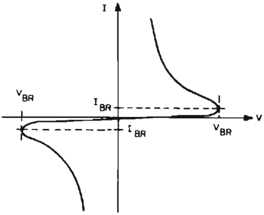


FIGURE 4.40 DIAC CHARACTERISTIC CURVE

The type ST2 diac has the following specifications:

$V_{(BR)}$ .... 28 to 36 volts
$I_{(BR)}$ .... 200 μamp (maximum)
e_p .... 3 volts (minimum)

The peak pulse voltage, e_p, is measured under the same conditions used with the SUS and SBS, namely: $R_2 = 20$ ohms; $C = 0.1$ microfarad. Since the ST2 is primarily used to trigger triacs, this minimum value of e_p has been established to ensure proper triggering of all G-E triacs, assuming, of course, the proper conditions of supply voltage and load impedance in the power circuit of the triac.

4.14.7 Asymmetrical AC Trigger Switch (ST4)

The ST4 is an integrated triac trigger circuit that provides wide range, hysteresis-free, phase control of voltage. This performance is possible with a minimum number of circuit components and at very low cost (see Chapter 7 for circuit details).

The equivalent circuit of Figure 4.41 reveals that the ST4 behaves like a zener diode in series with an SBS. The zener diode provides the asymmetry since now switching voltage V_{S1} has been increased by the avalanche voltage of the zener.

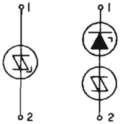


FIGURE 4.41 SYMBOL OF ASYMMETRICAL AC TRIGGER SWITCH (ST4) AND EQUIVALENT CIRCUIT

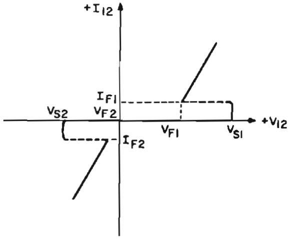


FIGURE 4.42 ST4 CHARACTERISTIC CURVE

The ST4 has the following specifications:

Switching Voltage:	V_{S1}	14-18 volts
	V_{S2}	7-9 volts
Switching Current:	I_{S1}, I_{S2}	80 μa (25°C)
	I_{S1}, I_{S2}	160 μa (−55°C)
On-State Voltages:	V_{F1}	7-10 volts
	V_{F2}	1.6 volts (max)
Peak Pulse Voltage,	V_O	3.5 volts minimum

4.14.8 Other Trigger Devices

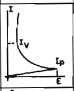
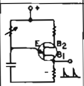
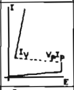
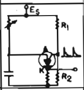
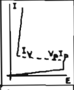
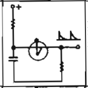
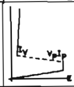
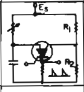
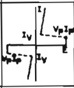
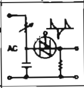
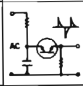
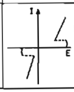
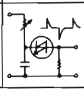
Several other unilateral and bilateral switching devices exist, having characteristics similar to those discussed above. In general, all operate as relaxation oscillators and are subject to the same criteria for oscillation. If the peak pulse voltage (or current) output is not specified, then the maximum switching time must be known. Otherwise, the trigger circuit must be over-designed by a factor depending upon the uncertainty of the unknowns.

Where a large demand exists for the same type triggering source, specialized integrated circuits could be and have been designed to meet the need. The GEL300 is a monolithic integrated triggering circuit that features "zero-voltage" switching to minimize RFI. Its operation and use is covered in Chapter 11. Similarly the GEL301 IC is used in phase control circuits (see Chapter 9).

Another method of triggering that is coming into its own employs light sensitive or light activated devices. This method offers speed along with incomparable electrical isolation. The reader is referred to Chapter 14 and Reference 16 for additional information.

4.14.9 Summary of Semiconductor Trigger Devices

The table below summarizes the electrical characteristics of the widely used triggering devices.

	CLASS	E-I CHARACTERISTICS	BASIC CIRCUIT	MAJOR TYPES	V_p PEAK POINT VOLTAGE	I_p (max) PEAK POINT CURRENT	I_v (min) VALLEY CURRENT	TON TURN ON TIME	SPECIFICATION NUMBER
Unidirectional	UJT Unijunction Transistor			TO-5 / TO-18 2N489A / 2N2417A 2N489B / 2N2417B 2N1671A / 5G515 2N1671B / 5G516 2N1671C 2N2646 2N2647	Fixed Fraction of Interbase Voltage	12 μa 6 μa 25 μa 6 μa 2 μa 5 μa 2 μa	8 ma 8 ma 8 ma 8 ma 8 ma 4 ma 8 ma	1-2 μsec Typ	60.10 60.10 60.50 60.50 60.50 60.62 60.62
	PUT Programable Unijunction Transistor			2N6027 2N6028	$\frac{R_2E_s}{R_1+R_2}$	As low as 2 μa As low as .15 μa (A function of R_1, R_2)	70 μa 25 μa (A function of R_1, R_2)	80 nsec Max	60.20
	SUS Silicon Unilateral Switch			TO-18 / TO-98 2N4983 / 2N4987 2N4984 / 2N4988 2N4985 / 2N4989 2N4986 / 2N4990	6-10 v 7.5-9 v 7.5-8.2 v 7-9 v	500 μa 150 μa 300 μa 200 μa	1.5 ma .5 ma 1.0 ma .75 ma	1.0 μsec Max	65.25, 65.26 65.27, 65.28 65.27, 65.28 65.25, 65.26
	SCS Silicon Control Switch			3N84	$\frac{R_2E_s}{R_1+R_2}$ (40v max)	A function of R_1 and R_2	10 ma Max (A function of R_1 and R_2)	1.5 μsec Max	65.18
Bidirectional	SBS Silicon Bilateral Switch			TO-18 / TO-98 2N4993 / 2N4991 2N4992	6-10 v 7.5-9 v	500 μa 120 μa	1.6 ma .6 ma	1.0 μsec Max	65.30, 65.31 65.32
	DIAC			ST2	28 v-36 v	200 μa	Very high	1 μsec Typ	176.30
	ATS Assymetrical AC Trigger Switch (ST4)			ST4	14-18V 7-9 V	80 μa 80 μa		1 μsec	175.32

Note: Common terminology used for comparison purposes. For actual terminology, see device specification sheets.

TABLE 4.2

4.15 NEON GLOW LAMPS AS TRIGGER DEVICES

The low price of neon glow lamps has led many to consider their use for triggering thyristors. The characteristics of the glow lamp are quite similar, but for magnitude, to those of the diac. The switching voltage is generally on the order of 90 volts and the switching current is extremely small (below 1 μa). However, the switching time is large in comparison with semiconductor devices, and the peak pulse voltage is usually not specified.

The G-E type 5AH is an isotope-stabilized neon glow lamp now being used in many low-cost SCR control circuits. The 5AH lamp has the following specifications:

V_S	60 to 100 volts
I_S	Not specified
V_F	Approx. 60 volts at 5 ma
V_H	Not specified
I_H	Not specified
i_p	25 ma (minimum)

The peak pulse current, i_p, is measured in a 20 ohm resistor when discharging a 0.1 μf capacitor. The minimum peak pulse voltage is, therefore, 0.5 volts under this condition. The specification also includes an indication of the operating life of the lamp: 5000 hours operation, on the average, at 5 ma DC results in a 5 volt change in V_S or V_F. This has not been correlated to hours operation in a relaxation oscillator at 120 Hz.

Glow lamps are useful for thyristor triggering under the following conditions:

(a) Thyristor I_{GT} on the order of 10 ma or less
(b) Wide tolerance in V_S is acceptable
(c) Minimum pulse voltage measured in sample lot several times minimum required to trigger the thyristor
(d) Change in V_S and pulse output with operating time is acceptable
(e) Cost of primary importance
(f) 5% loss in RMS voltage at full power tolerable

4.15.1 Neon Lamp Trigger Circuits

Neon lamp SCR phase-controlled trigger circuits have the promise of combining the low cost of the RC diode circuit with improved performance. In addition, the possibility exists in such a relatively simple yet high impedance circuit to exercise control over the charging rate of the trigger capacitor with suitable devices responsive to light, heat, pressure, etc.

Figure 4.43 shows a half wave AC phase-controlled circuit using a 5AH as the trigger for a two terminal system. The 5AH will trigger when the voltage across the two 0.1 MFD capacitors reaches the breakdown voltage of the lamp. Control can be obtained full off to 95% of the half wave RMS output voltage. Full power can be obtained with the addition of the switch across the SCR.

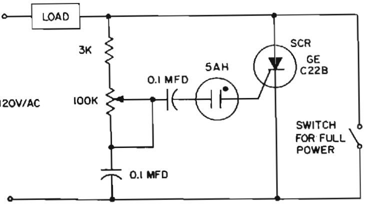


FIGURE 4.43 HALF WAVE/TWO TERMINAL

Figure 4.44 is a transformer coupled full-wave AC phase-controlled circuit using a 5AH as the trigger for a two terminal system. The 5AH will perform the same as in the half-wave circuit but the pulse transformer will allow the SCR's to alternate in firing. The resistor R and the pulse transformer should be chosen to give proper shape of the pulse to the gate of the SCR. Some loss of load voltage will occur but will amount to only about 5% in terms of total RMS output voltage.

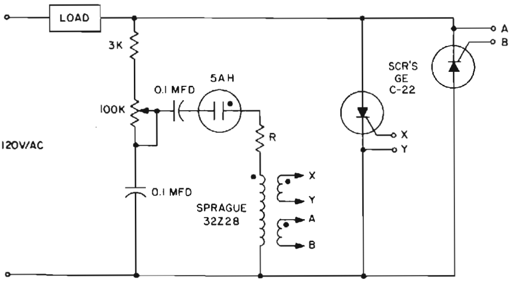


FIGURE 4.44 FULL WAVE TRANSFORMER COUPLED/TWO TERMINAL

4.16 PULSE TRANSFORMERS

Pulse transformer are often used to couple a trigger-pulse generator to a thyristor in order to obtain electrical isolation between the two circuits. There are many vendors of pulse transformers suitable for this purpose. Although several specific model numbers are shown on circuit diagrams in this manual, it is not our purpose nor intent to serve as a testing or approval function.

The transformers usually used for thyristor control are either 1:1, two-winding, or 1:1:1 three-winding types. As shown in Figure 4.45, the transformer may be connected directly between gate and cathode, or may have a series resistor R to either reduce the SCR holding current or to balance gate currents in a three-winding transformer connected to two SCR's, or may have a series diode D to prevent reverse gate current in the case of ringing or reversal of the pulse transformer output voltage. The diode also reduces holding current of the SCR. In some cases where high noise levels are present, it may be necessary to load the secondary of the transformer with a resistor to prevent false triggering.

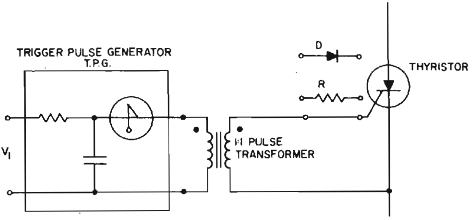


FIGURE 4.45 BASIC PULSE TRANSFORMER COUPLING

Figure 4.46 shows several ways of using a transformer to drive an inverse-parallel pair of SCR's. Full isolation is provided by the three-

winding transformer in Figure 4.46(a). Where such isolation is not required, a two-winding transformer may be used either in a series mode, Figure 4.46(b), or a parallel mode, Figure 4.46(c). In any case, the pulse generator must supply enough energy to trigger both SCR's, and the pulse transformer (plus any additional balancing resistors) must supply sufficient gate current to both SCR's under worst-case conditions of unbalanced gate impedances.

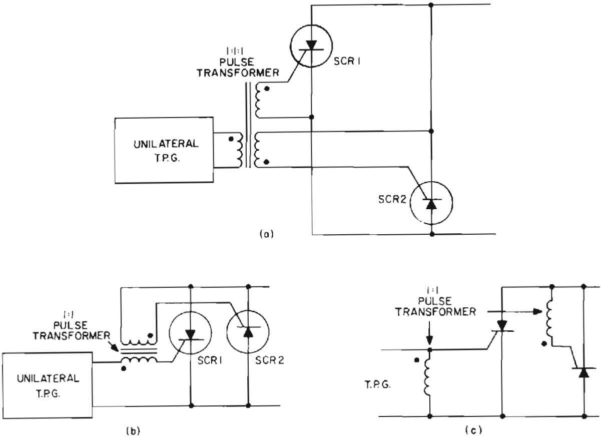


FIGURE 4.46 PULSE TRANSFORMER CONNECTIONS FOR TWO SCR'S

The prime requirement of a trigger pulse transformer is one of efficiency. The simplest test is to use the desired trigger pulse generator to drive a 20 ohm resistor alone and then drive the same resistor through the pulse transformer. If the pulse waveforms across the resistor are the same under both conditions, the transformer is perfect. Some loss is to be expected, however, and must be compensated by increased drive from the generator.

Some of the transformer design factors to be considered are:

(a) Primary magnetizing inductance should be high enough so that magnetizing current is low, in comparison with pulse current, during the pulse time.

(b) Since most pulse generators are unilateral, core saturation must be avoided.

(c) Coupling between primary and secondary should be tight, for single-SCR control, or may have specified leakage reactance to assist in balancing currents for multiple-SCR control.

(d) Insulation between windings must be adequate for the application, including transients.

(e) Interwinding capacitance is usually insignificant but may be a path for undesirable stray signals at high frequencies.

4.17 SYNCHRONIZATION METHODS

In the basic trigger circuit of Figure 4.47, the UJT can be triggered at any intermediate part of the cycle by reducing either the interbase voltage alone or the supply voltage, V_1. This results in an equivalent decrease in V_P in accordance with Equation 4.1 (or 4.3) and causes the UJT to trigger if V_P drops below the instantaneous value of V_E. Thus, the base-two terminal or the main supply voltage can be used to synchronize the basic trigger circuit. Figure 4.47 illustrates the use of a negative synchronizing pulse at base-two.

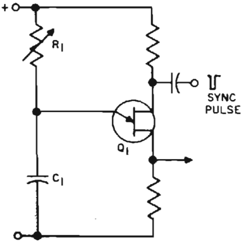


FIGURE 4.47 PULSE SYNCHRONIZATION OF UJT RELAXATION OSCILLATOR

Two methods of achieving synchronization with the AC line are illustrated in Figure 4.48. A full wave rectified signal obtained from a rectifier bridge or a similar source is used to supply both power and a synchronizing signal to the trigger circuit. Zener diode CR_1 is used to clip and regulate the peaks of the AC as indicated in Figures 4.48(a) and (b).

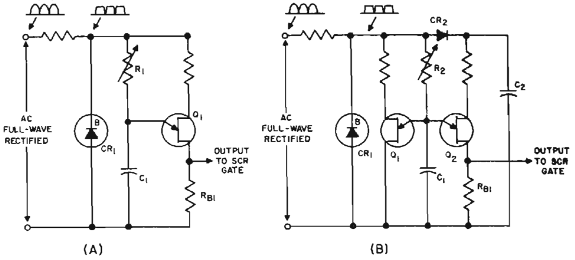


FIGURE 4.48 CIRCUITS FOR SYNCHRONIZATION TO AC LINE

At the end of each half-cycle the voltage at base-two of Q_1 will drop to zero, causing Q_1 to trigger. The capacitors C_1 are thus discharged at the beginning of each half cycle and the trigger circuits are thus synchronized with the line. In Figure 4.48(a) a pulse is produced at the output at the end of each half cycle which can cause the SCR to trigger and produce a small current in the load. If this is undesirable, a second UJT can be used for discharging the capacitor

at the end of the half cycle as illustrated in Figure 4.48(b). Diode CR_1 and capacitor C_2 are used to supply a constant DC voltage to Q_2. The voltage across Q_1 will drop to zero each half-cycle causing C_1 to be discharged through Q_1 rather than through the load R_{B1}. The UJT's should be chosen so that Q_1 has a higher standoff ratio than Q_2.

Synchronization of a PUT circuit is exactly analogous to the UJT since their operation is so similar.

4.18 TRIGGER CIRCUITS FOR INVERTERS

Inverter circuits usually require trigger pulses delivered alternately to two SCR's. There are many ways and types of circuits to perform this function, several of which are mentioned below.

4.18.1 Transistorized Flip-Flops

The transistor flip-flop[8] is a very fundamental and useful circuit for driving SCR or triac gates. The transistor may drive the gates directly, as described in Section 8.9.2, through a transformer or through a pulse shaper as shown in Section 4.19. The transformer must be designed to avoid saturation at the lowest operating frequency and highest supply voltage. The flip-flop may be driven by a UJT or a PUT relaxation oscillator for precise timing or may be connected as a free-running multivibrator.

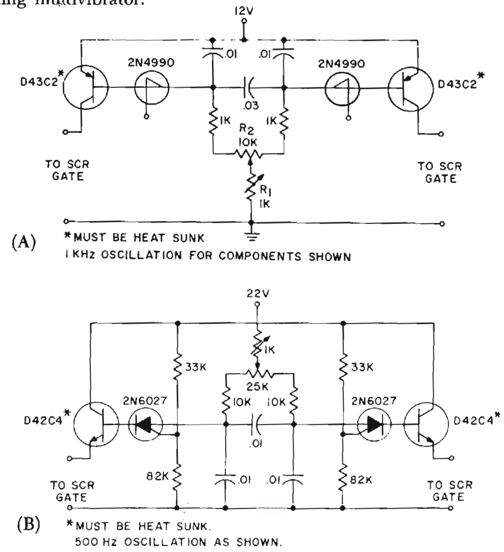


FIGURE 4.49 FLIP-FLOP TRIGGER CIRCUITS FOR TWO INVERTER SCR'S

Figure 4.49 shows two approaches which provides alternate output pulses such as required by many inverter circuits. Alternate output pulses are obtained by cross coupling two relaxation oscillator circuits by capacitor C_1. Frequency is trimmed by potentiometer R_1 and symmetry is trimmed by R_2. Both circuits offer the same rise times and have an upper frequency limit of 20 kHz but the circuit with the PUT does possess greater versatility and higher output voltages. The oscillation frequency of the latter can be varied either by changing the capacitors or by varying the gate bias on the PUT.

4.18.2 PUT Flip-Flop Trigger Circuit

This flip-flop circuit consists of two relaxation oscillator circuits coupled together as shown in Figure 4.50. When one of the two trigger devices is in the "on state," the other is always in the "off state." Turning on one device will instantaneously produce a negative voltage on the other due to the presence of capacitor C_T. This will shift it to the "off state." The frequency is adjusted by R_1 and the symmetry is trimmed by R_2. Outputs V_1 and V_2 may be coupled to additional stages of amplification before coupling to the gate.

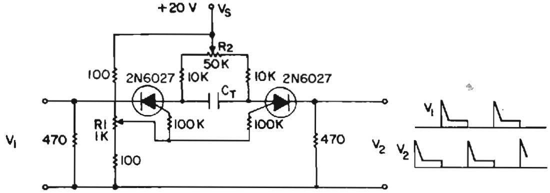


FIGURE 4.50 FLIP-FLOP TRIGGER CIRCUIT

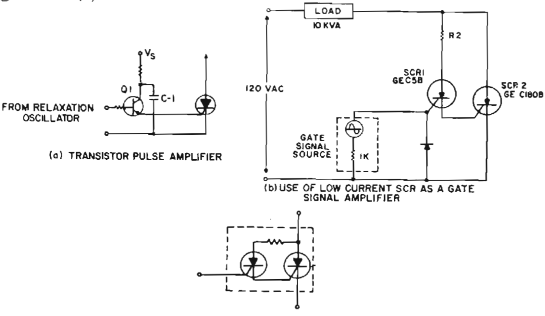
4.19 PULSE AMPLIFICATION AND SHAPING

Consideration of SCR trigger requirements may reveal that the output of a pulse generator is not of sufficient amplitude and/or its output rise time is too slow. With little additional expense, the output can be bolstered to meet the stringent gate requirements of SCR's working at high frequencies and high di/dt.

Figure 4.51 shows several gate amplifier circuits. Circuit (a) utilizes a transistor amplifier which is saturated during the duration of the relaxation oscillator pulse. This allows C_1 to discharge into the SCR.

The availability of SCR's with highly sensitive gates permits use of these devices to trigger higher rated SCR's as shown in Figure 4.51(b). Here, for example, a C5B as SCR_1 requires less than 200 microamperes of gate signal to trigger. Current then flows through R_2, SCR_1, and into the gate of SCR_2. When the current reaches the triggering requirements of SCR_2, this device turns on and shunts the main power away from SCR_1. In addition to providing a means of triggering high current SCR's by low level signals from high impedance sources, this type of triggering yields positive triggering from pulsed gate signals even with highly inductive loads due to the much lower latching current requirements of the C5 in comparison with the higher rated

SCR's. With SCR_1 latched into conduction, the gate of SCR_2 is driven by a trigger signal which is maintained until SCR_2 is forced into conduction. R_2 limits the current through SCR_1 to a value within its rating. SCR_1 must meet the same voltage requirements as SCR_2. However, its current duty is generally of a pulsed nature, and hence negligible. Several types of SCR's such as the C398 and C158 have amplifying gates, in which the predriver SCR's are internal to the device as shown in Figure 4.51(c).



(c) AMPLIFYING GATE SCR

FIGURE 4.51 TRIGGER PULSE AMPLIFIER CIRCUITS

Predrivers are particularly useful when the trigger voltage must be maintained for the entire conduction period. Under these conditions, the power dissipation in the gate of the power device may be excessive. Figure 4.52 provides a technique of maintaining trigger drive during the conduction period in the form of a pulse train and thus reducing the average gate dissipation. The transistor multivibrator, provides alternate driving voltages to the two unijunction transistor oscillators. The outputs of these oscillators provide the alternating pulse train sequence as required for inverter circuits.

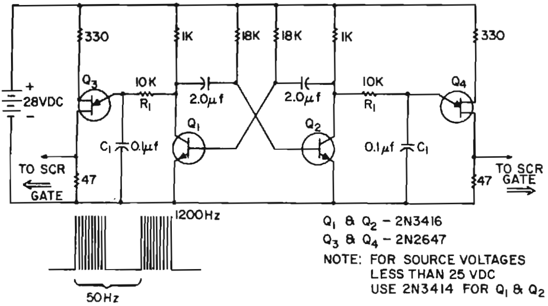


FIGURE 4.52 TRIGGER CIRCUIT PROVIDING TRAIN OF PULSES

For some high current switching applications, it is desirable to trigger with a fast rise-time pulse. A slow rising pulse may be sharpened by use of the circuit in Figure 4.53. When a pulse appears at the input of this circuit, the diode D_1 will conduct, charging the capacitor. The forward drop across the diode will assure a positive gate to anode voltage on the PUT and will prevent it from switching. When the capacitor charges to the peak voltage of the pulse, the diode will become reverse biased and the PUT will switch on. The consequent pulse delivered to the SCR will have a rise time of 50 to 100 nanoseconds determined by the PUT turn-on characteristics.

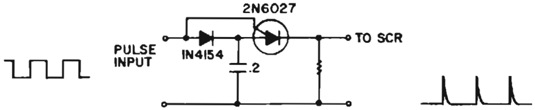


FIGURE 4.53 PULSE SHARPENER USING A PUT

It has been noted that for fast rising current loads, an SCR may require a fast rising high level rectangular pulse to assure triggering. Rectangular pulses can be shaped by the use of reactive pulse forming networks or by blocking oscillators. However, these circuits are relatively costly and large. Figure 4.54 shows a circuit which will generate rectangular pulses of 10 μseconds pulse width at repetition rates up to 20 kHz and does not require any inductive elements. With a 20 volt amplitude and 20 ohm source impedance, this circuit should adequately trigger most SCR's even under the most stringent di/dt conditions. The UJT operates as a conventional relaxation oscillator whose frequency may be controlled by any of the techniques that were previously mentioned. The UJT output pulses drive a four transistor amplifier circuit which improves the rise time and extends the pulse width to approximately 10 μseconds.

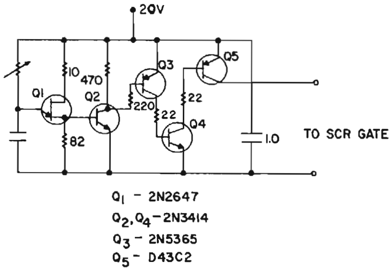


FIGURE 4.54 HIGH di/dt TRIGGER CIRCUIT

Depending on the nature of the control input signal other types of SCR's can be considered for triggering larger SCR's. The LASCR (Chapter 14) can be used where direct triggering by light is required. Also, the LASCR in conjunction with a suitable light source provides a simple way in which to obtain electrical isolation in SCR control circuitry.

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*Refer to Chapter 23 for availability and ordering information.

5 DYNAMIC CHARACTERISTICS OF SCR'S

Dynamic characteristics of an SCR refer to the SCR behavior during switching intervals. This may be switching of the SCR under consideration (either turn-on or turn-off) or switching elsewhere in the circuit (resulting in high dv/dt applied to the SCR). Although this typically represents a minor percentage of the time period, it often demands major consideration by both the manufacturer and user of the SCR.

During the turn-off, or commutation, interval the SCR characteristics to be considered are turn-off time, reapplied dv/dt, and reverse recovered charge. Each of these dynamic characteristics are dependent upon the set of operating conditions of the specific circuit.

During the turn-on interval the dynamic condition to be considered by the circuit designer is the rate of rise of forward current, di/dt. Switching losses during both turn-on and turn-off may be of concern to the equipment designer.

Another dynamic condition, a fast-rising forward voltage, can result in the SCR being switched from the blocking state to the on-state.

5.1 SCR TURN-OFF TIME, t_q

If forward voltage is applied to a undirectional thyristor (hereafter referred to as "SCR") too soon after anode current ceases to flow, the SCR will go into the conduction state again. It is necessary to wait for a definite interval of time after cessation of current flow before forward voltage can be reapplied. Chapter 1 describes the physical reasons for this required interval. For turn-off-time as it affects bi-directional thyristors, see Chapter 7.

To measure the required interval, the SCR is operated with current and voltage waveforms shown in Figure 5.1. The interval between t_3 and t_8 is then decreased until the point is found when the SCR will just support reapplied forward voltage.

This interval is not a constant, but is a function of several parameters. Thus, the minimum time t_3 to t_8 will increase with:

1. An increase in junction temperature.
2. An increase in forward current amplitude (t_1 to t_2).
3. An increase in the rate of decay of forward current (t_2 to t_3).
4. A decrease in peak reverse current (t_4).
5. A decrease in reverse voltage (t_5 to t_7).
6. An increase in the rate of reapplication of forward blocking voltage (t_8 to t_9).
7. An increase in forward blocking voltage (t_9 to t_{10}).
8. An increase in external gate impedance.
9. A more positive gate bias voltage.

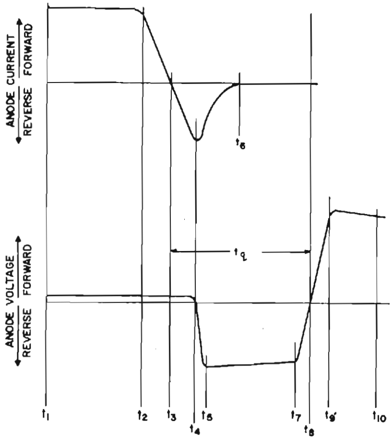


FIGURE 5.1 SCR WAVEFORM FOR TURN-OFF TIME MEASUREMENTS

5.1.1 SCR Turn-Off Time Definitions

Circuit commutated turn-off time of an SCR, t_q, is the time interval between the instant when the anode current has decreased to zero, and the instant when the SCR has regained some defined forward blocking voltage capability.

As mentioned in Section 5.1, t_q is not a constant, but is dependent upon the test conditions under which it is measured. One of these test conditions, forward current (I_T), is shown in Figure 5.2 for a narrow pulse of current and in Figure 5.3 for conventional circuit turn-off time. Refer to Chapter 2 for definition of terms used in the figures.

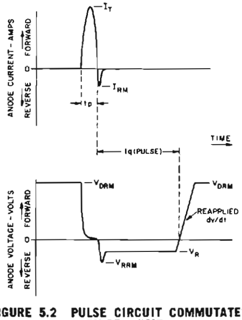


FIGURE 5.2 PULSE CIRCUIT COMMUTATED TURN-OFF TIME

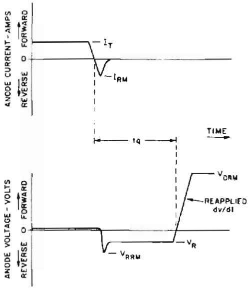


FIGURE 5.3 CONVENTIONAL CIRCUIT COMMUTATED TURN-OFF TIME

5.1.2 Typical Variation of Turn-Off Time

The extent to which the parameters in Section 5.1 affect turn-off time is dependent on both the parameter being considered and the device design. Turn-off time performance trade-off curves are used to determine which parameters are of significance, depending on the particular set of circuit operating conditions. Figure 5.4 for example shows a typical curve of change in SCR turn-off time with junction temperature for a specific SCR. Figure 5.5 shows the dependence of t_q on forward current, for rectangular current pulses for that same SCR.

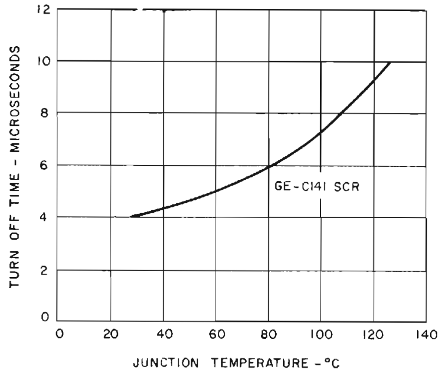


FIGURE 5.4 VARIATION OF TURN-OFF TIME WITH JUNCTION TEMPERATURE

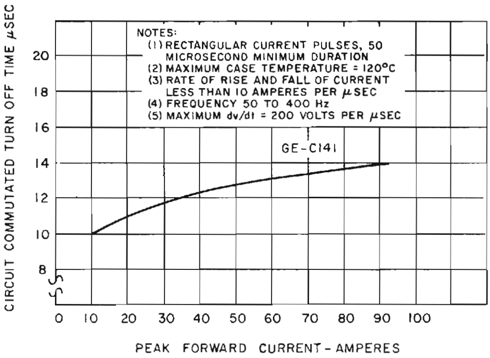


FIGURE 5.5 VARIATION OF TURN-OFF TIME WITH PEAK FORWARD CURRENT FOR A HIGH SPEED SCR

Typical variation of turn-off time with applied reverse voltage is seen in Figure 5.6 for the C158 SCR.

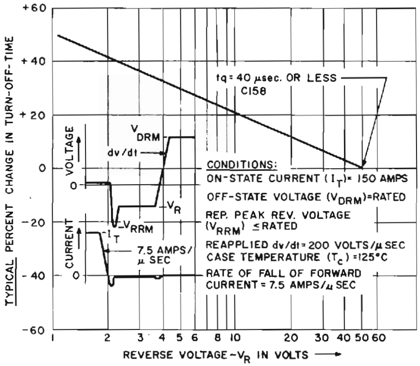


FIGURE 5.6 TYPICAL VARIATION OF TURN-OFF TIME WITH APPLIED REVERSE VOLTAGE DURING THE TURN-OFF INTERVAL

Typical dependence of turn-off time on another test condition, reapplied dv/dt, is shown in Figure 5.7. Specified turn-off time for the C158 is with a reapplied dv/dt test condition of 200 volts per microsecond.

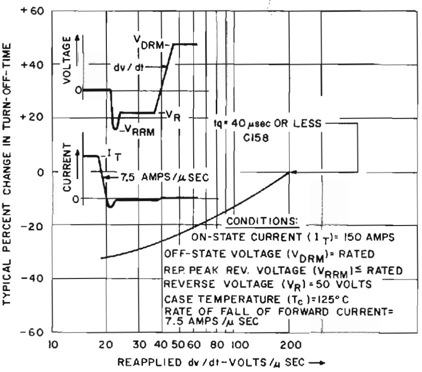


FIGURE 5.7 TYPICAL VARIATION OF SCR TURN-OFF TIME WITH REAPPLIED DV/DT

5.1.3 Circuit Turn-off Time (t_c)

Circuit turn-off time is the turn-off time that the circuit presents to the SCR.

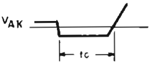
The circuit turn-off time (t_c) must always be greater than the turn-off time of the SCR (t_q); otherwise the SCR may revert to the on-state.

The turn-off times of general purpose phase control SCR's are usually given as typical values if at all. Wide deviations from the typical values can occur. In those circuits where turn-off time is a critical characteristic, it is necessary for the circuit designer to have control over the maximum value of SCR turn-off time. For this reason General Electric offers a range of SCR's with guaranteed maximum turn-off times under specified standard conditions of waveform and temperature. These SCR's are designed specifically for inverter applications where the need for good dynamic capabilities is essential.

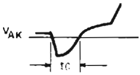
5.1.4 Feedback Diode

Many inverter circuits require the use of a feedback diode placed in inverse parallel with the SCR. The diode is needed to carry reactive energy to the supply during some portion of the operating period. This diode is a disadvantage from an SCR turn-off standpoint. The reverse voltage of the SCR during the commutation interval is limited to the diode forward voltage thereby adversely affecting SCR turn-off time as discussed earlier in this chapter.

The feedback diode, when needed, should be placed close to the SCR in order to minimize inductance in the diode path. As shown in the sketch, this inductance undesirably shortens the circuit turn-off time because of the voltage induced in the inductance due to the changing current (V = L di/dt).



(a) Diode adjoining SCR, No Inductance



(b) Inductance in Diode Path

5.2 TURN-OFF METHODS

The gate has no control over the SCR once anode-to-cathode current exceeds latching current. External measures therefore have to be applied to stop the flow of current. There are two basic methods available for commutation, as the turn-off process is called.

5.2.1 Current Interruption

The current through the SCR may be interrupted by means of a switch in either of two circuit locations. The switch must be operated for the required turn-off time. Note that the operation of the switch will cause the SCR to see high values of dv/dt. In Figure 5.8(a) when the switch is closed, or in 5.8(b) when the switch is opened, the SCR is susceptible to false turn-on due to high dv/dt.

As it is seldom that a mechanical switch is suitable for commutation, various static switching circuits have been developed for this purpose. It should be noted that SCR's are generally not characterized for this mode of commutation.

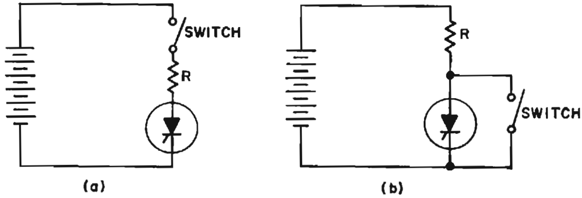


FIGURE 5.8 COMMUTATION BY CURRENT INTERRUPTION

5.2.2 Forced Commutation

When the above methods of current interruption are not acceptable, then forced commutation must be used. The essence of forced commutation is to decrease the SCR current to zero either by transferring the load current to a preferred path or by decreasing the load current to zero.

5.3 CLASSIFICATION OF FORCED COMMUTATION METHODS

There are six distinct classes by which the energy is switched across the SCR to be turned off:

Class A Self commutated by resonating the load
Class B Self commutated by an LC circuit
Class C C or LC switched by another load-carrying SCR
Class D C or LC switched by an auxiliary SCR
Class E An external pulse source for commutation
Class F AC line commutation

Examples of circuits which correspond to these classes will now be given. These examples show the classes as choppers (Chapter 13). The commutation classes may be used in practice in configurations other than choppers. References to literature covering the different classes will be found in Chapter 13.

5.3.1 Class A—Self commutated by resonating the load

When SCR_1 is triggered, anode current flows and charges up C

in the polarity indicated. Current will then attempt to flow through the SCR in the reverse direction and the SCR will be turned off.

The condition for commutation is that the RLC circuit must be under-damped.

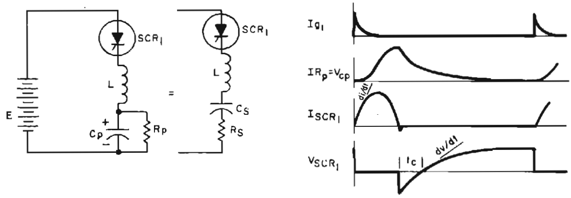


FIGURE 5.9 CLASS A COMMUTATION

5.3.2 Class B—Self commutated by an LC circuit

Example 1

Before the gate pulse is applied, C charges up in the polarity indicated.

When SCR_1 is triggered, current flows in two directions.

1. The load current I_R flows through R.

2. A pulse of current flows through the resonant LC circuit and charges C up in the reverse polarity. The resonant-circuit current will then reverse and attempt to flow through the SCR in opposition to the load current. The SCR will turn off when the reverse resonant-circuit current is greater than the load current.

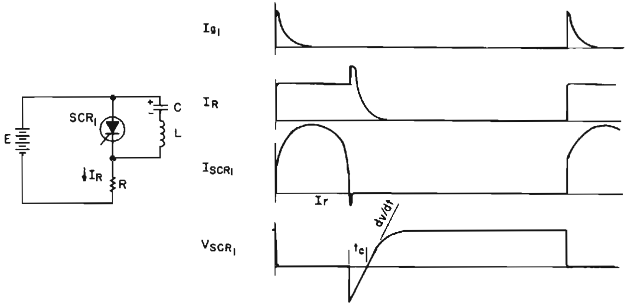


FIGURE 5.10 CLASS B COMMUTATION (EXAMPLE 1)

Class B—Self commutated by an LC circuit

Example 2 – The Morgan Circuit

From the previous cycle the capacitor is charged as shown in Figure 5.11 and the reactor core has been saturated "positively."

When SCR_1 is triggered, the capacitor voltage is applied to the reactor winding L_2. The polarity of the applied voltage immediately pulls the core out of saturation. For the time t_1 to t_2 (Figure 5.11) the load current is flowing through R. Simultaneously the capacitor is being discharged.

When the voltage across L_2 has been applied for the prescribed time, the core goes into "negative" saturation. The inductance of L_2 changes from the high unsaturated value to the low saturated value.

The resonant charging of C now proceeds much more rapidly from time t_2 to t_3. As soon as the peak of current is reached and current starts to decrease, the voltage across L_2 reverses.

As soon as the voltage reverses, the core comes out of saturation again, the inductance rises to the high value and the recharging of C proceeds at a more leisurely pace (t_3 to t_4).

The voltage across the inductor is held for the prescribed time and then positive saturation occurs (t_4).

Now the capacitor is switched directly across the SCR via the saturated inductance of L_2. If the reverse current exceeds the load current SCR_1 will be turned off. The remaining charge in C then is

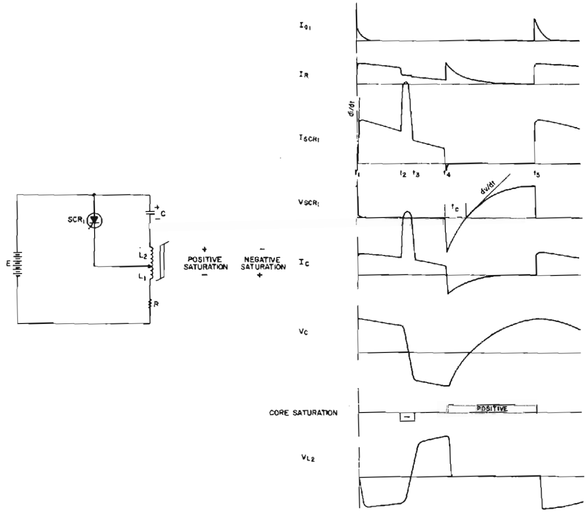


FIGURE 5.11 CLASS B COMMUTATION (EXAMPLE 2)

dissipated in the load and C is charged up and ready for the next cycle (t_5).

It is quite possible in practice to design L so that negative saturation does not occur. In this case the anode-current pulse from t_2 to t_3 is omitted.

5.3.3 Class C—C or LC switched by another load-carrying SCR

Assume SCR_2 is conducting. C then charges up in the polarity shown. When SCR_1 is triggered, C is switched across SCR_2 via SCR_1 and the discharge current of C opposes the flow of load current in SCR_2.

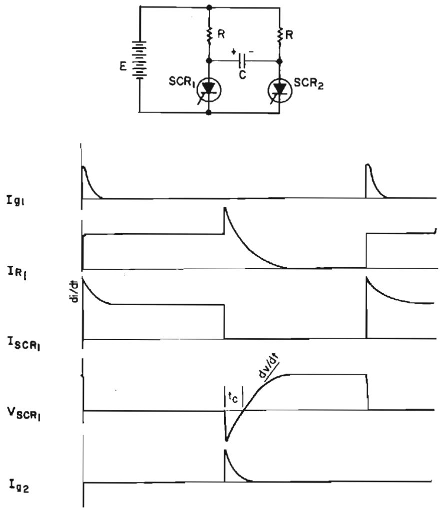


FIGURE 5.12 CLASS C COMMUTATION

5.3.4 Class D—LC or C switched by an auxiliary SCR

Example 1

The circuit shown in Figure 5.12 (Class C) can be converted to Class D if the load current is carried by only one of the SCR's, the other acting as an auxiliary turn-off SCR. The auxiliary SCR would have a resistor in its anode lead of say ten times the load resistance.

Example 2

SCR_2 must be triggered first in order to charge up the capacitor in the polarity shown. As soon as C is charged, SCR_2 will turn off due to lack of current.

When SCR_1 is triggered the current flows in two paths: Load current flows in R; commutating current flows through C, SCR_1, L, and D, and the charge on C is reversed and held with the hold-off diode D. At any desired time SCR_2 may be triggered which then places C across SCR_1 via SCR_2 and SCR_1 is turned off.

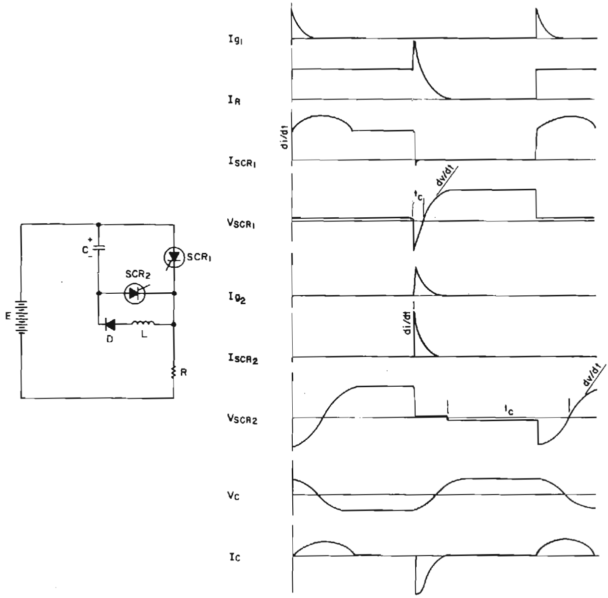


FIGURE 5.13 CLASS D COMMUTATION (EXAMPLE 2)

Class D—LC or C switched by an auxiliary SCR

Example 3 – The Jones Circuit

The outstanding feature of this circuit is its ability to start commutating reliably.

If C were discharged, then, on triggering SCR_1, voltage would be induced into L_2 by closely coupled L_1, and C would become charged in the polarity shown. As soon as SCR_2 is triggered, SCR_1 turn-off interval is initiated. C now becomes charged in the opposite polarity.

The next time SCR_1 is triggered, C discharges via SCR_1, and L_2, and its polarity is reversed ready for the next commutating pulse. The voltage to which C is charged (in the polarity shown in Figure 5.14), depends on which is greater: the voltage induced by load current flowing in L_1 or the reversal of the positive charge built up while SCR_2 was conducting.

With heavy loads, the induced voltage increases, thus tending to offset the decrease of turn-off time. Better turn-off times are obtained with this circuit as compared with Example 2 at the cost of higher voltages appearing across the SCR's. This circuit is discussed in more detail in Chapter 13.

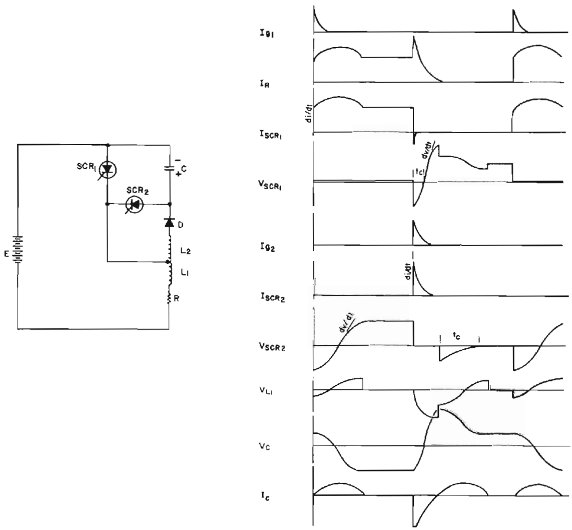
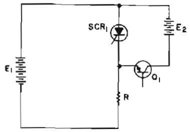


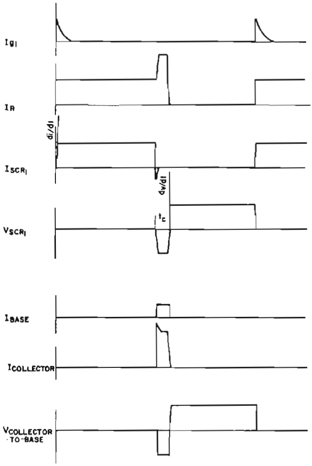
FIGURE 5.14 CLASS D COMMUTATION (EXAMPLE 3)

5.3.5 Class E—External pulse source for commutation

Example 1

When SCR_1 is triggered, current will flow into the load. To turn SCR_1 off base drive is applied to the transistor Q_1. This will connect auxiliary supply E_2 across SCR_1 turning it off. Q_1 is held on for the duration of the turn-off time.





5.15 CLASS E COMMUTATION (EXAMPLE 1)

Class E—External pulse source for commutation

Example 2

The transformer is designed with sufficient iron and air gap so as not to saturate. It is capable of carrying the load current with a small voltage drop compared with the supply voltage.

When SCR_1 is triggered, current flows through the load and pulse transformer. To turn SCR_1 off a positive pulse is applied to the cathode of the SCR from an external pulse generator via the pulse transformer. The capacitor C is only charged to about 1 volt and for the duration of the turn-off pulse it can be considered to have zero impedance. Thus the pulse from the transformer reverses the voltage across the SCR, and it supplies the reverse recovery current and holds the voltage negative for the required turn-off time.

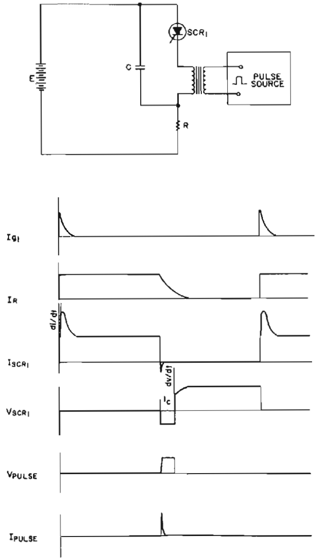


FIGURE 5.16 CLASS E COMMUTATION (EXAMPLE 2)

Class E—External pulse source for commutation

Example 3

When the SCR is turned on, the pulse transformer saturates and presents a low impedance path for the load current. When the time comes for turning off the SCR, the first step is to de-saturate the pulse transformer. This is done by means of a pulse in the polarity shown. This de-saturating pulse momentarily increases the voltage across the load and also the load current. Once the pulse transformer is de-saturated, a pulse in the reverse polarity is injected, reversing the voltage across the SCR and turning it off. The pulse is held for the required turn-off time.

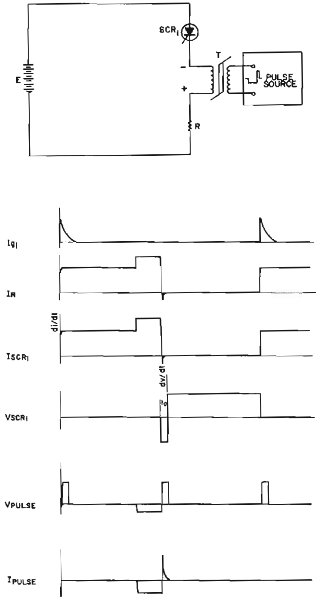


FIGURE 5.17 CLASS E COMMUTATION (EXAMPLE 3)

Class E—External pulse source for commutation

Example 4

This circuit is important because no capacitor-charging pulse flows through the load.

Assume C is charged in the polarity shown to some voltage greater than the supply voltage E. When SCR_1 is triggered, load current flows in R and L_2. SCR_2 is in a resonant circuit consisting of C and L_2. When SCR_2 is triggered, a pulse of current flows through L_2. A voltage is developed across L_2 which is greater than the supply voltage E. Reverse voltage is therefore applied to SCR_1 which turns it off. The termination of the discharge pulse through SCR_2 turns it off, and C is now charged in the opposite polarity. L_1 is much larger than L_2, and C is now resonantly charged via L_1 and D to some voltage greater than the supply voltage.

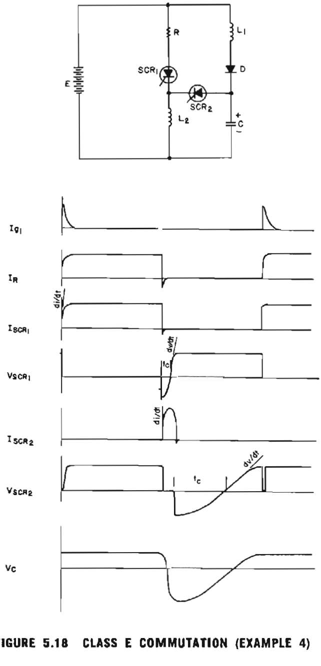


FIGURE 5.18 CLASS E COMMUTATION (EXAMPLE 4)

5.3.6 Class F—AC line commutated

If the supply is an alternating voltage, load current will flow during the positive half cycle. During the negative half cycle the SCR will turn off due to the negative polarity across the SCR. The duration of the half cycle must be longer than the turn-off time of the SCR.

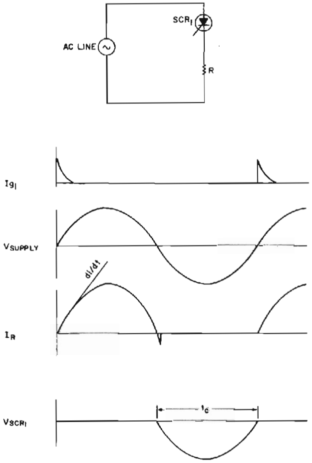


FIGURE 5.19 CLASS F COMMUTATION

5.4 RATE OF RISE OF FORWARD VOLTAGE, dv/dt

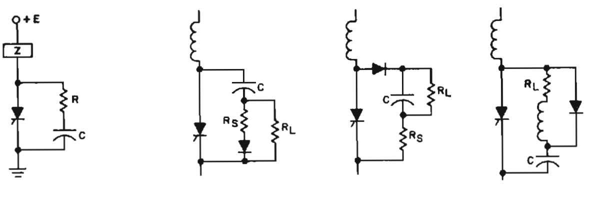
The junctions of any semiconductor exhibit some unavoidable capacitance. A changing voltage impressed on this junction capacitance results in a current, $i = C\,dv/dt$. If this current is sufficiently large a regenerative action may occur causing the SCR to switch to the on-state. This regenerative action is similar to that which occurs when gate current is injected, as discussed in Chapter 1. The critical rate of rise of off-state voltage is defined as the minimum value of rate of rise of forward voltage which may cause switching from the off-state to the on-state.

Since dv/dt turn-on is non-destructive, this phenomenon creates no problem in applications in which occasional false turn-on does not result in a harmful affect at the load. Heater application is one such case.

The majority of inverter applications, however, would result in circuit malfunction due to dv/dt turn-on. One solution to this problem is to reduce the dv/dt imposed by the circuit to a value less than the critical dv/dt of the SCR being used. This is accomplished by the use of a circuit similar to those in Figure 5.20 to suppress excessive rate of rise of anode voltage. Z represents load impedance and circuit impedance.

Since circuit impedances are not usually well defined for a particular application, the values of R and C are often determined by experimental optimization. A technique described in Chapter 16 can be used to simplify snubber circuit design by the use of nomographs which enable the circuit designer to select an optimized R-C snubber for a particular set of circuit operating conditions.

Another solution to the dv/dt turn-on problem is to use an SCR with higher dv/dt capability. This can be done by selecting an SCR designed specifically for high dv/dt applications, as indicated by the specification sheet. Emitter shorting, as discussed in Chapter 1, is a manufacturing technique used to accomplish high dv/dt capability.



(a) Basic Circuit (b) Circuit Variations

FIGURE 5.20 DV/DT SUPPRESSION CIRCUITS

Higher dv/dt capability can also be attained by choosing an SCR with higher voltage classification. Since a high circuit-imposed dv/dt effectively reduces $V_{(BO)}$ (the actual anode voltage at which the particular device being observed switches into the on state) under given temperature conditions, a higher voltage classification unit will allow a higher rate of rise of forward voltage for a given peak circuit voltage.

Alternatively, this increased dv/dt capability can be understood by reference to Figure 5.21, the typical variation of dv/dt capability with applied voltage. By choosing an SCR with higher V_{DRM}, the ratio of $V_{applied}$ to V_{DRM} will be lower for a given circuit and as indicated in Figure 5.21 the typical dv/dt capability will be higher. By making use of this technique, the SCR can be selected by the manufacturer for dv/dt capability in excess of that indicated on the specification sheet.

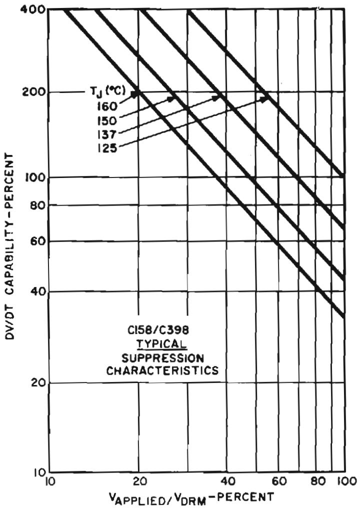


FIGURE 5.21 TYPICAL VARIATION OF DV/DT CAPABILITY WITH APPLIED VOLTAGE

Reverse biasing of the gate with respect to the cathode may increase dv/dt capability for small area SCR's not already designed for high dv/dt. The reader is referred to Chapter 4 for further discussion.

5.4.1 Reapplied dv/dt

Reapplied rate of rise of voltage, reapplied dv/dt, is the rate of rise of forward voltage following the commutation interval. Reapplied dv/dt is of importance because of its affect on turn-off time. The affect

on t_q of reapplied dv/dt, a test condition for t_q measurement, can be seen in Figure 5.7. Triac applications, discussed in Chapter 7, also require consideration of dv/dt.

5.5 RATE OF RISE OF ON-STATE CURRENT, di/dt

Critical di/dt is the maximum allowable value of the rate of rise of on-state current. The di/dt of on-state current while the SCR is in the process of turning on must be considered because it is capable of destroying the SCR or, in the absence of destruction, can cause a high switching loss. During the turn-on process only a small percentage of the silicon is conductive due to the finite spreading velocity, as discussed in Reference 2. A fast rising current can result in a high current density in that portion of silicon that is conducting. This high current density may result in excessive heat and a destroyed SCR.

5.5.1 Solutions to di/dt Problem

Inverter circuits with inherently high di/dt waveshapes can be made to operate reliable by choosing an SCR with high di/dt capability. The SCR manufacturer can attain this high di/dt capability by appropriate gate construction techniques as discussed in Chapter 1.

An additional technique used to accomplish high di/dt capability is to employ a hard-drive gate circuit. A hard drive consists of a fast rising gate current. Reference 5 discusses trigger circuit design techniques to accomplish high di/dt capability.

A saturable reactor in series with the SCR during its turn-on switching interval will greatly reduce switching dissipation in the SCR. When the SCR is triggered on, the amount of current that will flow during the turn-on interval is limited to the magnetizing current of the reactor. The reactor is designed to go into magnetic saturation sometime after the SCR has been triggered. The delay time is employed to bring operation of the SCR within its turn-on current limit capability. Sufficient SCR active area is then available to assume full load current at minimum dissipation. Since the load current is delayed, the output of the SCR-reactor combination is delayed relative to the SCR trigger signal. Realistic pulse repetition rates are achievable by this technique, notably in many pulse modulator applications.

The delay time t of the saturable reactor is given by the time to saturate

$$t_s = \frac{NA \triangle B\ 10^{-8}}{E} \text{ (seconds), where} \tag{5.1}$$

N = number of turns
A = cross sectional area of core in square centimeters
$\triangle B$ = total flux density change in Gauss
E = maximum circuit voltage being switched in volts

The current required at the time of saturable reactor switching I_s should be made small compared to the peak load current being switched. It is:

$$I_s = \frac{H_s l_m}{0.4\pi N} \text{ (amperes), where} \tag{3.4}$$

H_s = magnetizing force in Oersteds required for core flux to reach saturation flux density B_s (1 Oersted = 2.021 ampere-turns/inch)

l_m = mean length of core in centimeters

N = number of turns

Provision must be made to properly reset the core before the next current pulse. Depending on the details of the circuit, reset may be accomplished by the resonant reversal of current (reverse recovery current) or by auxiliary means.

5.6 REVERSE RECOVERY CHARACTERISTICS

The time during which reverse recovery current flows in the SCR (t_3 to t_6 in Figure 5.1) is known as the reverse recovery time. This is the time required before the SCR can block *reverse* voltage. This should not be confused with turn-off time which is the time that has to elapse before the SCR can block reapplied *forward* voltage. The reverse recovery phenomenon is also common in junction diodes.

Reverse recovery time in typical SCR's is of the order of a few microseconds. Recovery time increases as forward current increases and also increases as the rate of decay of forward current decreases. In addition, an increase of recovery time results from an increase of junction temperature.

The reverse recovery current phenomenon plays a minor but important part in the application of SCR's:

1. In full wave rectifier circuits using SCR's as the rectifying elements the reverse recovery current has to be carried in the forward direction by the complementary SCR's. This can give rise to high values of turn-on current.

2. In certain inverter circuits such as the McMurray-Bedford circuit (Chapter 13) where one SCR is turned off by turning another on, the reverse recovery current of the first gives rise to high values of turn-on current in the second.

3. The cessation of reverse current, which can be very sudden, may produce damaging voltage transients and radio frequency interference.

4. When SCR's are connected in series the reverse voltage distribution may be seriously affected by mismatch of reverse recovery times (Chapter 6).

Recovered charge, Q_R, (the time integral of reverse current), is the amount of charge in microcoulombs corresponding to the recovery interval. Figure 5.22 indicates the dependence of recovered charge on reverse di/dt. An inductor may be needed to limit recovered charge within a value acceptable for circuit operation. This inductance may be in the form of source, circuit, or load impedance. This same inductor serves to prevent di/dt failures as discussed in Section 5.5.1 above.

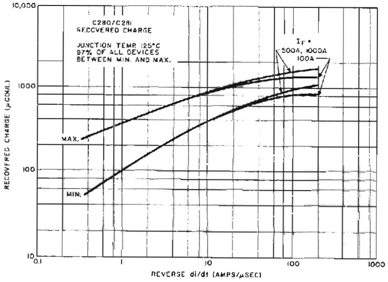


FIGURE 5.22 RECOVERED CHARGE AT 125°C

5.7 CAPACITORS FOR COMMUTATION CIRCUITS

The characteristics of the commutation capacitors must be carefully considered by the design engineer in their selection and specification. The following properties are desirable:

1. The capacitor life should be long, at the operating ambient temperature.
2. The power losses in the capacitors should be low for two reasons:
   a. To avoid high internal temperatures which would shorten the capacitor life.
   b. To maintain the advantage of high efficiency which the SCR gives to the over-all circuit.
3. The capacitor's equivalent series inductance should be known. In many circuits, inductance in series with the commutating capacitor plays an important part in controlling the initial rate of rise of anode current through the SCR.

The equipment designer is advised to take the following steps:

1. For the breadboard, standard inverter capacitors may be purchased from the General Electric Capacitor Department, Hudson Falls, New York. Figure 5.24 gives the ratings of standard capacitors. All General Electric SCR capacitors have heavy duty internal connections to carry the high currents, extended foil construction to give low inductance and minimum ESR (equivalent series resistance) and incorporate painted cases to keep the dielectric temperature rise to a minimum.

2. After completion of the breadboard tests, the voltage and current waveforms and temperature data should be submitted to the capacitor manufacturer for optimization of life, size, and cost. (See check list at end of chapter.)

The RMS current encountered in SCR applications is usually significant and even with minimum ESR the I^2R losses can be great. While

proper capacitor selection will provide a suitable component, the inherent power losses must be considered by the designer from a total circuit standpoint.

Another important consideration is the current carrying capability or limit of the capacitor itself. The maximum current capability of any capacitor listed in the Standard Ratings Table is 50 amperes RMS. Metalized designs have limits of 12 and 20 amperes RMS to gain optimum volumetric efficiency. In several cases, the RMS current listed is greater than these actual operating current limits. The greater values may only be used for derating purposes along with multipliers from the derating table Figure 5.23. All capacitors with such listed ratings are clearly indicated in the Standard Ratings Table with explanatory footnotes.

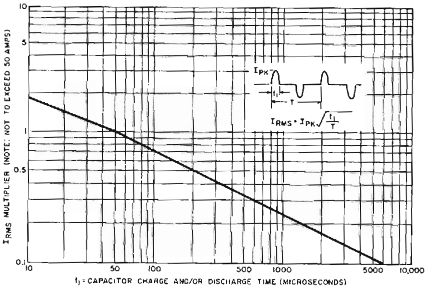


FIGURE 5.23 CORRECTION FACTOR TO BE APPLIED TO CURRENT (I_{RMS}) FOR CAPACITOR CHARGE OR DISCHARGE TIMES OTHER THAN 50 MICROSECONDS

The RMS current values in the standard ratings table are based on a current pulse width of 50 microseconds. Selection of capacitors for circuits involving 50 microseconds pulse widths can be made directly from the Standard Ratings Table by knowing the capacitance, voltage, RMS current and ambient operating temperature. For circuits involving pulse widths other than 50 microseconds the following example is offered.

Pulse width less than 50 μsec. Given:

Capacitance: 5 MFD $\pm$ 10 percent

Voltage: 65 VAC, 16.6 Khz continuous sinewave

Current: 34 amps RMS

Temperature: 80 C

a. Select a 5 MFD unit with an 80 C current rating near 34 amps RMS. 28F1248 has a current rating of 30.6 for 50 microseconds.

b. The current multiplier for 16.6 Khz (pulse width = 30 microseconds) from Figure 5.23 is 1.2.

c. Allowable current for Cat. No. 28F1248 at 16.6 Khz is (1.2) (30.6) = 36.7 amps RMS.

d. Since the allowable current of 36.7 amps is greater than the required value of 34 amps RMS, this unit is adequate.

STANDARD RATINGS

Dielectric	Nameplate Rating			Dimensions in inches			Volts Max. RMS AC	Max. RMS (Amperes) At Max. Ambient Temp†		
	Peak Volts*	μf	Catalog Number	Width	Depth	Case Height		60 C	70 C	80 C
	200	1		Use 1000 Volt Rating			200			
	200	2		Use 400 Volt Rating			200			
	200	3	28F5101	2.16	1.31	2.06	200	8.9	6.6	3.8
	200	5	28F5102	2.16	1.31	2.56	200	12.8	9.5	5.5
Paper	200	10	28F5103	2.16	1.31	3.81	200	22.1	16.3	9.4
	200	15	28F5104	2.16	1.31	4.69	200	30.1	22.1	12.8
	200	20	28F5105	2.69	1.56	4.50	200	37.7	27.8	16.1
	200	30	28F5106	2.91	1.91	5.25	200	52.6‡	38.9	22.4
	200	40	28F5107	2.91	1.91	6.75	200	68.9‡	50.9‡	29.4
	200	50	28F5108	3.66	1.97	6.25	200	81.1‡	59.9‡	34.6
	400	1		Use 1000 Volt Rating			300			
	400	2	28F5110	2.16	1.31	2.06	300	7.3	5.4	3.1
	400	3	28F5111	2.16	1.31	2.31	300	9.4	7.0	4.0
	400	5	28F5112	2.16	1.31	3.06	300	14.0	10.3	6.0
Paper	400	10	28F5113	2.69	1.56	4.50	300	26.6	19.7	11.4
	400	15	28F5114	2.91	1.91	4.75	300	35.4	26.2	15.1
	400	20	28F5115	2.91	1.91	6.25	300	46.9	34.6	20.0
	400	30	28F5116	3.66	1.97	6.75	300	65.3‡	48.2	27.8
	400	40	28F5117	3.66	1.97	8.00	300	82.1‡	60.6‡	35.0
	400	50	28F5118	4.56	2.84	5.88	300	89.4‡	66.0‡	38.1
	600	1		Use 1000 Volt Rating			400			
	600	2	28F5120	2.16	1.31	2.31	400	7.7	5.7	3.3
	600	3	28F5121	2.16	1.31	2.81	400	10.4	7.7	4.4
	600	5	28F5122	2.16	1.31	3.81	400	15.6	11.5	6.7
	600	10	28F5123	2.91	1.91	4.25	400	27.3	20.2	11.7
Paper	600	15	28F5124	2.91	1.91	5.75	400	39.0	28.8	16.6
	600	20	28F5125	3.66	1.97	5.75	400	49.2	36.3	21.0
	600	25	28F5126	3.66	1.97	6.75	400	59.6‡	44.0	25.4
	600	30	28F5127	3.66	1.97	8.00	400	71.1‡	52.5‡	30.3
	600	40	28F5128	4.56	2.84	5.88	400	79.1‡	58.9‡	33.7
	600	50	28F5129	4.56	2.84	6.75	400	95.8‡	70.8‡	40.8
	1000	1	28F5131	2.16	1.31	2.06	500	5.1	3.8	2.2
	1000	2	28F5132	2.16	1.31	3.06	500	8.9	6.5	3.8
Paper	1000	3	28F5133	2.16	1.31	3.81	500	12.1	8.9	5.2
	1000	5	28F5134	2.69	1.56	4.25	500	18.3	13.5	7.8
	1000	10	28F5135	2.91	1.91	6.25	500	33.2	24.5	14.1
	1000	20	28F5137	4.56	2.84	5.18	500	52.8‡	39.0	22.5
	1500	0.5	28F5141	2.16	1.31	2.06	700	3.6	2.7	1.5
	1500	1	28F5142	2.16	1.31	3.06	700	6.3	4.6	2.7
Paper	1500	2	28F5143	2.69	1.56	3.88	700	11.0	8.2	4.7
	1500	3	28F5144	2.91	1.91	4.25	700	15.0	11.1	6.4
	1500	5	28F5145	2.91	1.91	6.25	700	23.5	17.3	10.0
	1500	10	28F5146	4.56	2.84	5.18	700	37.3	27.6	15.9
	2000	0.25	28F5151	2.16	1.31	2.06	800	2.6	1.9	1.1
	2000	0.50	28F5152	2.16	1.31	2.56	800	4.0	3.0	1.7
	2000	1	28F5163	2.16	1.31	3.44	800	6.6	4.9	2.8
Paper	2000	2	28F5154	2.69	1.56	4.50	800	11.9	8.8	5.1
	2000	3	28F5155	2.91	1.91	4.75	800	15.8	11.7	6.8
	2000	5	28F5156	3.66	1.97	6.25	800	25.6	18.9	10.9
	2000	10	28F5158	4.56	2.84	6.25	800	41.2	30.4	17.6
	600	1	28F1245	2.16	1.31	2.06	330	21.0	15.5	9.0
	600	2	28F1246	2.16	1.31	2.81	330	34.0	25.3	14.6
Poly-	600	3	28F1247	2.16	1.31	3.44	330	45.6	33.8	19.5
carbonate	600	5	28F1248	2.69	1.56	3.88	330	72.0‡	53.0‡	30.6
	600	10	28F1249	2.91	1.91	5.25	330	120.0‡	89.5‡	52.0‡
	600	20	28F1202	3.66	1.97	6.00	330	189.0‡	148.0‡	86.0‡
	200	25	28F1101	2.69	1.56	2.12	120	12.5§	9.7	4.7
Metalized	200	50	28F1102	2.69	1.56	2.88	120	20.4§	15.8§	7.7
Paper	200	100	28F1103	3.66	1.97	3.12	120	34.6¶	26.8¶	13.0
	200	125	28F1104	3.66	1.97	3.88	120	43.2¶	33.2¶	16.3
	200	150	28F1105	3.66	1.97	4.25	120	49.5¶	38.2¶	22.0¶

FIGURE 5.24 EXTRACTS FROM GE CAPACITOR CATALOG

* See "Max. RMS Volts AC" column for a-c Rating.
† Based on 50 microsecond pulse width.
‡ This number is given for purposes of derating only. In no case may capacitor be operated at currents in excess of 50 amps RMS.
§ This number is given for purposes of derating only. In no case may capacitor be operated at currents in excess of 12 amps RMS.
¶ This number is given for purposes of derating only. In no case may capacitor be operated at currents in excess of 20 amps RMS.

CAPACITORS FOR SCR COMMUTATION APPLICATIONS

Design Data Sheet

To assist in obtaining proper capacitor design, it is particularly important that the circuit design engineer sketch out in detail a picture of voltage and current vs. time. This should be done by using the space provided below and showing specific values of voltage, current, and time over a complete cycle.

Primary Information:

Reference No.__________

1. Capacitance Required:_______ Tolerance (if less than ± 10 percent__________
2. Peak to Peak Voltage:_______ Rms Voltage:__________
3. Peak Current:__________ Rms Current:__________
4. Repetition Rate:__________ (cycles per second) Duty Cycle:__________ (time on — time off)
5. Ambient Temperature__________Max.________Min._______
6. Capacitor Discharge Time:____________________
7. Show Sketch of Voltage and Current Wave shape vs. Time. (Fill in below)

\+

Volts 0 Time

\+

Current 0 Time

Secondary Information:

8. Desired Operating Life:____________________(total cycles)
   ____________________(total hours)
9. Sample Requirements: (How many)____________________
   (When needed)____________________
10. Potential Usage:____________________
11. Physical Size Limitations:____________________
12. Mounting Requirements:____________________
13. Applicable Specifications (if any):____________________
14. Unusual Atmospheric Conditions:____________________
    (dust, chemicals, humidity, corrosion, etc.)
15. Other Special Requirement:____________________
    (high altitude, shock, vibration, etc.)
16. What kind cooling available:____________________
    (fins, heat sink, forced air, etc.)

REFERENCES

1. D. E. Piccone and I. S. Somos, "Are You Confused by High di/dt SCR Rating?", The Electronic Engineer, January 1969, Vol. 28, No. 1.
2. Application Note 200.28, "The Rating of SCR's When Switching Into High Currents," N. Mapham, May 1963.
3. S. J. Wu, "Analysis and Design of Optimized Snubber Circuits for dv/dt Protection in Power Thyristor Applications" presented at IEEE IGA Conference, October 1970. Available from General Electric Publication 660.24.
4. GE Capacitor Catalog GEA-8688.
5. J. M. Reschovsky, "Design of Trigger Circuits for Power SCR's," GE Application Note 200.54, February 1970.

NOTES

6 SERIES AND PARALLEL OPERATION

Since the introduction of SCR's in 1957, the power handling capability has been steadily improving with enhanced dynamic performance. SCR's with rated blocking voltage to 2600 volts and RMS current to 1100 amperes are readily available today. The power handling capability of an SCR appears to be limited by the effective utilization of larger and larger silicon wafers, methods of packaging, and techniques of cooling the junction temperature. Still, there are numerous applications where a single SCR cannot meet the power requirements, such as in terminals for HVDC transmission lines and rapid transit systems where system requirements dictate operation at higher voltage and/or current than can be realized within the capabilities of a single SCR. Series/parallel combinations must be employed if system requirements are to be met.

When SCR's are connected in series for high voltage operation, both steady-state and dynamic-state voltages must be equally shared across each unit. The di/dt and the dv/dt limitations must be assured not to exceed the ratings of each SCR. When SCR's are connected in parallel to obtain higher current output, the equalization of forward current, both during the turn-on interval and the conduction state, must be guaranteed either by matching the forward characteristics of individual units or by employing external forced sharing techniques.

Little work has been done on series/parallel connection of triacs. It appears the guidelines outlined here for SCR's generally apply to triacs. To date, the triac has been primarily employed in consumer/appliance/light industrial applications where slightly lower cost of trigger and control circuitry can be important factors.

As requirements for operation from higher voltage sources and at higher current levels, the applications may very well fall in the realm of heavy industrial applications. Therefore, inverse parallel SCR's are in general more appropriate to provide the function of AC switching.

6.1 SERIES OPERATION OF SCR's

When circuit requirements dictate operation at a voltage in excess of the blocking voltage capabilities of a single SCR, series combinations can be employed if certain design precautions are taken. These precautions are primarily the equalization of voltage sharing, both forward and reverse, between individual SCR's at steady-state and transient operation conditions. Due to differences in blocking currents, junction capacitances, delay times, forward voltage drops as well as reverse recovery for individual SCR's, external voltage equalization networks and special consideration in gating circuits design are required.

6.1.1 Need For Equalizing Network

Shown in Figure 6.1 are hypothetical voltage / current characteristics for two randomly selected SCR's. If the two SCR's are connected in series one might expect them to have a total forward blocking capability of at least 2 (V_2). Yet without forced voltage equalization the total peak forward blocking voltage must be limited to approximately ($V_1 + V_2$) in order to keep the voltage across SCR_2 from exceeding $V_{(BO)2}$.

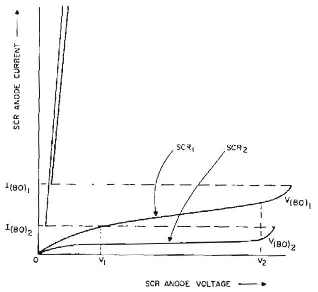


FIGURE 6.1 SCR CHARACTERISTICS

Figure 6.2 shows, diagramatically, the six operating states that can occure in a random sample of SCR's, connected in series, without forced equalization. It is seen that the equivalent individual impedances change continuously as the SCR series connection switches from state to state.

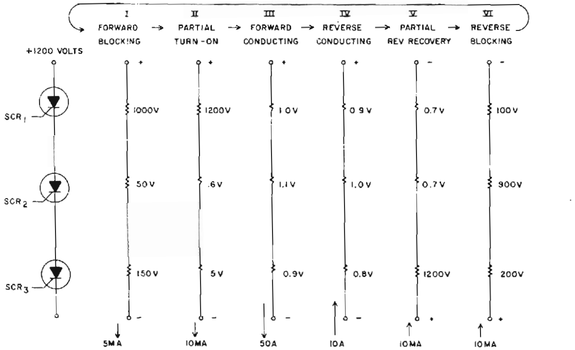


FIGURE 6.2 POSSIBLE OPERATING STATES OF AN UNEQUALIZED SERIES STRING OF SCR'S

During forward and reverse blocking states (I and VI) the difference in blocking characteristics result in unequal steady-state voltage sharing. This could be harmful to an SCR with inherently low blocking current since it might cause excessive voltage to appear across that SCR under blocking states. In order to equalize the voltage, a shunt resistor is connected across each SCR.

The conduction states (III and IV) represent no problem of voltage equalization.

States II and V represent undesirable unbalanced transient voltage sharing during turn-on and reverse recovery conditions.

In state II, the delay time of one SCR is considerably longer than other SCR's in the series string, consequently full voltage will be momentarily supported by the slow turn-on SCR. One method that can be taken to minimize unbalance caused by dissimilar turn-on delays is to supply high enough gate drive with fast rise time to minimize delay time differences. State V results from the fact that in a randomly chosen series string of SCR's, all SCR's will not recover at the time instant. The first cell to regain its blocking voltage capability will support the full voltage. To equalize the voltage during this period, a capacitor is connected across each SCR. If the impedance of the capacitor is low enough, and/or the time constant is properly chosen, the voltage buildup on the fastest SCR to recover is limited until the slowest one also recovers. This also alleviates the undesirable condition of state II.

In summary, states III and IV present no equalization problem. Shunt resistors equalize the voltage during states I and VI. Shunt capacitors equalize the voltage during states II and V. High gate-drive reduces inequalities during state II.

While capacitors provide excellent transient voltage equalization, they also produce high switching currents through the SCR's during the turn-on interval.[1,2] Switching currents can be limited by means of damping resistors in series with each capacitor. Although it is desirable to have a large value of R and therefore a small value of C to limit the power dissipation in the RC circuit, the value of the damping resistors must be kept to a reasonably low value in order not to reduce the effectiveness of the capacitors in equalizing voltage during the reverse recovery interval. Also, low values of damping resistance preclude excessive voltage build-up due to the IR drop during flow of reverse recovery current in the series connection after the first SCR has recovered.

Figure 6.3 shows the voltage equalization scheme described above.

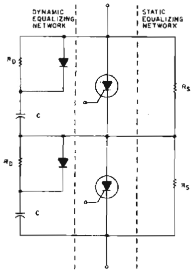


FIGURE 6.3 SERIES EQUALIZING ARRANGEMENT

Diodes can be placed across the damping resistors R_D to increase the effectiveness of the capacitors in preventing misfiring due to excessive rate of rise of forward voltage on the SCR's. Some small amount of damping resistance should still be used in series with the diode to prevent ringing.

It is cautioned that diodes should have soft recovery characteristics; otherwise, the abrupt recovery action of a snappy diode may produce an adverse effect, such as high voltage spikes and therefore hinder the performance of the RC circuits.[3,4]

6.1.2 Equalizing Network Design

6.1.2.1 Static Equalizing Network

For any given random group of SCR's there will be a given range of forward and reverse blocking current at given circuit conditions. Naturally, SCR's with low inherent blocking current will assume a greater portion of a steady state blocking voltage than will units with higher blocking current when all are connected in series. If the range of blocking current is defined as $I_b(max) - I_b(min) = \Delta I_b$, it is seen that the maximum unbalance in blocking voltage to SCR's of a series string occurs when one member has a blocking current of $I_b(min)$ and all remaining SCR's have $I_b(max)$. Figure 6.4 represents just such a case.

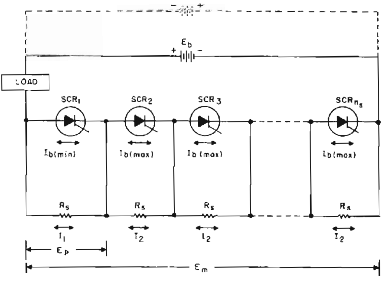


FIGURE 6.4 USE OF SHUNT RESISTORS TO EQUALIZE BLOCKING VOLTAGES TO SERIES SCR'S

Choose E_p as the maximum blocking voltage which we will allow across any one SCR. By inspection $I_1 > I_2$. Therefore:

$$E_p = I_1 R_s$$

Also:

$$E_m = E_p + (n_s - 1) R_s I_2$$

where:

E_m = peak blocking voltage to entire series string
n_s = number of SCR's in series string

$$I_2 = I_1 - \Delta I_b$$

$$E_m = E_p + (n_s - 1) R_s (I_1 - \Delta I_b)$$

$$= n_s E_p - (n_s - 1) R_s \Delta I_b$$

Now:

$$R_s \leqq \frac{n_s E_p - E_m}{(n_s - 1) \Delta I_b} \tag{6.2}$$

In general, only the maximum blocking currents for a particular SCR type are provided by the manufacturer. If one wishes to be conservative, I_b(min) can be assumed to be zero. The required value for R_s then becomes

$$R_s \leqq \frac{n_s E_p - E_m}{(n_s - 1) I_b(\max)} \tag{6.3}$$

Equalization resistors represent power consumers and as such it is desirable to use as large a resistance as possible. In a given group of SCR's, chances are good that one can select ΔI_b to be considerably less than I_b(max). For this reason the ΔI_b approach is recommended. When determining ΔI_b, it is best to measure blocking currents at maximum rated junction temperature and blocking voltage. After ΔI_b groups are selected, the ΔI_b should be checked at 25°C. To allow for differences in SCR temperatures when operating, a safety factor on ΔI_b should be used for design purposes.

Up to this point nothing has been said whether one must consider forward or reverse blocking current, or both. In general an SCR specification sheet gives one figure to cover both forward and reverse blocking current; when both are specified, they are usually the same.

Figure 6.5 is a useful aid for finding the required voltage equalizing resistance for series strings up to eight SCR's long. Enter the chart with a known E_m/E_p and read up to the curve designating the number of SCR's per string. Read across to find $\frac{R_s}{E_m/\Delta I_b}$. With a knowledge of E_m and ΔI_b, determine R_s(max).

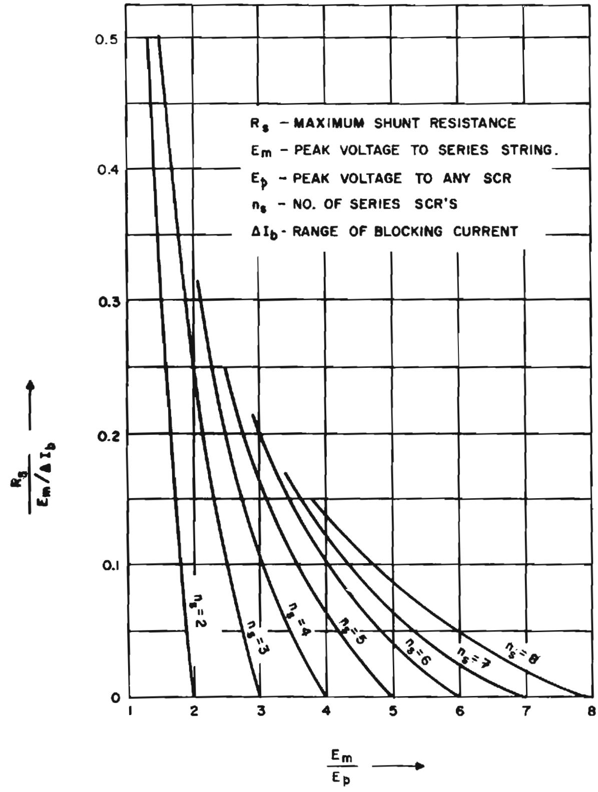
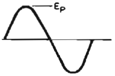


FIGURE 6.5 VOLTAGE EQUALIZING RESISTANCE FOR SERIES OPERATION OF SCR'S

To determine the power rating of the shunt resistors one must consider the resistor which experiences the highest peak voltage. The resistor effective power dissipation can be expressed as:

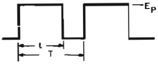
$$P_D = \frac{(E_{RMS})^2}{R_S} \tag{6.4}$$

For phase control applications the maximum power dissipation occurs at zero conduction angle:



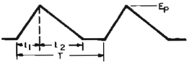
$$P_D = \frac{E_P{}^2}{2\,R_S} \tag{6.5}$$

For square wave applications:



$$P_D = \frac{E_P{}^2}{R_S}\left(\frac{t}{T}\right) \tag{6.6}$$

For triangle wave applications:



$$P_D = \frac{E_P{}^2}{3\,R_S}\left(\frac{t_1 + t_2}{T}\right) \tag{6.7}$$

6.1.2.2 Dynamic Equalizing Network

As mentioned earlier, shunt capacitors are required to limit rate of rise of voltage on the SCR's. Also during the reverse recovery interval such capacitors provide a reverse recovery current path for slow SCR's around those SCR's which recover first. Since the problem we are trying to correct arises from a difference in recovery characteristics within a given type of SCR we must take some time to discuss this characteristic.[3,4,5]

Two SCR's with a sizeable difference in reverse recovery current are depicted in Figure 6.6. The difference in the enclosed area is the differential charge (designated ΔQ).

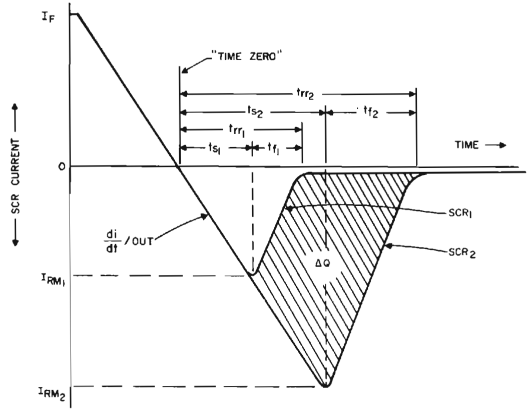


FIGURE 6.6 REVERSE RECOVERY CURRENTS FOR TWO UNMATCHED SCR'S OF THE SAME TYPE

Note that Figure 6.6 shows $t_{s2} > t_{rr1}$. This will not necessarily be true for two randomly chosen SCR's. However if one has two SCR's which represent the limit cases for a given type (i.e. worst case reverse recovery mismatch) then t_{s2} is generally greater than t_{rr1}. For design purposes this is a valid assumption.

Figure 6.7 shows current and voltage waveforms, during the reverse recovery interval, for two mismatched, series connected SCR's with shunt capacitors.

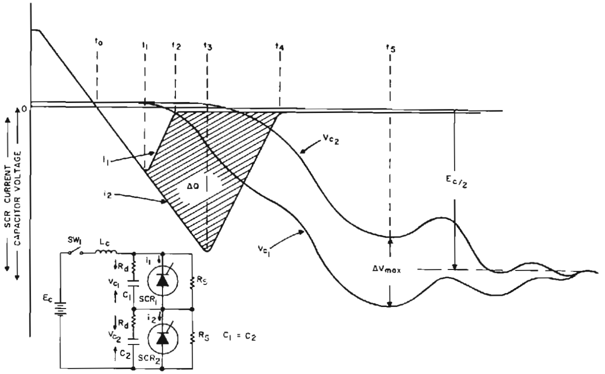


FIGURE 6.7 RECOVERY VOLTAGES OF CAPACITORS SHUNTING MISMATCHED, SERIES CONNECTED SCR'S

From t_0 to t_1 both SCR's present a short circuit to the flow of reverse current. Reverse current is applied at a rate determined by the commutating voltage E_c and the circuit commutating reactance L_c. During the period t_1 to t_2, capacitor C_1 begins to charge as SCR_1 begins to regain its blocking capability. The rate of charge of C_1 increases during this interval as the current in SCR_1 "tails-off." From t_2 to t_3 SCR_1 has fully recovered. The voltage and rate of charging C_1 further increases due to the increasing reverse current in SCR_2. At t_3, SCR_2 begins to recover and the current through SCR_2 begins to decrease thus reducing the charging rate of C_1. C_2 begins to charge as soon as SCR_2 begins to regain its blocking ability. At time t_4 both SCR's are fully recovered so that the only current path is through the capacitors. This means that at time t_4 the slopes of the voltage waveforms must be equal. From time t_4 on, the circuit behaves as a simple LRC circuit (C being a series combination of n discrete capacitors). Due to the difference in SCR recovery characteristics, the shunt capacitors when charged to peak voltage are not charged equally. The maximum difference in voltage is designated as ΔV_{max}. This ΔV_{max} can be simply represented by

$$\Delta V_{max} = \frac{\Delta Q_{max}}{C_x} \qquad (6.8)$$
$$x = 1, 2, 3 \ldots n$$

For steady state reverse blocking the shunt resistors share voltage to the designed degree. In Figure 6.7, the voltage difference between the two shunt capacitors varies from ΔV_{max} at t_5 to that determined by the shunt resistors at some time later than t_5. Assuming that the resistors share the steady state reverse voltage perfectly, ΔV after t_5 can be represented by:

$$\Delta V = \Delta V_{max}\, \epsilon - [t/R_sC] \qquad (6.9)$$
(time zero at t_5)

The worst combination of recovery characteristics for a series string of SCR's is with one fast recovery SCR and all the remaining ones being the slowest of that type. In this situation the peak voltages across the shunt capacitors are as follows:

$$V_C \text{ (fast SCR)} = (1/n_s)\,[E_C + (n_s - 1)\,\Delta V_{max}] \qquad (6.10)$$
$$V_C \text{ (slow SCR)} = (1/n_s)\,(E_C - \Delta V_{max})$$

Using relationships (6.8) and (6.10) and setting V_C (fast SCR) $= E_p$

$$C \geqq \frac{(n_s - 1)\,\Delta Q_{max}}{n_s E_p - E_C} \qquad (6.11)$$

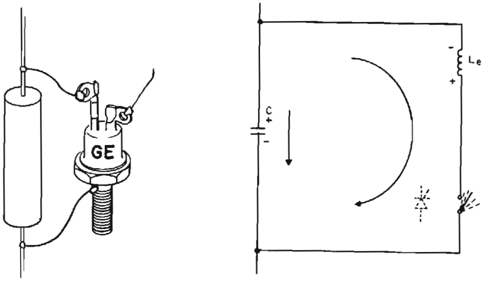
One might say: "This relationship for C is fine but how do I find ΔQ_{max} for a given type of SCR"? Following is a table of typical spread of ΔQ for some General Electric SCR types.

SCR	Related Types	ΔQ_{max} μCoulombs
C35	C36, C37, C38, C40	1
C137	C136	2
C139	C144	1
C140	C141	.5
C150	C350	30
C154	C155, C354, C355	18
C158	C358	22
C180	C380	45
C185	C385	20
C280	C281, C282, C283, C284	400
C290	C291, C600	340
C398	C387, C388, C397	40
C501	C601	400
C602		400

TABLE 6.1 TYPICAL RECOVERY CHARGE DIFFERENCE
$T_J = 125°C$ di/dt $= 10A/\mu s$

The reverse recovery charge is a function of both the device design characteristics and the circuit commutation conditions. By varying the commutation conditions, such as the magnitude of forward conduction current, circuit inductance and the device junction temperature, the recovery charge will vary accordingly. The values for ΔQ shown in Table 6.1 are for rated forward current at rated maximum junction temperature and a rate of reverse current of 10 A/μsecond. For detailed information other than specified, the reader is advised to refer to the individual SCR data sheets. The corresponding data sheet numbers are listed in Chapter 22.

Note that up to this point we have talked about voltages across the capacitors and tacitly assumed that such voltages are those on the SCR's. In practice this is usually not true. As shown in Figure 6.8 a certain amount of stray inductance is found in the physical capacitor-SCR loop.



(a) (b)

FIGURE 6.8 STRAY INDUCTANCE OF SCR-CAPACITOR LOOP

During the period t_f (Figure 6.8), current is changing in such a fashion as to set up a voltage in the stray inductance as shown. Realizing that this inductance is composed of wiring inductance, capacitor inductance and that inherent in the SCR, it is not hard to visualize, say, 1 μh in the loop. The induced voltage as shown represents additional reverse voltage to the SCR. During t_f the current can be changing at the rate of 200 amperes per microsecond when the commutation conditions are severe. This (with 1 μh) would mean an additional 200 volts reverse to the SCR. It cannot be overemphasized that the inductance of the capacitor-SCR loop should be held to as low a value as possible. For this reason GE extended foil capacitors are suggested.

Since the shunt capacitors discharge through the SCR's during turn-on, it is necessary to insert a small amount of resistance in series with each capacitor. The value of the resistance is chosen to limit the discharge current within the turn-on current limit of the SCR. Usually, the required value of resistance will fall between 5 and 50 ohms. In addition to limiting capacitor discharge current, high frequency oscillations due to interaction between the capacitors and circuit inductance are suppressed. It must be remembered that, although the damping resistance must be large enough to limit turn-on current and di/dt, it must not be so large that it either destroys the effect of the shunt capacitors or establishes an excessively high voltage during flow of reverse recovery current through it.

The value of this resistance can be estimated by the following formula:

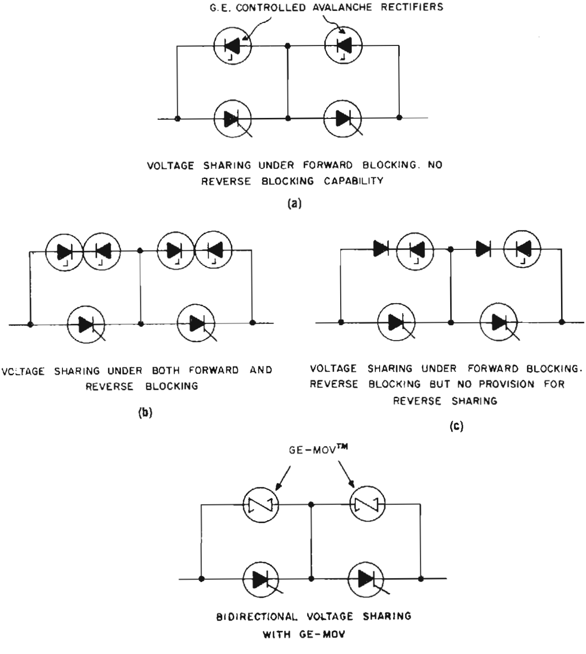
$$R_D = K\ C/L \qquad (6.12)$$

where K is a function of allowed overvoltage and circuit parameters[3] typical value is in the range of 1.25 to 1.5.

Methods of designing and selecting the proper damping resistor are discussed in Chapter 16.

6.1.2.3 Other Voltage Equalizing Arrangements

The arrangement of Figure 6.3 provides voltage sharing under all conditions of forward and reverse blocking. In applications where the increase in blocking losses due to current through the equalizing resistors must be avoided, as in SCR radar modulator switches, voltage sharing may be successfully accomplished by replacing each shunt equalizing network with a silicon controlled avalanche rectifier as shown in Figure 6.9(a). When maximum avalanche voltage is chosen correctly, total forward blocking current through the circuit need be only slightly higher than the maximum blocking current of the worst SCR. Maximum avalanche voltage of the shunt rectifier should be equal to, or slightly below, the SCR forward breakover voltage specifi-



VOLTAGE SHARING UNDER FORWARD BLOCKING. NO REVERSE BLOCKING CAPABILITY

(a)

VOLTAGE SHARING UNDER BOTH FORWARD AND REVERSE BLOCKING

(b)

VOLTAGE SHARING UNDER FORWARD BLOCKING. REVERSE BLOCKING BUT NO PROVISION FOR REVERSE SHARING

(c)

BIDIRECTIONAL VOLTAGE SHARING WITH GE-MOV

(d)

FIGURE 6.9 SERIES EQUALIZING USING CONTROLLED AVALANCHE RECTIFIER AND METAL-OXIDE VARISTORS

cation. Minimum avalanche voltage must be higher than E_m/n_s when measured at the controlled avalanche rectifier's minimum operating temperature. To provide optimum equalization it is desirable to have as narrow a tolerance as possible on the avalanche voltage of the shunt rectifier. Where a series string has to block appreciable reverse as well as forward voltage, inverse series controlled avalanche rectifiers may be substituted for the single units (see Figure 6.9(b)). In cases where reverse blocking requirements are not severe, some reverse blocking ability can be obtained using controlled avalanche rectifiers and conventional silicon rectifiers arranged as in Figure 6.9(c).

Figure 6.9(d) shows the shunt equalizing network utilizing a GE-MOV™ which provides a sharp voltage clip in both forward and reverse directions. The MOV™ functionally replaces two series connected avalanche diodes. Refer to Chapter 16 for more information regarding the GE-MOV.™

6.1.3 Triggering Series Operated SCR's

There are two primary methods in common use for triggering series SCR's, namely:

1. Simultaneous triggering
2. Slave triggering whereby one "master" SCR is triggered, and as its forward blocking voltage begins to collapse, a gate signal is thereby applied to the "slave" SCR.

Simultaneous triggering of all SCR gates is the preferred method. Slave triggering, while it is a unique way to provide gate isolation, produces some time delay between master and slave. Fortunately the capacitors used for voltage equalization during the reverse recovery period also limit the forward voltage rise. As long as the shunt capacitance is sufficient to limit forward voltage within the PFV ratings of the SCR's until all SCR's are "on," slave triggering can be reliably employed. The designer is cautioned to observe gate drive requirements of the SCR when employing slave triggering, particularly if switching into a fast rising anode current.

6.1.3.1 Simultaneous Triggering Via Pulse Transformer

When using pulse transformers particular attention should be given to the insulation between windings. This insulation must be able to support at least the peak of the supply voltage.

Triggering requirements may differ quite widely between individual SCR's. To prevent a cell with a low impedance gate characteristic from shunting the trigger signal away from a cell with a high impedance gate characteristic, resistance should be inserted in each gate lead, or impedance built into the transformer via leakage reactance, as shown by R_g in Figure 6.10.

Where the total energy available to trigger is limited, as may well be the case in a pulse triggering arrangement, it is preferable to replace these resistors with capacitors in series with each gate lead. Series capacitors tend to equalize the charge coupled to each SCR gate during trigger pulses, thus reducing the effects of unequal loading without

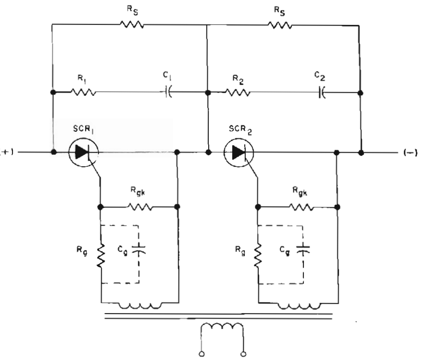


FIGURE 6.10 SIMULTANEOUS TRIGGERING OF SERIES CONNECTED SCR'S VIA PULSE TRANSFORMERS

additional energy dissipation. When capacitors are used in this manner a resistor, R_{gk}, should be connected from gate to cathode of each SCR to provide a discharge path for the capacitor. The circuit must be able to pass a fast rise time pulse, preferably less than 1 μsecond.

It must be emphasized again that marginal triggering is discouraged. Most SCR specification sheets today show a preferred triggering area on the gate characteristics curve. Particularly when switching into high currents, operation below this preferred area can be disastrous.

6.1.3.2 Simultaneous Triggering by Means of Light

Figure 6.11 shows an approach whereby simultaneous triggering of series connected SCR's is achieved by triggering LASCR's in the gate circuit of each SCR. This method of triggering provides the required gate isolation along with simultaneous turn-on when a single light source is used to turn on all LASCR's. The series combination of R_1 and R_2 is made equal to the required shunt resistance R_s. R_2 is made fairly small compared to R_1 so that low voltage LASCR's can be employed. The R_1C_1 time constant must be made sufficiently small so that C_1 is fully charged to the voltage dictated by R_2 at turn-on. Resistor R_4 limits the peak gate current. A useful trigger circuit (for LASCR's) employing Xenon flashtubes is shown in Figure 6.12. The circuit as shown operates well in the 60-400 Hz frequency range. The unijunction transistor relaxation oscillator provides alternate trigger pulses to the two C5 SCR's. As the C5 SCR's turn-on, the .22 μf capacitors discharge into the primaries of the high voltage trigger transformers thus providing approximately a 6 KV pulse at the flashtube. As the Xenon is ionized by this high voltage pulse the flashtubes conduct and emit a pulse of light. Refer to Chapter 14 for more detailed discussion of LASCR's and light couplers.

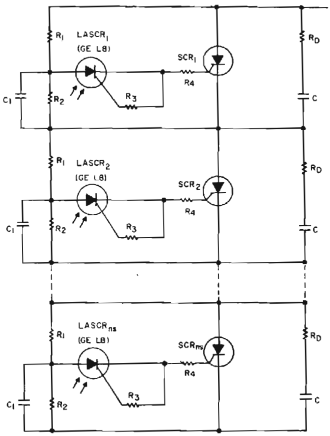


FIGURE 6.11 TRIGGERING OF SERIES CONNECTED SCR'S WITH LIGHT

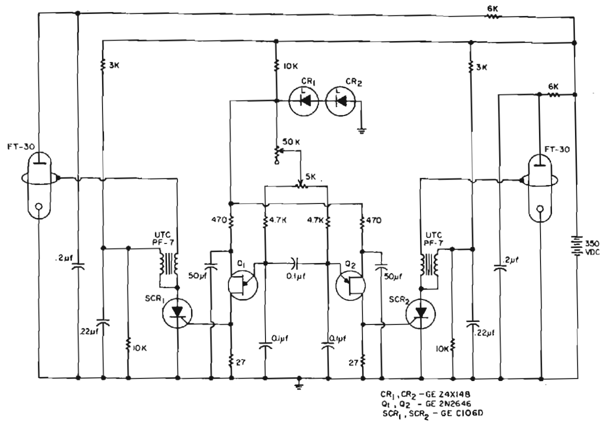


FIGURE 6.12 TRIGGER CIRCUIT FOR LIGHT TRIGGERING OF SERIES SCR'S

6.1.3.3 Slave Triggering for Series SCR's

Slave triggering is a technique for obtaining turn-on of more than one SCR by applying a trigger signal to only one SCR.[8,9] This approach, although a simple one to implement, has a rather serious limitation. Rather than simultaneous turn-on, one obtains staggered triggering so that total turn-on-time can be many times that of a single SCR. After the first few SCR's of a series string turn-on, the forward blocking voltage intended for the entire string must be supported by those units which have not yet switched. If the forward voltage to any one SCR exceeds its PFV rating, permanent damage to the SCR may result. The use of shunt capacitors tends to limit the rate of rise of forward voltage on the later SCR's to switch.

Figure 6.13 illustrates a slave triggering technique. A voltage equalizing network as previously described is connected across the cells. Only SCR_1 is directly triggered by the pulse source. The gate of SCR_2 is triggered by the surge of discharge current from capacitor C_1 when the voltage across SCR_1 decreases abruptly as it switches into conduction. Since the capacitor-resistor shunts, in conjunction with the SCR's present a balanced bridge to the zener, the triggering circuit to the SCR's is essentially insensitive to ordinary cyclical variations and transients from the supply voltage. In many cases the equalization network, optimized according to the procedure described earlier, will supply the required gate current to trigger. Rectifiers CR_2 and CR_3 can be paralleled with the damping resistors to inhibit triggering from dv/dt of the line voltage.

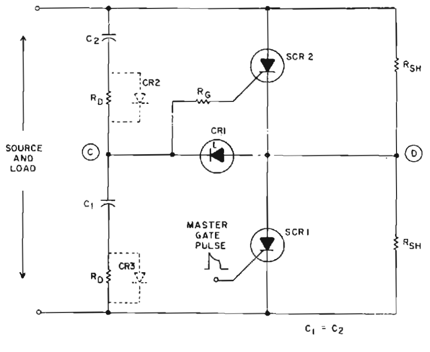


FIGURE 6.13 SERIES OPERATION OF SCR'S USING SLAVE TRIGGERING

The minimum capacitance required to supply sufficient gate current to trigger under all conditions is given by:

$$C_1 \geqq \frac{10}{R_G + \dfrac{V_{GT(max)}}{I_{GT(max)}}}\ \mu\,\text{fd} \qquad (6.13)$$

and

$$R_G = \frac{(V_z/2.7) - V_{GT(max)}}{I_{GT(max)}}\ \text{ohms} \qquad (6.14)$$

where V_z = nominal zener breakdown voltage of CR_1 (volts)
$I_{GT(max)}$ = maximum gate current to trigger under any of the circuit's operating conditions (milliamps)
$V_{GT(max)}$ = maximum gate voltage to trigger at $I_{GT(max)}$ (volts)

It is necessary that points C and D of Figure 6.13 be as closely balanced as possible. This is to prevent the flow of current in the bridge due to normal cyclical and transient variations of the supply voltage. Depending on the direction of an unbalance, a positive gate current to SCR_2 can result from either a falling or rising supply voltage. The slave triggering technique of Figure 6.13 is expandable to more than two SCR's in series.

Figure 6.14 shows another method of slave triggering series connected SCR's. Capacitors C_1, $C_2 \ldots C_n$ serve a dual purpose in this configuration. First, they provide transient voltage equalization and secondly they provide the slave triggering current at turn-on. As SCR_1 is triggered by the master signal, it begins to discharge capacitor C_1 through the gate of SCR_2 thus triggering SCR_2. As SCR_2 turns on capacitor C_2 begins to discharge through the gate of SCR_3, and so on. Resistors R_1, $R_2 \ldots R_{n-1}$ limit the SCR gate currents. Inductor L limits the di/dt to SCR_n. Figure 6.15 shows what overvoltage can be expected at each SCR during the turn-on interval when employing slave triggering. Overvoltage as used here is a percentage of E_p.

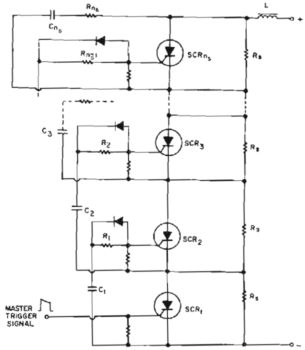


FIGURE 6.14 SLAVE TRIGGERING OF SERIES CONNECTED SCR'S

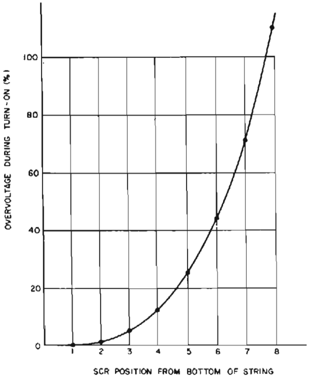


FIGURE 6.15 SCR OVERVOLTAGE AT TURN-ON WHEN SLAVE TRIGGERED VS SCR POSITION IN STRING

6.1.3.4 The Triggering Pulse

For series operation it is imperative to operate the gate well beyond the locus of minimum triggering (see Figure 4.13) in order to obtain turn-on in the minimum possible time. In addition, the pulse should have a very steep rise (ideally about 100 nanoseconds). The width of the pulse should be sufficient to insure that the SCR will latch into conduction under all operating conditions. If anode current swings momentarily to zero during the conducting cycle, the gate pulse must be maintained over the entire conduction period. The amplitude of the gate pulse should be the maximum permissible within the average and peak gate power dissipation ratings of the SCR.

6.2 PARALLEL OPERATION OF SCR's

When the demands for current handling capability to achieve load current requirements plus additional margins for overload and reliability purposes exceed the capability of the largest single SCR's presently available with the desired characteristics, the practice of paralleling SCR's becomes essential. The main consideration for operating SCR's in parallel is the equalization of forward conduction current through the parallel paths during both steady and dynamic states. When paralleling low resistance elements, variation in the magnetic flux linked by the parallel circuit can often be the most significant cause of unequal current balance. In SCR circuits, this general situation is further aggravated by any non-uniformity between SCR's forward

characteristics. Unequal current sharing can lead to a marked increase in the junction temperature of SCR's that are carrying a disproportionately large share of the total current. The temperature variation may further accentuate the characteristic differences, thus resulting in a thermal runaway condition.

6.2.1 SCR Transient Turn-On Behavior

Without considering external balancing, when paralleling cells the degree of success one obtains is limited by the degree of control the device designer is able to achieve on two key turn-on characteristics:[10] delay time, t_d, and the minimum turn-on voltage, V_{on}. The delay time can be interpreted as the time between application of gate signal and the actual turn-on of the SCR. The minimum turn-on voltage, sometimes referred to as the "finger" voltage, is the minimum forward anode voltage at which an SCR can be successfully turned-on with a trigger signal of sufficient magnitude. Differences in delay times can result in voltage unbalance during turn-on. Differences in finger voltages may prohibit the SCR with highest turn-on voltages to trigger. Figure 6.16 shows a hypothetical E-I curve for two SCR's with different finger voltages.

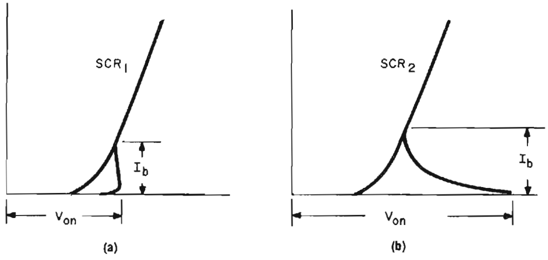
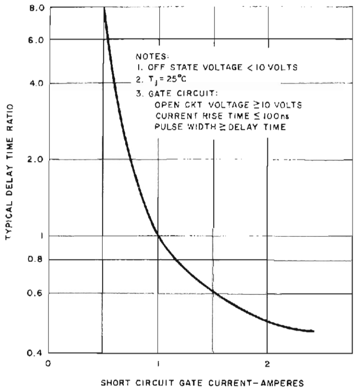


FIGURE 6.16 STATIC SCR GATE TURN-ON BEHAVIOR

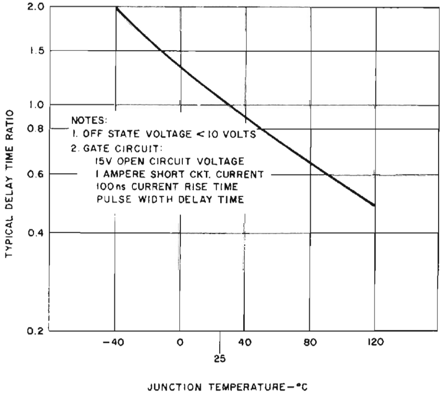
Obviously, if SCR_1 is connected directly in parallel with SCR_2 having identical characteristics, SCR_2 will never turn-on in applications requiring zero voltage triggering. When SCR_1 is switched on, the anode voltage of SCR_2 would be that of the on-state voltage of SCR_1, and consequently it will never equal or exceed the minimum required anode voltage to fire SCR_2 even if the width of the trigger pulse is greater than the delay time of the SCR. (Trigger requirements for parallel operation will be discussed in Section 6.3.5.)

Therefore, it is essential that in direct paralleling of SCR's, the forward characteristics of each and every cell must be properly matched.

Figure 6.17 shows the direction and roughly the magnitude of change in delay time vs gate current and junction temperature.



(a)



(b)

FIGURE 6.17 NORMALIZED DELAY TIME VS GATE CIRCUIT CURRENT & NORMALIZED DELAY TIME VS JUNCTION TEMPERATURE

Delay time has a negative coefficient with gate drive, temperature and switching voltage which can vary widely between types of SCR's. For SCR's exhibiting a strong dependence of switching voltage with delay time, direct paralleling of cells is fraught with danger. If two cells are connected in direct parallel with different delay times and if the switching voltage is low, the SCR with longer delay time may never be turned on. With sufficient switching voltage and trigger pulse wider than the delay time of the slow cell, even if turn-on of both cells is ensured, the turn-on current may not be shared as intended. In order to achieve the proper current sharing, certain remedial measures must be carefully undertaken. We shall discuss a few selected methods as listed below.

1. Direct paralleling using SCR's with matched forward characteristics.
2. External forced current sharing using SCR's with unmatched forward characteristics.

6.2.2 Direct Paralleling Using SCR's With Unmatched Forward Characteristics and No Sharing Networks

When forced current sharing is not employed, particular care must be taken to assure that impedance in series with each individual parallel path is maintained as nearly equal as possible. Wiring and connections should be uniform in all respects. The tendency for current to crowd to the outer branches or paths of a parallel network due to reactive effects is of particular significance at higher frequencies, and during the switching interval at the beginning and end of each conduction period. Mutual and self-inductance in series with each parallel path should be equalized where this phenomenon poses a problem.[11]

For direct parallel operation, SCR's with low and uniform turn-on voltages, closely matched forward E-I characteristics, and short delay times are desirable. Figures 6.18 and 6.19 illustrate the delay time and turn-on voltage spread of the C501 respectively.

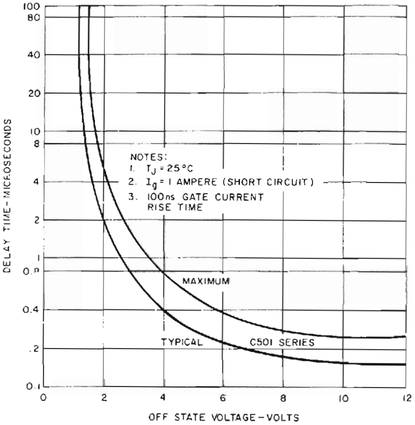


FIGURE 6.18 DELAY TIME VS OFF-STATE VOLTAGE

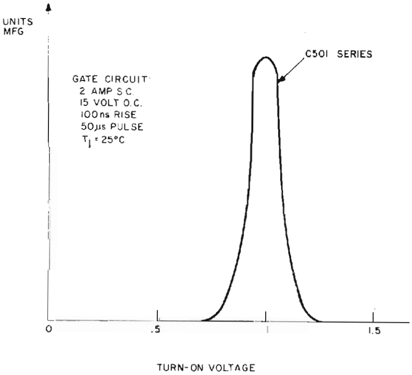


FIGURE 6.19 TURN-ON VOLTAGE DISTRIBUTION

Figure 6.20 is the on-state E-I characteristic curve of the C501. Similar uniform characteristics exist for the C600, C601 and C602 series.

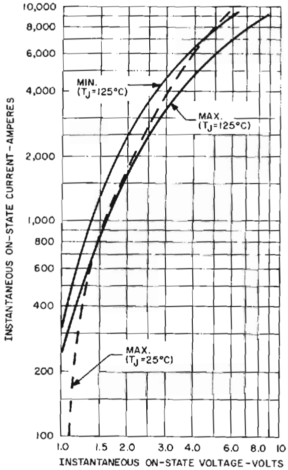


FIGURE 6.20 C501 FORWARD CONDUCTION CHARACTERISTICS

Use of factory assembled paralled cell heat exchangers provide for a high degree of uniformity in thermal and electrical parameters. A secondary benefit is minimum heat exchanger package size. For operation at maximum current levels water cooling is recommended.

Determination of derating factors using C501 SCR's will be undertaken using a design example with the G5 liquid cooled post as the heat exchanger. It is the basic building block of the G4 and G7 exchangers which allow direct paralleling, water cooling of 3 and 2 SCR's respectively.

Assume we have a three phase waveform. What average current can two unmatched C501 type SCR's handle? Begin by assuming that the SCR with the lowest V_T (call this device SCR_1) will be allowed to run at maximum rated junction temperature and nominal RMS current. For the type C501 SCR this is 125°C and 850 amperes respectively. For three phase operation we shall assume a rectangular current waveshape of 0.333 duty cycle. The RMS value for a rectangular waveshape is given by the following relationship

$$I_{RMS} = I_{PK} \sqrt{\text{Duty Cycle}}$$

For the type C501 SCR in a three phase circuit:

$$850 = I_{PK} \cdot \sqrt{0.333}$$

$$I_{PK} = 1470 \text{ amperes}$$

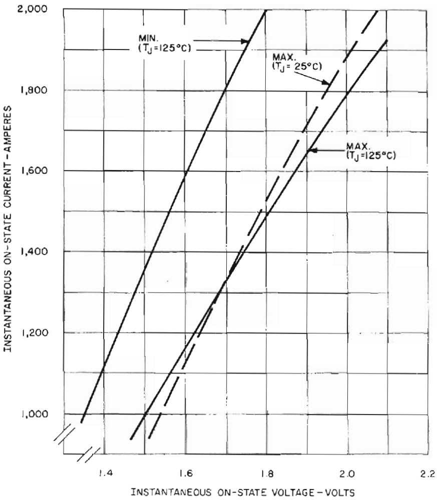


FIGURE 6.21 EXPANDED ON-STATE CHARACTERISTICS TYPE C501 SCR

During the "on" portion of the cycle, SCR_1 may conduct 1470 amperes. Remember that SCR_1 takes a disproportionate share of the total current. This is the SCR with the lowest on-state voltage drop at a given current and temperature among the SCR's of that type connected in parallel. SCR_1 is represented by the curve designated "min (T_j = 125°C)" in Figure 6.21. From this curve we may calculate the power dissipation in SCR_1 when conducting at maximum allowable junction temperature.

$$P_{diss(SCR_1)} = (I_{PK})\, V_T \text{ (Duty Cycle)} \tag{6.16}$$
$$= (1470)\,(1.55)\,(0.333) = 760 \text{ watts}$$

The problem now is to find how little current other SCR's in the cluster will conduct. As we have seen the on-state drop across the parallel combination must go no higher than that permitted by SCR_1 when conducting maximum RMS current at maximum rated junction temperature. For our assumed example this was 1.55 volts. Note now that two maximum on-state voltage drop curves are shown in Figure 6.21; one at T_j = 125°C and one at T_j = 25°C. With SCR_1 running at maximum rated junction temperature it follows that high-on-state drop units will be running at considerably cooler junction temperatures since they are conducting less current and hence dissipating less power.

It is seen that the lower the junction temperature the less the current conducted at the on-state voltage drop determined by SCR_1. Naturally, use of the $T_j = 25°C$ curve will give an ultraconservative estimate of the mismatch between units. Conversely, use of the $T_j = 125°C$ curve is inappropriate since it makes the degree of mismatch look better than it really may be. We must estimate at what temperature the junction of this device is operating and then check our estimate.

Assume, as an arbitrary starting point, that $T_j = 100°C$. Find the point (Figure 6.21) where $V_F = 1.55$ and is 25% of the way between the $T_j = 125°C$ and $T_j = 25°C$. We see that this occurs at a current of 1060 amps.

First we calculate at what temperature we must hold the water of the heat exchanger on which the SCR's are mounted. This is done from a knowledge of the power dissipated in SCR_1 and the maximum thermal resistance from junction to water. In order to find the lowest temperature at which the heat exchanger water must be held, we use maximum thermal resistance $R_{\Theta JA}$. For SCR type C501 mounted in the G5 heat exchanger post configuration

$R_{\Theta JA(3\phi)} = .085°C/watt$ (maximum)

J – Junction

A – Ambient Water

$$T_j - T_A = [P_{diss(SCR)1}] \times [\Theta_{JA(3\phi)}]$$
$$125°C - T_A = 760\ (0.085)$$
$$T_A = 125°C - 65°C$$
$$= 60°C$$

We see immediately that the junction temperature of SCR_2 will be higher than 60°C. We are interested in finding the lowest temperature any type C501 SCR will run.

The power dissipation in SCR_2 is

$$P_{diss(SCR_2)} = (1060)\ (1.55)\ (0.333)$$
$$= 548 \text{ watts}$$

In order to get the lowest probable junction temperature we must use minimum thermal resistances. Usually, minimum thermal resistances are not given on specification sheets. For the type C501 SCR mounted on a G5 post exchanger the following thermal resistance may be considered as a minimum value.

$$\Theta_{JA(3\phi)} = 0.08°C/watt$$

We can now compute the junction temperature of SCR_2.

$$T_j - T_A = P_{diss(SCR_2)} \times (\Theta_{JC(3\phi)}\ (min))$$
$$T_j - 60°C = 548 \times 0.08$$
$$= 44$$
$$T_j = 104°C$$

We see now that our first guess of $T_j = 100°C$ was a pretty good one and no further calculation is necessary. Naturally if our assumption did not correlate with the answer, a new assumption and interpolation would be necessary.

We can now formulate a general relationship for the maximum three phase average current that a parallel group of standard C501 SCR's can handle.

$$I_{AV(max)} = \frac{1470 + (n_p - 1)\,1060}{3} \qquad (6.17)$$

where n_p = number of C501 SCR's in parallel

If it is found that heat exchanger water temperature cannot be held at 60°C, then full current capability of SCR_1 cannot be realized. One must start with water temperature and adjust average current in SCR_1 to maintain junction temperature at +125°C.

It can be seen that in our example we have derated current 14% for parallel operation of two unmatched C501 SCR's. Section 6.2.3 defines "% parallel current derating."

If we had assumed single phase current rather than three-phase, the approach would be quite similar. Using the peak current in SCR_1, peak power is obtained from the "min (T_j = 125°C)" curve. For 180° half sine wave conduction, average power dissipation is given by the following empirical relationship:

$$P_{ave} = (0.286)\,P_{pk} \qquad (6.18)$$

The remainder of the calculation follows that outlined for the three phase example.

Note that all calculations have been made assuming the SCR's to be in full conduction. With a constant impedance load, if you are operating within SCR rating at full conduction, you will remain within rating as conduction angle is decreased. However, with a variable impedance load, particularly back EMF loads, required current at maximum retard angle is used to choose the proper SCR. Assuming operation at maximum allowable RMS current at 120° conduction angle, the average power dissipation is about 15% less than that at 180° conduction angle and full RMS rating. When phasing back to less than 120° conduction angle, *average* power dissipation decreases about 12-15% more for every additional 30° of retard down to 30° conduction angle. These rules-of-thumb are used to determine power dissipation in the one low-forward-voltage-drop cell for which the specification sheet rating curves do not apply. For all other cells (high-forward-voltage-drop units) the specification sheet curves apply.

6.2.3 Use of SCR's With Matched Forward Characteristics

As we have seen from Figures 6.20 and 6.21, the range of forward characteristics for a given SCR production line can be quite wide. If we define percent derating for parallel operation as follows

$$\%\ \text{Parallel Derating} = \left(1 - \frac{I_T}{n_p\, I_M}\right) \times 100\% \qquad (6.19)$$

where I_T = Total required load current through parallel arrangement

I_M = Maximum allowable current for a single cell operating alone

n_p = Number of cells in parallel

then we see that in our previous example of Section 6.2.2, 14% derating was required when operating two standard cells in parallel

$$\left(1 - \frac{1470 + 1060}{2 \times 1470}\right) \times 100\% = 14\%$$

In order to allow for less derating, General Electric supplies C501 type SCR's with matched characteristics. The matching is quantified by specifying a maximum on-state voltage spread or band. Figure 6.22 gives the relationship between band width, in millivolts at 1500 amps and 125°C, T_j, and % parallel current derating.

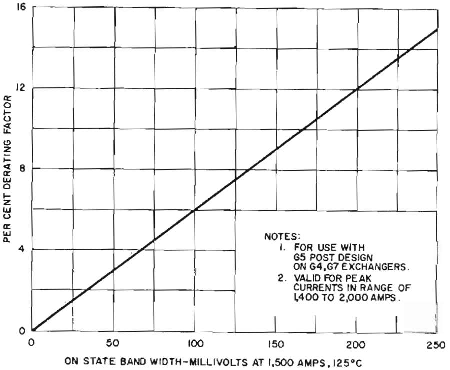


FIGURE 6.22 % PARALLEL CURRENT DERATING FACTOR FOR THE C501 SCR, FACTORY MOUNTED

The procedure for designing parallel arrangements with matched SCR's is quite similar to that outlined in Section 6.22 with the following possible exception. Since little derating usually accompanies the use of matched cells, all cells are operating near maximum rated junction temperature. As such the $T_j = 125°C$ forward characteristics can usually be used exclusively with very little error.

Figures 6.23 and 6.24 show two factory mounted liquid cooled heat exchanger assemblies available from General Electric with or without matched cells.

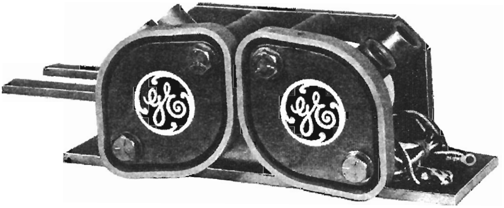


FIGURE 6.23 TWO C501'S IN PARALLEL MOUNTED IN A G-7 HEAT EXCHANGER

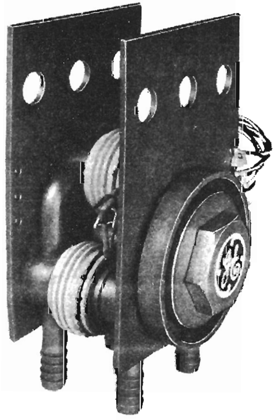


FIGURE 6.24 THREE C501'S IN PARALLEL MOUNTED IN A G-4 HEAT EXCHANGER

6.2.4 External Forced Current Sharing

If less than approximately 10% current derating is required when paralleling SCR's with unmatched forward characteristics, external forced sharing is required. Returning to our example of Section 6.2.2 we found that SCR_1 carried an average current of 490 amperes and SCR_2 carried 353 amperes giving a total capability of 843 amperes.

The maximum average capability of one cell is 490 amperes; it follows that with varying degrees of forced current sharing, one could approach about 950 average amperes for two cells in parallel. Let's see how we go about designing such an arrangement. Figure 6.25 shows such an arrangement. Let's assume we want to force share just enough to allow 950 amperes of 3 phase average current.

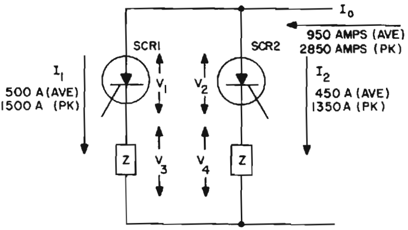


FIGURE 6.25 PARALLEL OPERATION OF SCR'S WITH FORCED SHARING

At ⅓ duty factor (three-phase operation) the current through the pair during the "on" portion of the cycle must be 2850 amperes. With 1500 amperes allowed in SCR_1, SCR_2 must handle 1350 amperes. Reading on-voltage from Figure 6.21, the relationship $V_1 + V_3 = V_2 + V_4$ can be solved.

$$V_1 + V_3 = V_2 + V_4 \tag{6.19}$$

$$1.56 + 1500\,Z = 1.71 + 1350\,Z$$

$$\therefore \quad Z = 1.0 \times 10^{-3} \text{ Ohms}$$

If resistors are used to effect the sharing, they will indeed be effective, but necessarily inefficient. In this example, the 1.0 milliohm resistor in series with SCR_1 will dissipate 250 watts.

Current sharing with reactors is a more efficient method than with resistors.[12] Figure 6.26 shows a 1:1 ratio reactor in bucking connection for two SCR's in parallel operation.

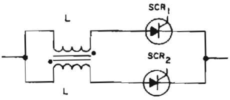


FIGURE 6.26 EXTERNAL FORCED CURRENT SHARING WITH PARALLEL REACTORS

If the current through SCR_1 tends to increase above the current through SCR_2, a counter EMF will be induced proportional to the

unbalanced current and tends to reduce the current through SCR_1. At the same instant, a boosting voltage is induced in series with SCR_2 increasing the current flow through the cell. When two matched cells are used, the magnetic flux balance each other and the core becomes unnecessary. The most important magnetic requirements of such a reactor are high saturation and low residual flux densities in order to provide as great a change in total flux each cycle as possible. An effectively designed balancing reactor will produce a peak voltage equal to the maximum overvoltage deviation of the two cells throughout the entire conduction period without saturating. In a single phase circuit the paralleling reactor should be able to support $\frac{\Delta V}{2f}$ volt-second without saturation where

f = supply frequency, Hz

ΔV = maximum on-state voltage mismatch between two SCR's

In a conservative estimation, ΔV equals .5 volt at peak load current.

Figure 6.27 and 6.28 illustrate how equalizing reactors can be used in paralleling odd and even numbers of SCR's.[13] These arrangements may be physically cumbersome and relatively expensive, but they are highly reliable when continuous operation under partial fault conditions must be provided.

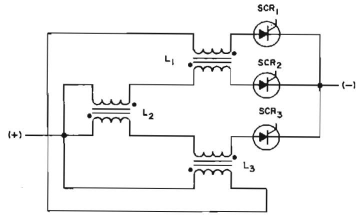


FIGURE 6.27 THREE SCR'S IN PARALLEL CONNECTION

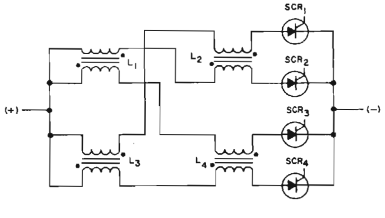


FIGURE 6.28 FOUR SCR'S IN PARALLEL CONNECTION

6.3 Triggering of Parallel Connected SCR's

If parallel SCR's are triggered from a common source, which is an essential requirement when switching high currents to large resistive or capacitive loads, each cell must be supplied with sufficient drive to exceed its own specific triggering needs. As previously pointed out, triggering requirements may differ quite widely between individual SCR's, whether or not units are parallel matched. As such the suggestions of Section 6.1.3 apply. In addition, it is necessary to drive the gate hard, regardless of the structure and sensitivity of the gate, commensurate with the peak and average gate power dissipation ratings in order to insure fast turn-on. This will help the SCR's to share the switching duty.

At low values of anode current the forward voltage-current characteristic changes from a positive to a negative resistance as current is reduced to the holding current. Below this value, the SCR will turn off by reverting to the forward blocking state. This transition point between positive and negative resistance is represented by the valley indicated in Figure 6.29, i.e., the current at which minimum forward voltage drop occurs. It is very difficult to match SCR's satisfactorily

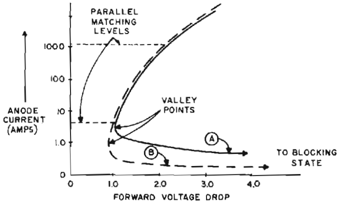


FIGURE 6.29 ANODE VOLTAGE-CURRENT RELATIONSHIP OF SCR'S WITH MATCHED FORWARD CHARACTERISTICS

for identical characteristics in this region, particularly over wide ranges of temperature. This poses no problem when the gate signal is supplied to the parallel SCR's throughout the anode conduction period, since any instability in current-sharing or a tendency of one SCR to turn off will not overheat the other device(s) in parallel because of the low current level in the region of the valley. As long as gate current is maintained, an SCR with a tendency to turn off at low anode current levels will switch into conduction again as soon as the total load current moves out of this valley area. It will thus assume its share of the load before overloading on its partner can occur. When a pulse type of gate signal is employed for triggering paralleled SCR's, instability may be encountered at low anode current levels which may have serious consequences if high levels of current follow. Pulsed gate signals are typical of unijunction transistor triggering circuits and some types of saturable reactor triggering schemes. Unless the total load current has reached a sufficiently high level to keep all of the parallel

cells above the valley point by the time the gate pulse is removed, a cells such as A in Figure 6.29 will turn off. In the absence of any further gate signal, it will remain in the non-conducting state through the remainder of that cycle, thus failing to carry its share of the load. This phenomenon is likely to occur when operating at very large conduction angles in phase controlled AC circuits and when triggering from reactive lines or into inductive loads where the buildup of load current to normal levels is restrained by the inductive effect.

For the above reasons use of a maintained gate signal is recommended for triggering parallel SCR's whenever possible.[14]

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13. "Parallel Operation of Silicon Rectifier Diodes," G. T. Tobisch, Mullard Technical Communications, Vol. 8, No. 73, October 1964.
14. "Phase Control of SCR's With Transformer and Other Inductive AC Loads," F. W. Gutzwiller and J. D. Meng, Application Note 200.31*, General Electric Company, Auburn, N. Y.

*Refer to Chapter 23 for availability and ordering information.

NOTES

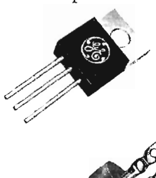
7 THE TRIAC

7.1 DESCRIPTION

"TRIAC" is an acronym that has been coined to identify the *tri*ode (three-electrode) *AC* semiconductor switch which is triggered into conduction by a gate signal in a manner similar to the action of an SCR. The triac, generically called a Bidirectional Triode Thyristor, first developed by General Electric (patent No. 3,275,909 and others applied for), differs from the SCR in that it can conduct in both directions of current flow in response to a positive or negative gate signal.

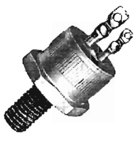
The primary objective underlying development of the triac was to provide a means for producing improved controls for AC power. The use of SCR's has proven the technical feasibility and benefits of the basic functions of solid-state switching and phase-control. In many cases, however, use of these functions has been limited by cost, size, complexity, or reliability. The triac development was based upon a continuing study of various ways for improving overall feasibility of the basic functions, including evaluation of circuits and components. To this end, the development appears to have been notably successful, particularly in the most simple functions.

At this time triacs are available from General Electric in current ratings up to 25 amperes and voltages to 500 volts. These devices are available in four different packages as shown in Figure 7.1. Triacs are rated for both 50-60 Hz and 400 Hz. For abbreviated specifications of these devices see Chapter 22.



(a) Molded Silicone Plastic, TO-220. Available in 6 and 10 Amperes.

PRESS-FIT



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ISOLATED STUD

(b) Metal Can Versions. Available in 3, 6, 10, 15 and 25 Ampere Types.

FIGURE 7.1 TRIAC PACKAGES

7.1.1 Main Terminal Characteristics

The basic triac structure is shown in Figure 7.2(a). The region directly between terminal MT_1 and terminal MT_2 is a p-n-p-n switch in parallel with an n-p-n-p switch. The gate region is a more complex arrangement which may be considered to operate in any one of four modes: direct gate of normal SCR; junction gate of normal SCR; remote gate of complementary SCR with positive gate drive; and remote gate of complementary SCR with negative gate drive. For more detailed explanation of triac operation, see Section 7.2.

Figure 7.2 also shows the triac symbol, oriented in proper relationship to the structure diagram. Note that the symbol, although not fully definitive, is composed of the popularly accepted SCR symbol, combined with the complementary SCR symbol. Since the terms "anode" and "cathode" are not applicable to the triac, connections are simply designated by number. Terminal MT_1 is the reference point for measurement of voltages and currents at the gate terminal and at terminal MT_2.

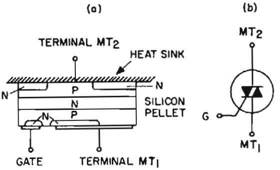


FIGURE 7.2 THE TRIAC; (A) SIMPLIFIED PELLET STRUCTURE, (B) CIRCUIT SYMBOL

The AC volt-ampere characteristic of the triac, Figure 7.3, is based on terminal MT_1 as the reference point. The first quadrant, Q-I, is the region wherein MT_2 is positive with respect to MT_1 and vice versa for Q-III. The breakover voltage, $V_{(BO)}$, in either quadrant (with no gate signal) must be higher than the peak of the normal AC waveform applied in order to retain control by the gate. A gate current of specified amplitude of either polarity will trigger the triac into conduction in either quadrant, provided the applied voltage is less than $V_{(BO)}$. If $V_{(BO)}$ is exceeded, even transiently, the triac will switch to the conducting state and remain conducting until current drops below the "holding current," I_H. This action provides inherent immunity for the triac from excessive transient voltages and generally eliminates the need for auxiliary protective devices. *In some applications the turning on of the triac by a transient could have undesirable or hazardous results on the circuit being controlled, in which case transient suppression is required to prevent turn-on, even though the triac itself is not damaged by transients.*

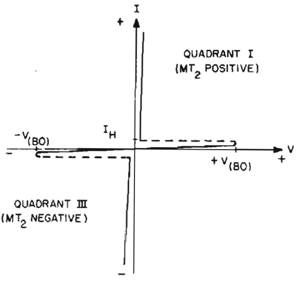


FIGURE 7.3 AC VOLT-AMPERE CHARACTERISTIC OF THE TRIAC

Triac current ratings are based on maximum junction temperature, similar to SCR's. The current rating is determined by conduction drop, i.e., power dissipation, and thermal resistance junction to case, and is predicated on proper heatsinking. If the case temperature is allowed to go above its rated value, as determined from the specification sheet, the triac can no longer be guaranteed to block its rated voltage, or to reliably turn off when main terminal current goes through zero. For more details on current ratings of SCR's and triacs, see Chapter 3. For information on proper heatsink design, see Chapter 18.

For inductive loads, the phase-shift between line current and line voltage means that at the time that current drops to the I_H value and the triac changes to the non-conducting state, a certain line voltage exists which must then appear across the triac. If this voltage appears too rapidly, the triac will immediately resume conduction. In order to achieve proper commutation with certain inductive loads, the dv/dt must be limited by a series RC circuit in parallel with the triac, or current, voltage, phase-shift, or junction temperature reduced. For further information on the use of triacs with inductive loads, see Section 7.1.4.

7.1.2 Gate Triggering Characteristics

Since the triac may be triggered with low energy positive or negative gate current in both the first and third quadrants, the circuit designer has a wide latitude for selection of the control means. Triggering can be obtained from DC, rectified AC, AC, or pulse sources such as unijunction transistors, neon lamps, and switching diodes such as the ST-2 "diac," the silicon bilateral switch (SBS), and the asymmetrical trigger switch (ST-4).

The triggering modes for the triac are:

MT2+, Gate+; I+; First quadrant, positive gate current and voltage.

MT2+, Gate−; I−; First quadrant, negative gate current and voltage.

MT2−, Gate +; III+; Third quadrant, positive gate current and voltage.

MT2−, Gate−; III−; Third quadrant, negative gate current and voltage.

The sensitivity of the triac, at present, is greatest in the I+ and III− modes, slightly lower in the I− mode, and much less sensitive in the III+ mode. The III+ mode should not be used, therefore, unless special circumstances dictate it. In such a case, triacs which have been specially selected for the application are available and should be specified.

The V-I characteristics of the triac gate shows a low non-linear impedance between gate and terminal MT_1. The characteristic is similar to a pair of diodes connected in a inverse parallel configuration. Since in any given mode this characteristic is similiar to an SCR gate, the gate requirements are rated exactly like SCR's. For details on gate trigger ratings, see Chapter 4.

7.1.3 Simplified Triac Theory

Four basic thyristor concepts provide a foundation for the theory of bidirectional thyristor operation. These concepts are:

a) The basic reverse blocking triode thyristor (or SCR)
See Section 1.4.

b) The shorted emitter thyristor
See Section 1.5.

c) Junction gate thyristor

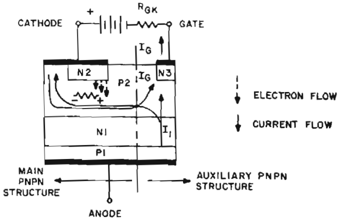


FIGURE 7.4 JUNCTION GATE THYRISTOR

Figure 7.4 shows a typical junction gate thyristor structure. Initially, gate current I_G forward biases the gate junction p_2-n_3 of the auxiliary p_1-n_1-p_2-n_3 structure, and this structure turns on in conventional p-n-p-n fashion. As p_1-n_1-p_2-n_3 turns on, the voltage drop across it falls, and the *right hand section* of region p_2 moves towards anode potential. Since the *left hand section* of p_2 is clamped to cathode potential, a transverse voltage gradient now exists across p_2, and current flows laterally through p_2. As the right hand edge of p_2-n_2 becomes forward biased, electrons are

injected at this point and the main structure turns on (compare this action to that of the shorted emitter structure).

d) Remote gate thyristor

A remote gate thyristor is one that can be triggered without an ohmic contact to either of its internal base regions. Figure 7.5 depicts a typical remote base structure.

The external gate current I_G causes p_1-n_3 to become forward biased, and inject electrons as shown. These electrons diffuse through region p_1 and are collected by junction p_1-n_1. Note that junction p_1-n_1 can still act as a collector even though it is forward biased,[4] since the electric field associated with it is in the same

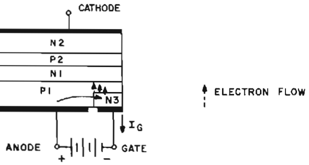


FIGURE 7.5 REMOTE GATE THYRISTOR

direction as it would be if p_1-n_1 were reverse biased, as a "collector" normally is. The electrons from n_3 collected by p_1-n_1 cause an increase of current across p_1-n_1, regeneration starts, and the structure turns on.

The salient features of the four devices just described can be combined into a single device—the "triac"—which can block voltage in either direction, conduct current in either direction, and be triggered on in either direction by positive or negative gate signals. Figure 7.6 is a pictorial view of a typical device. Operation is as follows:

a) Main terminal #2 positive, positive gate current

In this mode the triac behaves strictly like a conventional thyristor. Active parts are p_1-n_1-p_2-n_2.

b) Main terminal #2 positive, negative gate current

Operation is analogous to the junction gate thyristor. p_1-n_1-p_2-n_2 is the main structure, with n_3 acting as the junction gate region.

c) Main terminal #2 negative, negative gate current

Remote gate mode. p_2-n_1-p_1-n_4 is the main structure, with junction p_2-n_3 injecting electrons which are collected by the p_2-n_1 junction.

d) Main terminal #2 negative, positive gate current

p_2-n_2 is forward biased and injects electrons which are collected by p_2-n_1. p_2-n_1 becomes more forward biased. Current through the p_2-n_1-p_1-n_4 portion increases and this section switches on. This mode, too, is also analogous to remote gate operation. Reference 1 gives a more detailed description of triac triggering.

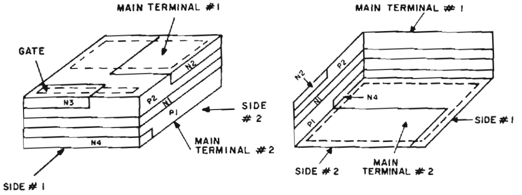


FIGURE 7.6 TYPICAL TRIAC STRUCTURE

7.1.4 Commutation of Triacs

One important difference between use of a pair of SCR's and use of a triac in an A-C circuit is that with SCR's each SCR has an entire half cycle to turn off, while the triac must turn off during the brief instant while the load current is passing through zero. For resistive loads this is fairly simple to accomplish since the time available for the triac to turn-off extends from the time the device current drops below holding current until the reapplied voltage exceeds the value of line voltage required to allow latching current. With inductive loads the task of commutating the triac becomes more difficult.

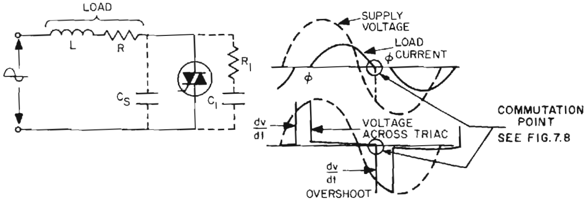


FIGURE 7.7 INDUCTIVE LOAD WAVEFORMS

Figure 7.7 shows the triac voltage and current waveforms for a typical inductive load circuit. If we were to examine the waveforms at the current zero (i.e., at the turn-off point), a waveform such as Figure 7.8 would be found.

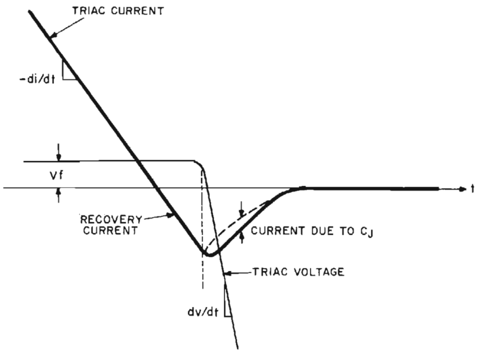


FIGURE 7.8 TRIAC CURRENT AND VOLTAGE AT COMMUTATION

It can be seen from the current waveform in Figure 7.8 that the recovery current is acting as a virtual gate current and trying to turn the device back on. In addition there is a component to the reverse current which is due to the junction capacitance and the reapplied dv/dt. This component directly adds to the recovery current but does not appear until the triac begins to block the opposite polarity.

Section 3.13 discusses the reverse recovery phenomenon in SCR's. As the rate of removal of current (—di/dt) decreases, the recovery current also decreases. This then implies that at lower di/dt's, higher reapplied dv/dt's are permissible for a given commutation capability.

An example of such a relationship is shown in Figure 7.9. If the dv/dt is above this value then additional protection circuits must be incorporated. The standard method is to use an R-C snubber such as R_1, C_1 in Figure 7.7. The values of R_1 and C_1 are a function of the load, line voltage and triac used. For aid in the choice of R_1 and C_1, Section 16.3 covers the subject in greater detail.

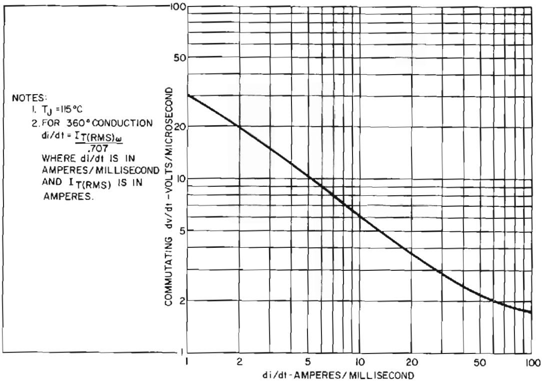
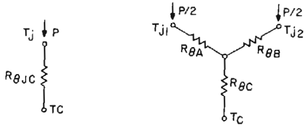


FIGURE 7.9 TYPICAL RATE OF REMOVAL OF CURRENT (di/dt) EFFECT UPON COMMUTATING dv/dt FOR SC60/61 TRIACS

7.1.5 Triac Thermal Resistances



(a) JEDEC Thermal Resistance (b) Triac Effective Thermal Resistance

FIGURE 7.10 THE TWO DIFFERENT TRIAC THERMAL RESISTANCES

On GE triac data sheets two different thermal resistance values are specified for the same device. This at first sounds impossible, but consider what these two numbers mean and why they're there.

1) JECEC Thermal Resistance

This thermal resistance specification, usually found in the Characteristics Table of GE Triac Spec Sheets, is a thermal characteristic specified by JEDEC for purposes of establishing device interchangeability. It is the value obtained by measuring the peak junction temperature rise, above the case reference point, produced by a unidirectional DC power being dissipated in the device. The conduction direction for which this thermal resistance

value applies is the one that yields the highest value, assuming that the thermal characteristic is not quite the same for both conduction directions.

2) Apparent Thermal Resistance

A triac is generally used in AC applications, and consequently, the JEDEC unidirectional thermal resistance value would yield a somewhat conservative device AC current rating when using it in the current maximum case temperature rating calculations. To overcome this, GE establishes an "apparent" thermal resistance value which when multiplied by the average power, produced by a full sinewave of current of specified frequency, yields the instantaneous junction temperature at the end of each half cycle of current conduction. The current rating is so established that this value of instantaneous junction temperature is the maximum rated value for the device. This assures that the device is ready to block full rated off-state voltage (within dv/dt limitations) following any half cycle current conduction interval.

This "apparent" thermal resistance of the triac can be represented by a "Y" model as shown in Figure 7.10(b). The branches of the Y ($R_{\theta A}$, $R_{\theta B}$) each represent the thermal resistance of approximately half of the silicon element (operation for one polarity of circuit current). The common leg of the Y represents the thermal resistance of the package base from the point of silicon element attachment to the reference point (T_C). GE also establishes an apparent transient thermal impedance curve for use in AC overload current calculations. Again the average power produced by any given number of full cycles of AC current multiplied by the corresponding value of thermal impedance taken from the curve will yield the instantaneous junction temperature at the end of the appropriate half cycle current conduction interval.

7.2 USE OF THE TRIAC

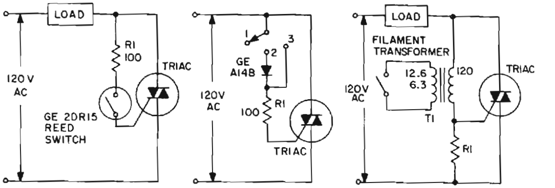
The versatility of the triac and the simplicity of its use make it ideal for a wide variety of applications involving AC power control.

7.2.1 Static Switching

The use of the triac as a static switch in AC circuits gives many definite advantages over mechanical switching. It allows the control of relatively high currents with a very low power control source. Since the triac "latches" each half cycle, there is no contact bounce. Since the triac always opens at current zero, there is no arcing or transient voltage developed due to stored inductive energy in the load or power lines. In addition, there is a dramatic reduction in component count compared to other semiconductor static switches.

The most striking example of circuit simplification is seen in the elementary static switch shown in Figure 7.11(a). The glass-enclosed magnetic reed switch provides many million operations from a perma-

nent magnet or from a DC electromagnet "relay" coil. Since the contacts only handle current during the few microseconds required to trigger the triac, a wide variety of small switching elements may be used in place of the reed switch, such as relays, thermostats, pressure switches, and program/timer switches. In many cases, snap action of triggering contacts can be eliminated, thus reducing their cost as well. This circuit uses gate triggering modes MT2+, Gate+ and MT2−, Gate−. Figure 7.11(b) shows the use of a low current diode in series with the surge limiting resistor, and a three position switch, to obtain



BASIC STATIC SWITCH (a) — 3 POSITION STATIC SWITCH (b) — ISOLATED LOW VOLTAGE CONTROL (c)

FIGURE 7.11 STATIC AC SWITCHING APPLICATIONS OF THE TRIAC

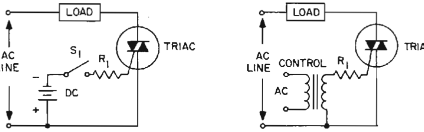
a simple 3 position power control. In position one, there is no gate connection, and the power is off. In position two, gate current is allowed in one half cycle only, and the power in the load is half-wave. In position three, there is gate current for both half cycles, and the power is on full. As shown in Figure 7.11(c), the switch can be replaced by a transformer winding. This circuit makes use of the difference in primary impedance between the open circuit and shorted secondary cases. The resistance R is chosen to shunt the magnetizing current of the primary to ground. This circuit provides control with isolated low voltage contacts.

Resonant-reed relays have also been used with the triac in the circuit of Figure 7.11(a) to provide very sharp frequency-selective switching in response to coded audio input signals in multi-channel operations. At the lower frequencies some modulation of triggering point results from beating with line frequency.

Other useful switching circuits are shown in Figure 7.12, showing DC and AC triggering for the triac. Switch S_1 may be replaced by a transistor which is controlled by a thermistor or a photocell, or other electrical signal as shown in Figure 7.13. The AC signal of Figure 7.12(b), could be 60 Hz if phased properly to trigger early in each half cycle of the supply wave. Higher frequencies, above 600 Hz, are also effective and reduce the size of T, but produce very slight irregularities in triggering point, which are usually negligible. Frequency selectivity may be obtained by tuning T or by use of other static or dynamic filter circuits for remote-control work or for tape-recorder programming of a system. In any case the trigger signal should be significantly ON or OFF since the trigger sensitivity of the triac is not quite uniform in both polarities or both quadrants and should not be used, therefore, as a threshold detector.

The transistor connections of Figure 7.13 are ideal for driving the triac, or an array of triacs, from a low level DC logic source. One example of this is illustrated by Figure 7.14 which shows two triacs being driven by a transistor flip-flop circuit in an AC power flasher arrangement.

For further informative details on static switching, see Chapter 8.



(a) DC CONTROL (b) AC CONTROL

FIGURE 7.12 ELECTRICALLY ACTUATED AC STATIC SWITCHES

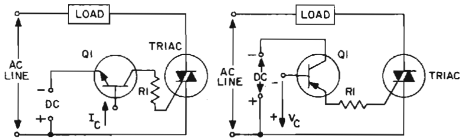


FIGURE 7.13 TRANSISTOR GATING CONTROL

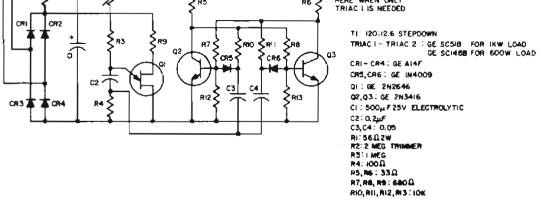


FIGURE 7.14 A-C POWER FLASHER. TRIACS 1 AND 2 ALTERNATE THEIR ON-STATE AT A FREQUENCY DETERMINED BY THE SETTING OF R2

7.2.2 Firing With a Trigger Diode

Only four components are required to form the basic full wave triac phase control circuit shown in Figure 7.15. Adjustable resistor R_1 and capacitor C_1 are a single-element phase-shift network. When

the voltage across C_1 reaches breakover voltage, $V_{(BO)}$, of the diac, a bi-directional trigger diode, C_1 is partially discharged by the diac into the triac gate. This pulse triggers the triac into the conduction mode for the remainder of that half-cycle. Triggering is in the I+ and III− modes in this circuit. Although this circuit has a limited control range, and a large hysteresis effect at the low-output end of the range, its unique simplicity makes it suitable for many small-range applications such as lamp, heater and fan-speed controls.

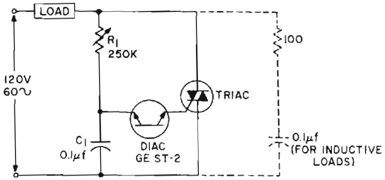


FIGURE 7.15 BASIC DIAC-TRIAC PHASE CONTROL

To eliminate some of the problems of this basic circuit, more sophisticated circuits are generally used where the full control range is required. Other types of bidirectional trigger diodes, such as the Asymmetrical Trigger Switch (ST-4) may also be used. More details on this type of firing circuit will be found in Chapter 9.

7.2.3 Other Triggering Methods

In addition to the diac (ST-2) and ATS (ST-4) mentioned above, devices such as the Unijunction Transistor and Programmable Unijunction Transistor can also be used as triac triggers. Chapters 4 and 9 outline methods for proper circuit designs using these devices.

General Electric also has developed two integrated circuit triggers for triacs. The first of these is the GEL300, Zero Voltage Switching Integrated Circuit. With this IC, a triac and four outboard components, a precision temperature control can be built. This IC and its uses are covered in depth in Chapters 11 and 12.

The second IC is the GEL301, Integrated Phase Control. This circuit is designed for high gain, feedback, phase control systems. A description of this IC, along with several examples of its use are covered in Section 9.7 and Chapter 10.

7.3 TRIAC CIRCUITRY

In general triac circuitry is the same as that of other thyristors. Scattered throughout Chapters 8, 9, 10, 11, 12 and 14 are many examples of triac circuits. In designing triac circuits it is necessary to keep in mind the unique characteristics of triacs. Below is a short check list

of those things unique to triacs. These items should be added to those of Chapter 21 when triacs are used.

1) Commutating—Has adequate arrangement been made to guarantee commutation?
2) Gate Trigger Modes—Has the system been designed so that variations in sensitivity between trigger modes will not affect system performance?

REFERENCES

1. Gentry, Scace and Flowers, "Bidirectional Triode P-N-P-N Switches," Proceedings of IEEE, April 1965.
2. "Solid State Incandescent Lighting Control," R. W. Fox, Application Note 200.53, General Electric Company, Syracuse, N. Y.*
3. "Using the Triac for Control of AC Power," J. H. Galloway, Application Note 200.35, General Electric Company, Syracuse, N. Y.*
4. J. F. Essom, "Bidirectional Triode Thyristor Applied Voltage Rate Effect Following Conduction," Proceedings of the IEEE, August 1967, pp. 1312-1317.
5. R. J. Buczynski, "Commutating dv/dt and its Relationship to Bidirectional Triode Thyristor Operation in Full-Wave AC Power Control Circuits," IEEE Conference Record of 1967 IGA Second Annual Meeting, pp. 45-49.

*Refer to Chapter 23 for availability and ordering information.

NOTES

8 STATIC SWITCHING CIRCUITS

8.1 INTRODUCTION

Since the SCR and the triac are bistable devices, one of their broad areas of application is in the realm of signal and power switching. This chapter describes circuits in which these thyristors are used to perform simple switching functions of a general type that might also be performed non-statically by various mechanical and electromechanical switches. In these applications the thyristors are used to open or close a circuit completely, as opposed to applications in which they are used to control the magnitude of average voltage or energy being delivered to a load. These latter types of applications are covered in detail in succeeding chapters.

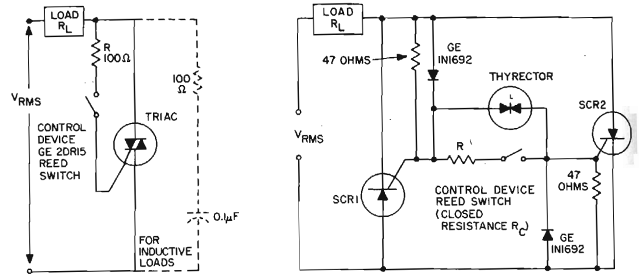
Static switching circuits can be divided into two main categories: AC switching circuits and DC switching circuits. AC circuits, as the name implies, operate from an AC supply and the reversal of the line voltage turns a thyristor off. Since most triacs are designed for 50-400 Hz operation, applications at higher frequency would dictate the use of two SCR's in inverse-parallel connection. The maximum frequency of operation of SCR's however is limited to approximately 30 K Hz by the turn-off time requirement of the SCR. Above these frequencies the SCR's may not recover their blocking ability between successive cycles of the supply. DC switching circuits on the other hand operate from a DC (or a rectified and filtered AC) source and an SCR must be turned off by one of the methods described in Chapter 5. In applications where the circuit turn-off time is limited, special inverter type SCR's (see Chapter 22) may be required. These types have tested maximum turn-off time specifications.

8.2 STATIC AC SWITCHES

8.2.1 Simple Triac Circuit and Inverse-Parallel ("Back-to-Back") SCR Connection

The circuits of Figure 8.1 provide high speed switching of AC power loads, and are ideal for applications with a high duty cycle. They eliminate completely the contact sticking, bounce, and wear associated with conventional electromechanical relays, contactors, etc. As a substitute for control relays, thyristors can overcome the differential problem, that is the spread in current or voltage between pickup and dropout, because thyristors effectively drop out every half-cycle. Also, providing resistor R is chosen correctly, the circuits are operable over a much wider voltage range than is a comparable relay. Resistor R is provided to limit gate current peaks. Its resistance (which can include

any "contact" resistance of the control device and load resistance) should be just greater than the peak supply voltage divided by the peak gate current rating of the SCR. If R is made too high, the SCR's may not trigger at the beginning of each cycle, and "phase control" of the load will result with consequent loss of load voltage and waveform distortion. The control device indicated can be either electrical or mechanical in nature. Light dependent resistors and light activated semiconductors, photocouplers (see Chapter 14 where normally open and normally closed light activated relays are shown), magnetic cores, and magnetic reed switches are all suitable control elements. In particular, the use of hermetically sealed reed switches as control elements in combination with SCR's and triacs offers many advantages. The reed switch can be actuated by passing AC or DC current through a small winding around it, or by the proximity of a small magnet. In either case complete electrical isolation exists between the control signal input, which may be derived from many sources, and the switched power output. Long life is assured the SCR or triac/reed switch combination by the minimal volt-ampere switching load placed on the reed switch by the SCR or triac triggering requirements. The thyristor ratings determine the amount of load power that can be switched.



$R \geq \frac{\sqrt{2} \cdot V}{I_{GM}} - (R_L + R_C)$ WHERE I_{GM} IS PEAK GATE CURRENT RATING OF SCR

(a) Basic Triac Static Switch **(b) Inverse-Parallel SCR'S**

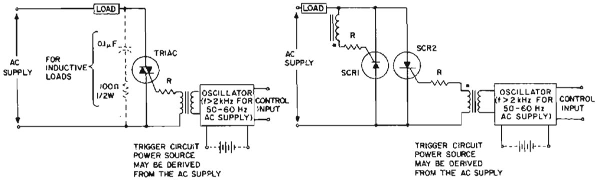
FIGURE 8.1 STATIC AC SWITCHES

For simple static AC switching, the circuit of Figure 8.1(a) has the advantage over that of Figure 8.1(b) in that it has fewer components. The circuit of Figure 8.1(b), and those circuits to follow using

the inverse-parallel SCR configuration, should be kept in mind for applications where the commercially available triacs cannot handle severe load requirements such as high frequency, voltage, and current. For inductive loads an RC snubber circuit, as shown, is required. For more information on selecting the proper snubber circuit see also Chapter 15. Triacs are available up to 400 Hz. Above 400 Hz the circuit shown in Figure 8.1(b) should be used.

8.2.2 Static Switching With Separate Trigger Source

Where DC isolation between control signal input and load is desired *without* the use of a mechanical switch (for more details on light emitters, photosensitive devices, and photocouplers, see Chapter 14), or saturable core intermediary, or where a widely varying AC supply precludes satisfactory triggering of the type shown in Figure 8.1, a triac or a back-to-back pair of SCR's may be triggered from a separate source as shown in Figure 8.2. Here, the high frequency output of a transistor blocking oscillator, or a UJT free-running oscillator is transformer coupled to the triac or SCR gates. Suitable oscillator circuits are discussed in Section 4.14. For minimum load waveform distortion and minimum generated RFI, oscillator frequency should be high enough to ensure that the triac or SCR's trigger early in the AC cycle. Other types of UJT trigger circuits suitable for use with AC static switching arrays are described in Chapter 4.



(a) (b)

FIGURE 8.2 OSCILLATOR DRIVEN AC STATIC SWITCH

8.2.3 Alternate Connections For Full Wave AC Static Switching

Full wave static AC switching can also be performed by various combinations of SCR's and conventional rectifiers, or simply by a triac. The most useful of these arrays are shown in Figure 8.3.

The circuit of Figure 8.3(a) uses a single SCR connected across the DC output of a rectifier bridge, to switch an AC load connected in series with the supply line. The bridge rectifies the incoming AC to full wave pulsating DC, so that one SCR can control both half cycles of the AC. In this circuit the SCR turns off at the end of each half cycle when the supply voltage is zero. Unsmoothed DC can be made

to flow in the load, if desired, by removing the load from the AC supply line, and placing it in series with the SCR as shown in Figure 8.3(b). In this case, for proper commutation of the SCR, a "free-wheeling" diode must be connected across the load if the load is at all inductive. The circuit of Figure 8.3(c) uses two SCR's and two rectifiers to switch an AC load, SCR1 and CR1 conducting on one half cycle of the supply, SCR2 and CR2 conducting on the other. The "DC load" equivalent to Figure 8.3(c) is shown in Figure 8.3(d). If the AC supply has significant inductance, the AC bridge in Figures 8.3(a) and (b) will reverse so rapidly that the SCR may not have time to commutate. In such a case Figures 8.3(c) and (d) will give a better result. The circuit of Figure 8.3(e) shows how a triac may be triggered with a DC control signal. Unlike the circuit of Figure 8.1(b), the static switching configurations of Figure 8.3 may be triggered directly by a single-ended (DC) non-isolated control signal, because the SCR cathodes are tied together. In low voltage switching applications, the multiple voltage drops in series with the load for Figures 8.3(a) through (d) may be a disadvantage.

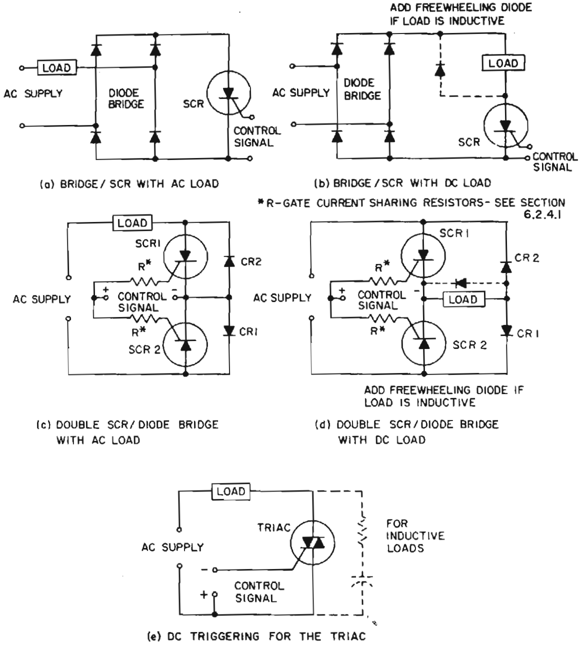


FIGURE 8.3 SCR/DIODE AND TRIAC STATIC SWITCH CONFIGURATIONS

8.2.4 Triac Latching Technique

The circuits of Figure 8.4 show a basic triac latching switch. When voltage is applied to the circuit of Figure 8.4(a), the triac is initially blocking, and the full line voltage appears across the triac. This means that no voltage appears across the load, and since the gate must be at the same level as MT_1 of the triac, there is no voltage across R_1 and C_1, and no current in the gate. After the triac has been triggered, the line voltage appears across the load, and across R_1 and C_1. The quadrature current through R_1, C_1 and the triac gate is at its peak when the load voltage goes through zero, retriggering the triac each half cycle. Since this circuit uses triggering modes III+ and I−, a specially selected triac must be used (for example, a SC41B13 should be specified instead of only SC41B).

Similarly, in Figure 8.4(b), when a trigger pulse is applied, the triac turns on. The line voltage which now appears across the load causes the flow of current through inductor L_1 and resistor R_2. This gate current is about 90° out of phase with the supply voltage. When the line voltage reverses polarity, this current continues to flow out of the gate to inductor L_1 causing the triac to turn on as the line voltage on MT_2 goes negative. Unlike the circuit of Figure 8.4(a), the circuit in Figure 8.4(b) uses triggering modes I+, III− and therefore does not require a specially selected triac as was the case for Figure 8.4(a).

The instantaneous current through the gate networks (R_1-C_1, or R_2-L_1) at the instant the line current reverses polarity determines if the triac will latch on. It is therefore necessary to select the values of R_1-C_1 or R_2-L_1 to produce a sufficient quadrature current to trigger the triac each half cycle. For reactive loads, the sinusoidal gate current is sufficiently phase shifted from the line current such that R_1 or R_2 alone (without C_1 or L_1) may be used to trigger the triac provided that enough gate drive is available when the line current goes through zero.

It will be noted that if the triac is triggered by a transient on the line, the latching characteristic of the circuit will cause the load to remain energized until the circuit is reset.

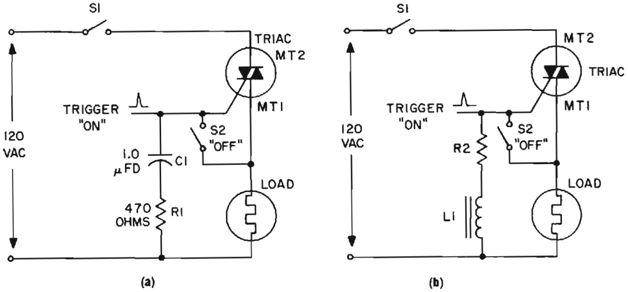


FIGURE 8.4 TRIAC LATCHING CIRCUIT

8.2.5 AC-Static SPDT Switch

A SPDT solid state relay is shown in Figure 8.5. When voltage is applied Q_1 will turn on, activating load #1, because the full line voltage appears across Q_2, supplying gate current through R_1. When S_1 is closed Q_2 turns on removing the gate drive from Q_1 and activating load #2. This circuit can be modified by using the different latching networks shown in Figure 8.4(a) and (b).

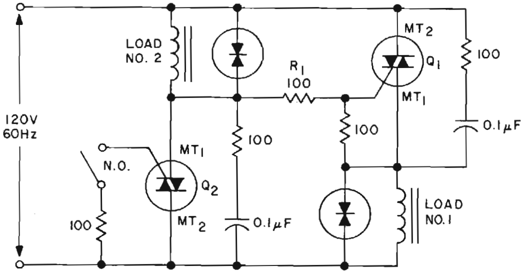


FIGURE 8.5 AC STATIC SPDT SWITCH

8.3 NEGATIVE HALF CYCLE SCR SLAVING TECHNIQUES

The circuit of Figure 8.6 shows how one SCR, in a back-to-back configuration, can be latched on to trigger at the beginning of a negative half cycle as a slave of another SCR. When SCR_1 is triggered, capacitor C_1 is charged through diode CR_1 and resistor R_1. C_1 then discharges through R_2 and the gate of SCR_2, supplying the necessary gate current to trigger SCR_2 at the beginning of the negative half cycle.

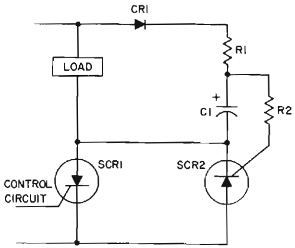


FIGURE 8.6 NEGATIVE HALF CYCLE SCR SLAVING CIRCUIT

Design Equation: $I_{GT_{max}}$ from Specification

$I_{GT_{peak}}$ $5 \times I_{GT_{max}}$

$$R_2 = \frac{E_{C1\,max}}{I_{GT_{peak}}} \qquad (8.1)$$

$$\tau_2 = C_1 \cdot R_2 \approx 4 \text{ ms (for 60 Hz operation)} \qquad (8.2)$$

$$C_1 = \frac{\tau_2}{R_2}$$

$$R_1 \approx \frac{E_{line} \cdot \sqrt{2} \cdot R_2}{E_{C1\,max}} \qquad (8.3)$$

If inductive loads have to be actuated, τ_2 may have to be increased.

In order to fire SCR_1 again when the AC line goes positive, the control circuit must supply the necessary trigger current; otherwise both SCR's would stay off. This circuit therefore is not a latching circuit.

8.3.1 SCR Slaving and Zero Voltage Switching

Figure 8.7 shows another combination of SCR slaving and synchronous switching. Here the absence of an "open" signal causes the SCR's to deliver full wave power to the load. Regardless of the phasing of the control signal, load voltage is always applied in full cycles with negligible discontinuities, hence minimum radio frequency interference. SCR_2 operates as a "slave" of SCR_1 because the energy stored in inductor L_1 triggers SCR_2 at the beginning of the next half cycle, thus always delivering an even number of half cycles to the load, and reducing magnetic saturation effects in inductive loads. By applying a gate signal to SCR_3, the gate drive to SCR_1 is diverted and its gate is essentially clamped to its cathode. When the line goes positive on the anode of SCR_1, since there is no gate signal present, SCR_1 is kept off, thus de-energizing the load. These circuits are ideal wherever RFI and audio filtering is undesirable, where magnetizing inrush current to transformers causes nuisance fuse blowing, and where sensitive test equipment operates in the vicinity of power switches.

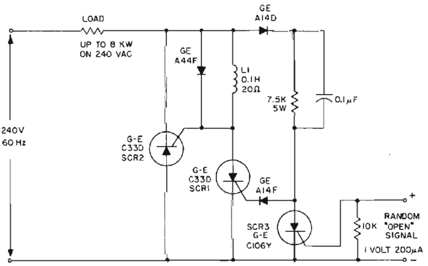
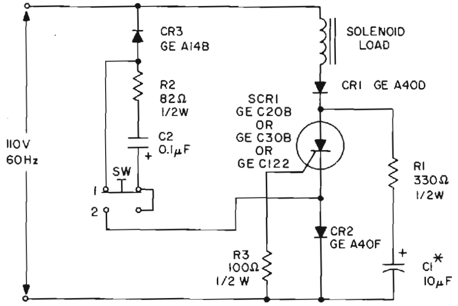


FIGURE 8.7 ZERO VOLTAGE SWITCHING FOR LOW RFI OPERATION

This circuit is shown to explain how slaving techniques can be employed. For more information on zero voltage switching refer to Chapter 11 on zero voltage switching.

8.4 "ONE SHOT" SCR TRIGGER CIRCUIT

A circuit to trigger an SCR for one complete half cycle only of the AC supply is shown in Figure 8.8. Triggering is initiated by closing push button switch SW, and the SCR triggers always *near the beginning* of a positive half cycle, even though the switch may be closed randomly at any time during the two preceding half cycles. The SCR will not trigger again until SW is opened and then reclosed. This type of logic is required for some test equipment supplies and for the solenoid drives of electrically operating stapling guns, impulse hammers, etc., where load current must flow for one complete half cycle only.



*TIME CONSTANT OF C1 R1 MAY NEED TAILORING DEPENDING ON HOLDING CURRENT OF SCR1. SEE TEXT.

FIGURE 8.8 ONE SHOT SCR TRIGGER CIRCUIT

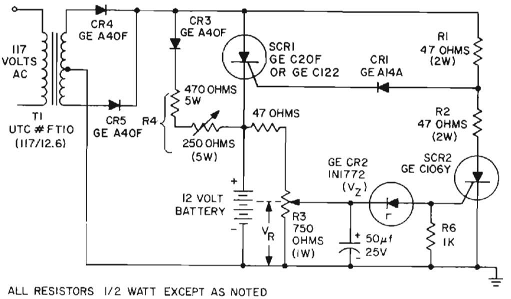
During half cycles of the AC line when the SCR anode is positive, capacitor C_1 will be charged through the load, CR_1 and R_1. As long as switch SW is maintained in position 1, the SCR will be non-conducting. When SW is flipped to position 2 and the line voltage is negative, the charging current of C_2 (through the series-network of R_3, the gate to cathode junction of the SCR, SW, C_2, R_2 and CR_3) will trigger the SCR even though the line voltage is negative because the anode of the SCR sees the positive voltage on C_1. SCR_1 is thus only turned on when the line voltage is negative and maintained on by supplying holding current from capacitor C_1, through resistor R_1. The series network of R_1 and C_1 is selected to supply a sufficient amount of holding current for one-half cycle only since providing holding current for a longer duration than one-half cycle would keep the SCR on for succeeding half cycles. The SCR holding current therefore determines R_1 C_1. Once C_2 has been charged, there will be no gate current through the SCR

even if SW is maintained in position 2. To trigger the SCR again, SW would have to be flipped to position 1 in order to discharge C_2.

8.5 BATTERY CHARGING REGULATOR

Figure 8.9 illustrates an inexpensive means of utilizing the SCR as a battery charging regulator, thus eliminating the problems inherent in electromechanical voltage relays – contact sticking, burning, wide range of pickup and drop out, wear, etc. As shown the circuit is capable of charging a 12 volt battery at up to a six ampere rate. Other voltages and currents, from 6 to 600 volts and up to 300 amperes, can be accommodated by suitable component selection.[3] When the battery voltage reaches its fully charged level, the charging SCR shuts-off, and a trickle charge as determined by the value of R_4 continues to flow.

CR_4 and CR_5 deliver full-wave rectified DC to SCR_1 in series with the battery to be charged. With the battery voltage low, SCR_1 is triggered on each half cycle via resistor R_1 and diode CR_1. Under these conditions, the pick-off voltage V_R at the wiper of potentiometer R_3 is less than the breakdown voltage V_Z of zener diode CR_2, and SCR_2 cannot trigger. As the battery approaches full charge, its terminal voltage rises, the magnitude of V_R equals V_Z (plus gate voltage required to trigger SCR_2), and SCR_2 starts to trigger each half cycle. At first SCR_2 triggers at $\pi/2$ radians (90°) after the start of each half cycle, coincident with peak supply voltage, peak charging current and maximum battery voltage. As the battery voltage climbs yet higher as charging continues, the triggering angle of SCR_2 advances each half cycle until eventually SCR_2 is triggering *before* the input sine wave has sufficient magnitude to trigger SCR_1. With SCR_2 on first in a half-cycle, the voltage divider action of R_1 and R_2 keeps CR_1 back-biased, and SCR_1 is unable to trigger. Heavy charging then ceases. Diode CR_3 and resistor R_4 may be added, if desired, to trickle charge the battery during the normal "off" periods. Heavy charging will recommence automatically when V_R drops below V_Z and SCR_2 stops triggering each cycle.



ALL RESISTORS 1/2 WATT EXCEPT AS NOTED

FIGURE 8.9 BATTERY CHARGING REGULATOR

8.6 DC STATIC SWITCH

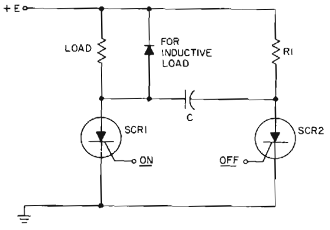


FIGURE 8.10 DC STATIC SWITCH (SCR FLIP-FLOP)

Figure 8.10 illustrates a static SCR switch for use in a DC circuit. When a low power signal is applied to the gate of SCR_1, this SCR is triggered and voltage is applied to the load. The right hand plate of C charges positively with respect to the left hand plate through R_1. When SCR_2 is triggered on, capacitor C is connected across SCR_1, so that this SCR is momentarily reverse biased between anode and cathode. This reverse voltage turns SCR_1 off provided the gate signal is not applied simultaneously to both gates. The current through the load will decrease to zero in an exponential fashion as C becomes charged.

SCR_1 should be selected so that the maximum load current is within its rating. SCR_2 need conduct only momentarily during the turn-off action, it can be smaller in rating than SCR_1. The minimum value of commutating capacitance C can be determined by the following equations:

$$\text{For Resistive Load: } C \geqq \frac{1.5\, t_{off} I}{E}\ \mu\text{fd} \tag{8.4}$$

$$\text{For Inductive Load: } C \geqq \frac{t_{off} I}{E}\ \mu\text{fd} \tag{8.5}$$

Where t_{off} = Turn-off time of SCR in μ seconds (see specification for inverter-type SCR)

I = Maximum load current (including possible overloads) in amperes at time of commutation

E = Minimum DC supply voltage

The resistance of R_1 should be ten to one hundred times less than the minimum effective value of the forward blocking resistance of SCR_2. This latter value can be derived from the published leakage current curves for the SCR under consideration.

In some cases a mechanical switch may be substituted for SCR_2, to turn off SCR_1 when it (the switch) is momentarily closed. Many other useful variations of this basic DC static switch can be devised, among them the following circuits.

8.6.1 DC Latching Relay or Power Flip-Flop

By replacing resistor R_1 with a second driven load, and selecting SCR_2 to suit, the circuit of Figure 8.10 becomes the static analog of a single pole double throw latching relay. In this case commutating capacitor C should be selected on the basis of the heavier of the two loads. By driving the gates with a train of pulses as shown in Figure 8.11 the circuit becomes a high power flip-flop or multivibrator. Sine wave or square wave sources may also be used to drive the gates in this configuration.

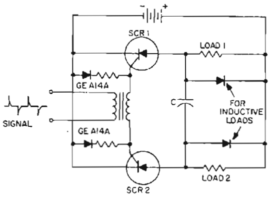


FIGURE 8.11 POWER FLIP-FLOP AND LATCHING RELAY

8.7 FLASHER CIRCUITS

The different types of flasher circuits described in Section 8.6 are basically power flip-flop and used in a variety of applications such as traffic lights, navigational beacons, aircraft beacons, and illuminated signs. The SCR and the triac are ideally suited for this type of application since they can function over a wide range of current and voltage with a much higher degree of reliability than the commonly used electromechanical systems. The SCR and the triac also offer an important advantage over power transistors in that they do not require excessive derating of current to handle the high inrush currents of incandescent lamps. The UJT, PUT and transistor make ideal trigger devices for the SCR and triac in this type of application since they permit an economical method for obtaining a wide frequency range and a high degree of frequency stability. More information on flashers will be found in Reference 4.

8.7.1 DC-Flasher With Adjustable On & Off Time

Figure 8.12 shows a flasher circuit utilizing a power flip-flop and programmable unijunction (PUT) to obtain adjustable "on" and "off" times.

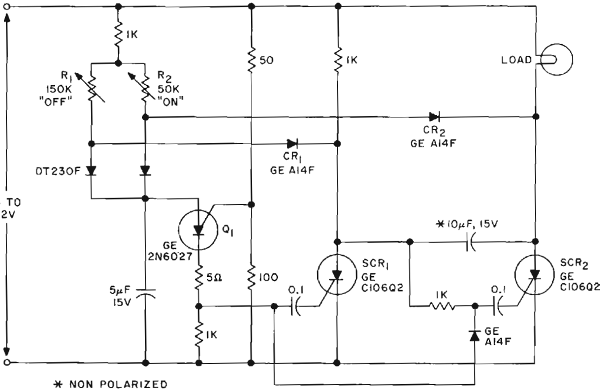


FIGURE 8.12 DC FLASHER WITH ADJUSTABLE "ON" AND "OFF" TIME

Assume SCR_1 is on, which inhibits the 0.1 μf capacitor on the gate of SCR_2 from charging. Resistor R_1 is clamped to ground through SCR_1, so that it cannot contribute to the charging current of the 5μf timing capacitor on the anode of the PUT. When the anode voltage on Q_1 exceeds the gate voltage by about 0.5 volt, Q_1 will trigger and trigger SCR_2. SCR_1 will be turned off by energy stored in the 10μf commutating capacitor. The 0.1 capacitor on the gate of SCR_2 will charge to the anode voltage of SCR_1 and R_2 will be clamped by SCR_2. Now only R_1 can charge the 5μf capacitor. When the triggering voltage of Q_1 is reached for the second time, SCR_1 will be triggered and SCR_2 will be commutated.

"On" and "off" times can be independently adjusted. The 1 K resistor in the anode circuit of SCR_1 can be replaced by a second lamp.

8.7.2 Low Voltage Flasher

Using an SCR and a complementary SCR, as shown in Figure 8.13, a simple low cost, low voltage flasher is feasible.

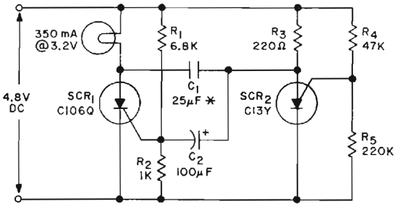


FIGURE 8.13 LOW VOLTAGE FLASHER

Applying voltage to the circuit triggers SCR_1. With SCR_1 on the voltage on the anode of SCR_2 rises until SCR_2 triggers to commutate SCR_1. The voltage on the gate of SCR_1 will swing negative at this time and only after a positive potential of $\approx$ 0.5 volt is once again attained, will SCR_1 retrigger.

The circuit could be used for higher voltage levels, but the peak negative voltage on the gate of SCR_1 must be limited to less than 6 volts.

8.7.3 Sequential Flasher

A sequential flasher as used in automotive turn signals is shown in Figure 8.14.

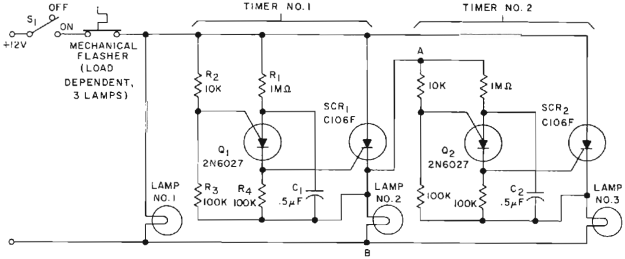


FIGURE 8.14 SEQUENTIAL FLASHER

When the turn signal switch S_1 is closed, lamp #1 will be activated and capacitor C_1 will charge to the triggering voltage of Q_1. As soon as the anode voltage on Q_1 exceeds its gate voltage by 0.5 V, Q_1 will switch into the low resistance mode, thereby triggering SCR_1 to activate lamp #2 and the second timing circuit. After Q_2 switches into the low

resistance state, SCR_2 will be triggered to activate lamp #3.

When the thermal flasher interrupts the current to all three lamps, SCR_1 and SCR_2 are commutated and the circuit is ready for another cycle.

8.7.4 Low Power Flasher

The circuit shown in Figure 8.15 has been chosen to illustrate the basic principles of an SCR/UJT flasher which can be easily simplified or modified to meet specific application requirements.

Unijunction transistor Q_1 operates as a relaxation oscillator, delivering a train of trigger pulses to the two SCR gates via resistor R_1. Assume SCR_2 is "on" and the lamp is energized. When the next trigger pulse comes along it triggers SCR_1 and SCR_2 is turned off by the commutation pulse coupled to its anode via capacitor C_2. Because the commutation pulses have longer duration than the trigger pulses, SCR_2 cannot be re-triggered inadvertently at this time. SCR_2 is re-triggered properly by the *next* trigger pulse from R_2. "Lock-up" (failure to flash caused by both SCR's being on together) is prevented by making SCR_1's turn off independent of the commutating capacitor. This is done by operating SCR_1 in a "starved" mode, that is by making resistor R_2 so large that SCR_2 is unable to remain "on", except to discharge C_2. During the remainder of the cycle SCR_1 is off, and C_2, therefore, is always able to develop commutating voltage for SCR_2. With the components shown, the flash rate is adjustable by potentiometer R_3 within the range 36 flashes per minute to 160 flashes per minute.

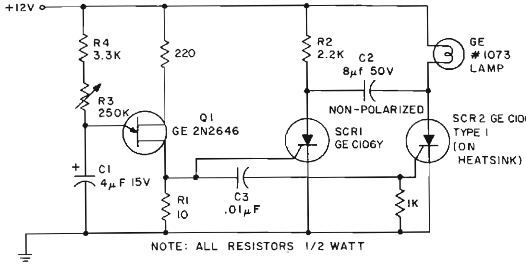


FIGURE 8.15 DC LOW POWER FLASHER

8.7.5 AC Flasher

For heavy load requirements, the DC flashers have the disadvantage of requiring a large commutating capacitor. In such applications, the use of AC flashers ends up being more economical. Figure 8.16 illustrates a power flip-flop flasher circuit that can handle two independent loads up to 2.5 KW each. Transformer T_1, diodes CR_1

through CR_4, resistor R_1 and capacitor C_1 provide the DC supply to the free running unijunction oscillator and the transistor flip-flop of Q_2, Q_3. The interbase voltage for Q_1 is taken directly from the positive side of the bridge rectifier in order to synchronize the free running unijunction oscillator with the supply frequency. The negative going output pulses developed across R_4 trigger the transistors of the flip-flop which alternately turn the triacs on and off. The flashing rate is determined by the time constant of R_2, R_3 and C_2.

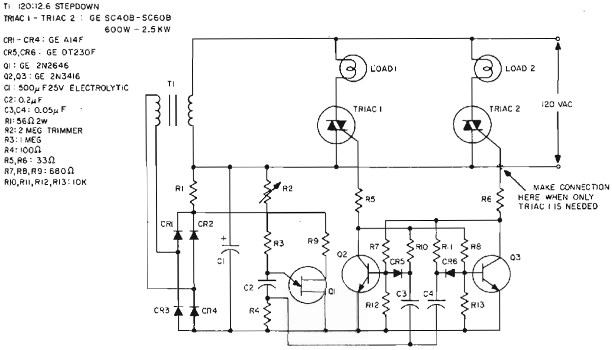


FIGURE 8.16 AC POWER FLASHER

8.8 PROTECTIVE SCR CIRCUITS

The fast switching characteristic of the SCR makes possible some interesting protective circuits against line transients, excessive voltages, and short circuit currents.

Some examples of this type of circuit are shown below, but a more thorough treatment of the subject of overcurrent and overvoltage on thyristors can be found in Chapters 14 and 15.

8.8.1 Overvoltage Protection on AC Circuits

Figure 8.17 illustrates a circuit that may be employed for general transient protective service on AC lines. When the line exceeds the avalanche voltage of the zener diode, either SCR_1 or SCR_2 triggers, depending on the polarity of the AC line at that instant. Resistor R_1 limits the current to the short term surge capabilities of the SCR's. For the C35, R_1 must limit the one cycle peak current to less than 225 amperes. This loading effect on the circuit drops the transient voltage across line impedance. Alternation of the AC line voltage turns off the current through the conducting SCR at the end of the cycle.

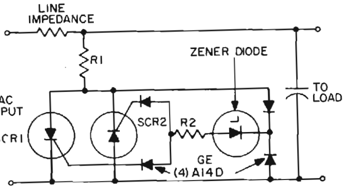


FIGURE 8.17 TRANSIENT VOLTAGE PROTECTION USING SILICON CONTROLLED RECTIFIERS

8.8.2 SCR Current-Limiting Circuit Breakers

In some phase controlled applications, the fault current due to a short circuit may reach destructive proportions within one-half cycle. This would prohibit use of conventional circuit breakers for protection. Also, in some types of inverters operating on DC it may be desirable to have a fast electronic circuit breaker in the event of loss of commutation in the inverter for any reason.

An SCR current limiting circuit breaker of the type shown in its simplest form in Figure 8.18 will provide these protective functions very nicely. This package can be inserted in series with the DC output of a phase-controlled rectifier or in series with the DC input to an inverter circuit.

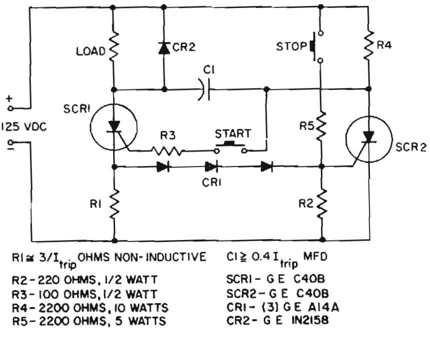
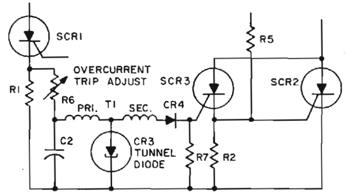


FIGURE 8.18 16 AMPERE DC CIRCUIT BREAKER

The circuit breaker is basically a parallel capacitor commutated flip-flop. When the "Start" button is momentarily depressed, SCR_1 starts to conduct and delivers power to the load provided the load current is above the minimum holding current of SCR_1. Capacitor C_1 then charges to the load voltage through R_4, the right hand terminal of C_1 being positive with respect to the left hand terminal. When SCR_2 is triggered by momentary closing of the "Stop" button, the positive terminal of capacitor C_1 is connected to the cathode of SCR_1, reversing the polarity across this SCR and turning it off. This interrupts the flow of load current and opens the circuit. SCR_2 will also be triggered by the voltage developed across R_1 by load current if this exceeds the forward voltage drop of the string of series diodes CR_1 plus the gate triggering requirements of SCR_2. By adjustment of the value of R_1 and by selecting the proper number of series diodes CR_1, the circuit can be made to trip out and interrupt overload or fault current at any predetermined level. For a more consistent tripping level under temperature variations, a zener diode can be substituted in place of all but one of the series diodes at CR_1. For still more precise tripping, a UJT or PUT overcurrent sensor can be used.

The characteristics of the germanium tunnel diode are also very useful in developing a gate signal when a specific level of current is exceeded. The tunnel diode has a very stable peak current at which it switches from a low resistance to a relatively high resistance. This, combined with a very low voltage drop, makes it almost ideal for this type of application. A tunnel diode overcurrent detecting network for the circuit breaker of Figure 8.18 is shown in Figure 8.19. Main load current flows through SCR_1 and R_1. Part of the load is shunted through R_6, tunnel diode CR_3, and the primary winding of T_1, R_1 and R_6 are selected so that less than 20 ma. flows through the tunnel diode at maximum rated load. Under this condition CR_3 remains in its low resistance state. If the main load current rises to the point where more than 20 ma. flows through CR_3, it switches instantaneously to its high resistance state. If the current through the tunnel diode is maintained constant through the switching interval, the voltage across it increases about five-fold. This sudden change in voltage across CR_3 induces a pulse of voltage in the primary of T_1 which is stepped up by autotransformer action and applied to the gate of SCR_3, thereby tripping the circuit breaker. The tripping point is stable within a few percent over a wide temperature range and is independent of the triggering characteristics of SCR_3.

The component values in Figure 8.18 apply for a 125 volt DC system. When using the C40 SCR, the tripping current level should not exceed 100 amperes in order to stay within the switching rating of SCR_2.



SCR3 - GE C106B
R1 ≈ -3/I_{trip} OHMS, NON-INDUCTIVE
R6 - 250 OHM LINEAR POT
R7 - 1000 OHMS, 1/2 WATT
C2 - 2 MFD, 10 VOLT
CR3 - GERMANIUM TUNNEL DIODE GE IN372
CR4 - GE IN91
T1 - AIR CORE TRANSFORMER, 1/4" DIA.,
P = 50T, S = 500T, # 26AWG

FIGURE 8.19 TUNNEL DIODE SENSING NETWORK FOR FIGURE 8.18

8.8.3 High Speed Switch or "Electronic Crowbar"

A form of "electronic crowbar," shown in Figure 8.20, has proved very useful for protecting DC circuits against input line voltage transients and short circuit load conditions. If the DC supply exceeds the desired maximum value as determined by the setting of potentiometer R_1, the voltage at the emitter of UJT_1 exceeds the peak point voltage causing UJT_1 to trigger which in turn triggers the SCR. The full supply voltage is then applied to the circuit breaker trip coil causing the circuit breaker to open the main DC supply bus. Besides increasing the speed of the circuit breaker action this circuit instantly loads down the DC bus, preventing the voltage on the load from rising until the circuit breaker has time to operate. The circuit also protects the load and the supply against short circuit conditions by monitoring the current through resistor R_3. When the voltage across R_3 exceeds the desired maximum value as determined by the setting of potentiometer R_2 the voltage at the emitter of UJT_2 exceeds the peak point voltage, causing UJT_2 and the SCR to trigger as before. Due to the stable firing voltage of the UJT the trip voltage across R_3 can be very low, a value in the range from 100 millivolts to 500 millivolts being suitable for most applications. If only overvoltage protection is desired the circuit of Figure 8.20 can be simplified by eliminating UJT_2 and its associated circuitry. Similarly, if only overcurrent protection is desired UJT_1 and its associated circuitry can be eliminated.

In the circuit of Figure 8.20 rectifier CR_1 and capacitor C_3 are used to provide filtering against negative voltage transients which would otherwise result in false tripping of the circuit. The values of potentiometer R_1 and R_2 are chosen to have appropriate time constants with C_1 and C_2 so as to give the desired voltage-time response in the tripping action.

The SCR is ideal for this type of circuit because of its ability to switch on within a few microseconds after being triggered.

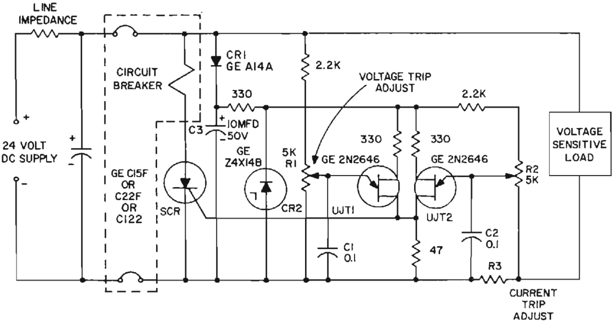


FIGURE 8.20 ELECTRONIC CROWBAR PROTECTION OF DC CIRCUITS AGAINST OVERVOLTAGE AND/OR OVERCURRENT

For higher capacity circuits, the C35F or C50F SCR's can be substituted for the C22F shown. With the C50F SCR this circuit is capable of carrying momentary currents as high as 2000 amps for 2 milliseconds without damage to the SCR.

8.9 RING COUNTERS

A ring counter may be considered as a circuit that sequentially transfers voltage from one load to the next, when a number of loads are connected in parallel from a common supply. Transfer along the string proceeds always in the same direction, and each transfer is initiated by pulsing a common input line. The ring counter is an extremely useful tool in digital applications, and SCR ring counters in particular excel in low speed applications that require high voltage, high current or both.

8.9.1 Cathode Coupled Ring Counter

As an example a ten stage SCR ring counter can function as a decade counter with direct lamp or glowtube (Nixie)® readout. The circuit of Figure 8.21 is a three stage cathode coupled ring counter, suitable for driving high voltage loads up to 50 mA. Additional stages may be added as required. Assume SCR_1 is conducting load current, and SCR_2 and SCR_3 are both blocking. Capacitors C_3 and C_1 charge to the supply voltage through R_3/R_{L2} and R_1/R_{L3} respectively, while capacitors C_5 and C_6 charge through R_{L2} and R_{L3}. Because SCR_1 is conducting, C_2 and C_4 cannot charge. When a shift pulse arrives at the shift line only SCR_2 can be triggered, since its gate steering diode CR_2 is the only diode not reverse biased by a pre-charged capacitor. In any ring counter only the SCR following the conducting SCR will trigger. As SCR_2 turns on, capacitor C_5 is connected across R_4, which drives the common cathode line momentarily to the supply voltage, reverse biasing SCR_1 and forcing it to turn off. When the next shift pulse arrives, SCR_3 turns on and SCR_2 turns off and so on. The advan-

tage of the cathode coupled ring counter is that undistorted square waves free from commutation transients appear across each load. Its major disadvantage is that relatively large value commutating capacitors (C_4, C_5, C_6) are required with consequent limitations on circuit speed.

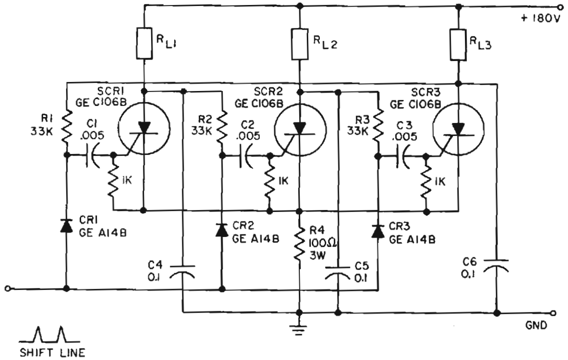


FIGURE 8.21 CATHODE COUPLED RING COUNTER

8.9.2 Anode Coupled Ring Counter

In applications where commutation transients can be tolerated and/or higher speed operation is required (lamp driving circuits for instance), the ring counter circuit can be modified as follows:

1. Remove resistor R_4, and ground the common cathode line.
2. Remove C_4, C_5, and C_6.
3. Connect a .005 μf capacitor between each pair of SCR anodes.

Figure 8.22 shows the modified circuit being used to drive a #6844A Nixie Decade Readout Tube.[5]

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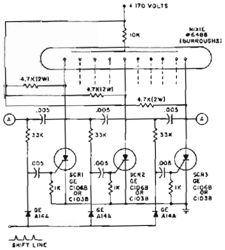
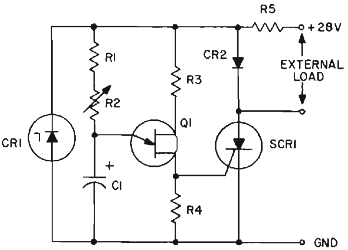


FIGURE 8.22 ANODE COUPLED RING COUNTER (DECADE READOUT)

8.10 TIME DELAY CIRCUITS

Time delay circuits are used frequently in industrial controls and aircraft and missile systems to apply or remove power from a load a predetermined time after an initiating signal is applied. Cascaded time delay circuits can be used to sequentially perform a series of timed operations.

8.10.1 UJT/SCR Time Delay Relay



R1 - 2.2K, 1/2 WATT
R2 - 1K TO 500K LINEAR POT
R3 - 150Ω, 1/2 WATT
R4 - 27, Ω, 1/2 WATT
R5 - 560Ω, 2 WATT

C1 - 0.2 TO 100 MFD, 15V
SCR1 - GE C22F OR C11F OR C122F
CR1 - 18V, 10%, 1 WATT ZENER, 1N1776
CR2 - GE A14A
Q1 - GE 2N1671B

FIGURE 8.23 PRECISION SOLID STATE DC TIME DELAY CIRCUIT

Figure 8.23 illustrates an extremely simple yet accurate and versatile solid state time delay circuit. The operating current and voltage of the circuit depend only on the proper choice of the SCR. Resistor R_5 and Zener diode CR_1 provide a stable voltage supply for the UJT. Initially SCR_1 is off and there is no voltage applied to the load. Timing is initiated either by applying supply voltage to the circuit or by opening a shorting contact across C_1. The timing capacitor C_1 is charged through R_1 and R_2 until the voltage across C_1 reaches the peak point voltage of the UJT at which time the UJT triggers, generating a pulse across R_4 which triggers SCR_1. The full supply voltage minus the SCR drop then appears across the external load terminals. Holding current for SCR_1 is provided by the current through R_5 and CR_2. Thus the external load may be removed or connected at any time without affecting the performance of the circuit. When SCR_1 triggers, the voltage across the UJT drops to less than 2 volts due to the clamping action of CR_2. This acts to rapidly set and maintain a low voltage on C_1 so that the time interval is maintained with reasonable accuracy if the circuit is rapidly recycled. For the highest accuracy, however, additional means must be used to rapidly and accurately set the initial voltage on C_1 to zero at the beginning of the timing cycle. A pair of mechanical contacts connected across C_1 is ideal for this purpose.

The time delay of the circuit depends on the time constant $(R_1 + R_2) C_1$ and can be set to any desired value by appropriate choice of R_1, R_2, and C_1. The upper limit of time delay which can be achieved depends on the required accuracy, the peak point current of the UJT, the maximum ambient temperature, and the leakage current of the capacitor and UJT (I_{EO}) at the maximum ambient temperature. The absolute upper limit for the resistance $R_1 + R_2$ is determined by the requirement that the current to the emitter of the UJT be large enough to permit it to trigger (i.e., be greater than the peak point current) or

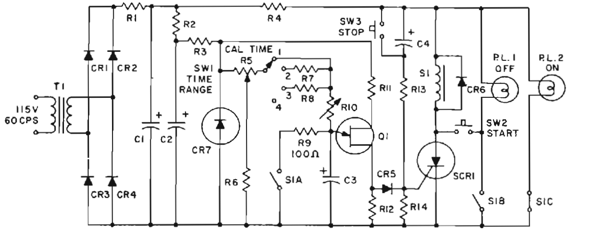
$$R_1 + R_2 < \frac{(1 - \eta) V_1}{\frac{25 I_p}{V_1} + I_c} \tag{8.6}$$

where η is the maximum value of intrinsic standoff ratio, V_1 is the minimum supply voltage on the UJT, I_p is the maximum peak point current measured at an interbase voltage of 25 volts, and I_c is the maximum leakage current of the capacitor at a voltage of ηV_1. If high values of capacitance are required it is desirable to use stable, low leakage types of tantalytic capacitors. If tantalytic or electrolytic capacitors are used it is necessary to consider forming effects which will cause the effective capacitance and hence the period to change as a function of the voltage history of the capacitor. These effects can be reduced by applying a low bias voltage to the capacitor in the standby condition.

The resistor R_3 can serve as a temperature compensation for the circuit, increasing the value of R_3 causes the time delay interval to have a more positive temperature coefficient. The over-all temperature coefficient can be set exactly zero at any given temperature by careful adjustment of R_3. However, ideal compensation is not possible over a wide range because of the nonlinear effects involved. To reset the circuit in preparation for another timing cycle SCR_1 must be turned off either by momentarily shorting it with a switch contact or by opening the DC supply.

8.10.2 AC Powered Time Delay Relay

Figure 8.24 illustrates a time delay circuit using a relay output with a push button initiation of the timing sequence. In the quiescent state SCR_1 is on and relay S_1 is energized. Contact S_1A is closed, shorting out the timing capacitor C_3. To initiate the timing cycle push button switch SW_2 is momentarily closed which shorts SCR_1 through contact S_1B causing SCR_1 to turn off. When SW_2 is released S_1 is de-energized and the timing sequence begins. The particular configuration of SW_2 and S_1B is used to prevent improper operation in case SW_2 is closed again during the timing cycle. Capacitor C_3 is charged through R_5 and R_{10} until the voltage across C_3 reaches the peak point voltage of Q_1 causing Q_1 to trigger. The positive pulse generated across R_{12} triggers SCR_1 which pulls in the relay and ends the timing cycle. The timing cycle can be terminated at any time by push button switch SW_3 which causes current to flow in R_{13} thus triggering SCR_1. Capacitor C_4 supplies current through R_{13} during the instant after the supply is turned on thus triggering SCR_1 and setting the circuit in the proper initial state.



R1 – 2Ω, 1 WATT
R2, R3 – 330Ω, 1/2 WATT
R4 – 35Ω, 5 WATT
R5 – 2.5K, LINEAR POT
R6 – 25K, 1/2 WATT
R7 – 100K, 1/2%, 1/2 WATT
R8 – 200K, 1/2%, 1/2 WATT
R9 – 10Ω, 1/2 WATT
R10 – 100K, 10 TURN HELIPOT
R11 – 150Ω, 1/2 WATT
R12 – 18Ω, 1/2 WATT
R13 – 1.2K, 2 WATT
R14 – 100Ω, 1/2 WATT
C1 – 500μFD, 50V
C2 – 100μ FD, 50V
C3 – 100μFD, 20V TANTALUM
C4 – 10μFD, 50V
SCR1 – GE C15F OR C11F OR C122
CR1 – CR6 – GE A14A
CR7 – 18V, 10% 1 WATT ZENER
Q1 – GE 2N1671B
S1 – GE CR2791G122A4 4PDT RELAY
PL1, PL2 – GE 1447, 24V LAMP
T1 – 115V/25V 1A TRANSFORMER

FIGURE 8.24 VARIABLE TIME CONTROL CIRCUIT

The timing interval is determined by the setting of a precision ten turn Helipot R_{10} which may be set from 0.25 to 10.25 seconds in increments of 0.01 second. The initial setting of 0.25 seconds takes into account the added series resistance of the time calibration potentiometer R_5. Additional series resistance of 100K and 200K may be added by SW_1 to extend the time range by 10 seconds and 20 seconds. A fourth position of SW_1 open circuits the timing resistors and thus permits unrestricted on-off control of the circuit.

Tests of the circuit have shown an absolute accuracy of 0.5% after initial calibration and a repeatability of 0.05% or better.

8.10.3 Ultra-Precise Long Time Delay Relay

Predictable time delays from as low as 0.3 milliseconds to over

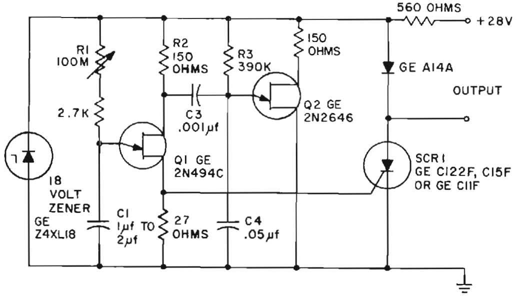


FIGURE 8.25 ULTRA-PRECISE LONG PERIOD TIME DELAY

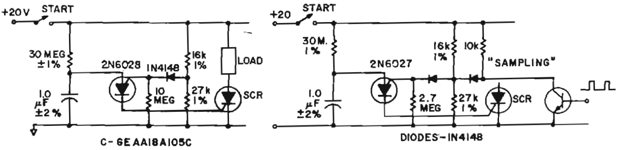
3 minutes are obtainable from the circuit of Figure 8.25, without resorting to a large value electrolytic-type timing capacitor. Instead, a stable low leakage paper or mylar capacitor is used and the peak point current of the timing UJT (Q_1) is effectively reduced, so that a large value emitter resistor (R_1) may be substituted. The peak point requirement of Q_1 is lowered up to 1000 times, by pulsing its upper base with a ¾ volt negative pulse derived from free-running oscillator Q_2. This pulse momentarily drops the peak point voltage of Q_1, allowing peak point current to be supplied from C_1 rather than via R_1. Pulse rate of Q_2 is not critical, but it should have a period τ that is less than .02 ($R_1 \cdot C_1$). With $R_1 = 2000$ megohms and $C_1 = 2$ μf (mylar), the circuit has given stable time delays of over one hour. R_2 is selected for best stabilization of the triggering point over the required temperature range. Because the input impedance of the 2N494C UJT is greater than 1500 megohms before it is triggered, the maximum time delay that can be achieved is limited mainly by the leakage characteristics of C_1.

8.10.4 Time Delay Circuits Utilizing the Programmable Unijunction Transistor (PUT)

Very simple and precise time delay circuits can be achieved with the PUT.[6] Among the important advantages are elimination of calibration pots, longer time delays and low cost.

8.10.4.1 30 Second Timer

Figure 8.26(a) shows a 30 second time delay using the 2N6028. Here we are taking advantage of high sensitivity to achieve high values of timing resistance (30 megs). Calibration has been eliminated by using 1% components for the intrinsic standoff resistors and also for the RC timing components. Note the additional use of the compensation diode 1N4148.



(a) (b)

FIGURE 8.26 PRE-CALIBRATED 30 SECOND TIMERS

The same performance can be achieved using the 2N6027, as in Figure 8.26(b). When using the 2N6027, one must either significantly decrease the value of the timing resistor and increase the capacitance, or use a sampling scheme as shown here. This is precisely the same timer as in Figure 8.26(a) with the addition of the 10K resistor, a diode

and the sampling transistor. A 1KHz pulse train is applied to the base of the NPN transistor. Each pulse lasts 10 μsecs. This modulates the intrinsic standoff voltage once every 1 millisecond to "take a look" at the capacitor voltage. The 2N6027 derives its peak point current from the capacitor.

Calibration of timers is easier using the PUT. When R_T and C_T are not 1% parts, the scheme in Figure 8.27 can be used. Here an inexpensive, low resistance, trimpot can be used instead of a wire-wound pot for the time adjustment.

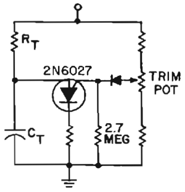


FIGURE 8.27 CALIBRATION VIA THE "INTRINSIC STAND-OFF RATIO"

8.10.4.2 Long Delay Timer Using PUT

Figure 8.28 shows the use of the PUT's as both a timing element and sampling oscillator. A low leakage film capacitor is required for C_2 due to the low current supplied to it.

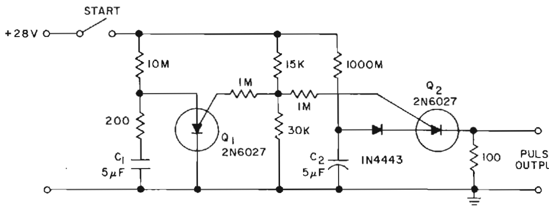


FIGURE 8.28 LONG DELAY TIMER

8.10.5 A 60-Second Time Delay Circuit Switching AC

Figure 8.29 shows a time delay circuit using the triac latching technique. When capacitor C_1 charges to the breakover voltage of the diac, the triac triggers and energizes the load. The time delay is determined by the time constant of $(R_1 + R_2)$ and C_1. To reset the circuit, capacitor C_1 is discharged through R_3 and S_1.

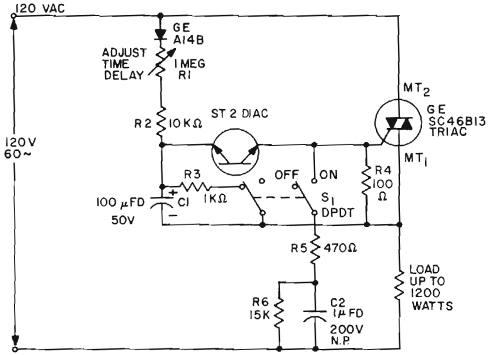


FIGURE 8.29 A SIXTY-SECOND TRIAC TIME DELAY CIRCUIT

8.10.6 One Second Delay Static Turn-Off Switch

An AC-switch with delayed turn-off is shown in Figure 8.30. The components CR_1, R_1, CR_2 and C_1 supply about -20 V between the MT_1 and the gate terminal of the triac, but gate current can only flow to trigger Q_1 when SW is closed to forward bias Q_2 into conduction. As long as SW is closed Q_2 is saturated and Q_1 maintains the load activated.

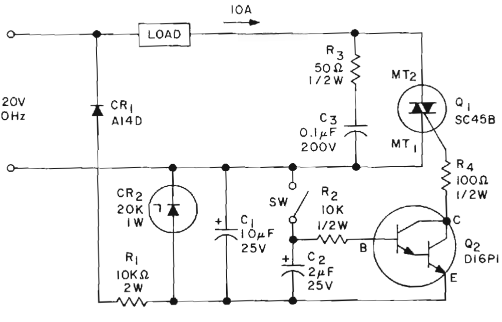


FIGURE 8.30 ONE SECOND DELAY STATIC TURN-OFF SWITCH

When SW is opened C_2 will discharge through R_2 and the base emitter junction of Q_2, keeping Q_2 and Q_1 conducting. As C_2 discharges, Q_2 will finally turn off and the triac will commutate at the next zero crossing, interrupting the load current.

Changing the time constant C_2 R_2 permits the selection of various turn-off delay intervals.

8.11 NANOAMPERE SENSING CIRCUIT WITH 100 MEGOHM INPUT IMPEDANCE

The circuit of Figure 8.31 may be used as a sensitive current detector, or as a voltage detector having high input impedance. A sampling technique similar to that described in the previous section is used to give an input current sensitivity (I_{IN}) of less than 35 nanoamperes. Input impedance is better than 100 megohms.

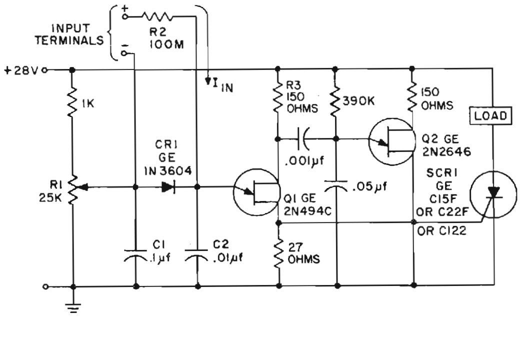


FIGURE 8.31 NANOAMPERE SENSING CIRCUIT

Current gain between output and input of the circuit as shown is greater than (200×10^{-6}).

Resistor R_1 is adjusted so that the circuit will not trigger in the absence of the current input signal I_{IN}. I_{IN} then charges C_2 through the 100 megohm input resistor R_2 towards the emitter triggering voltage of Q_1. R_2, however, cannot supply the peak point current (2 μA) necessary to trigger Q_1, and this current is obtained from C_2 itself by dropping Q_1's triggering voltage momentarily below V_{C2}. Relaxation oscillator Q_2 supplies a series of .75 volt negative pulses to base two of Q_1 for this purpose. The period of oscillation of Q_2 is not critical but should be less than .02 times the period of Q_1. Capacitor C_2 can be kept small for fast response time because C_1 stores the energy required to trigger SCR_1. Rapid recovery is possible because both capacitors are charged initially from R_1. Some temperature compensation is provided by the leakage current of CR_1 subtracting from the

leakage current of Q_1. Further compensation is obtainable by adjusting the value of R_3. A floating power supply for the UJT trigger circuit with pulse transformer coupling from Q_1 to SCR_1, enables one of the two input terminals to be grounded, where this may be desirable.

8.12 MISCELLANEOUS SWITCHING CIRCUITS USING GE LOW CURRENT SCR'S

The C103 C5, C6 and C106 series of SCR's have a high gate sensitivity. Gate triggering can therefore be achieved from such low level elements as thermistors and light sensitive resistors. When used as a gate amplifier for the higher rated SCR's, either of these devices makes possible a multitude of solid state thyratron tube analogues. The C5 SCR is also suitable for use as a very high voltage remote-base transistor. For more detailed application information on the low current SCR's, see Reference 5.

8.12.1 Dual Output, Over-Under Temperature Monitor

The circuit of Figure 8.32 is ideal for use as an over-under temperature monitor, where its dual output feature can be used to drive "HIGH" and "LOW" temperature indicator lamps, relays, etc.

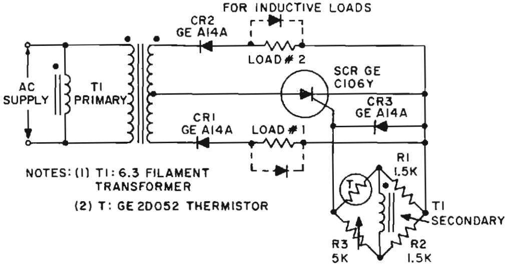


FIGURE 8.32 TEMPERATURE MONITOR

T_1 is a 6.3 volt filament transformer whose secondary winding is connected inside a four arm bridge. When the bridge is balanced, its AC output is zero, and the C5 (or C7) receives no gate signal. The bridge's DC resistance is sufficiently low to stabilize the SCR during forward blocking periods.* If now the bridge is unbalanced by raising or lowering the thermistor's ambient temperature, an AC voltage will appear across the SCR's gate cathode terminals. Depending in which sense the bridge is unbalanced, positive gate voltage will be in phase with, or 180° out of phase with the AC şupply. If positive gate voltage is in phase, SCR will deliver load current through diode CR_1 to load (1), diode CR_2 blocking current to load (2). Conversely, if positive gate

*See Section 4.3.6 "Negative Gate Biasing."

voltage is 180° out of phase, diode CR_2 will conduct and deliver power to load (2), CR_1 being reverse biased under these conditions. CR_3 prevents excessive negative voltage from appearing across the SCR's gate/cathode terminals. With component values shown, the circuit will respond to changes in temperature of approximately 1–2°C. Substitution of other variable-resistance sensors, such as cadmium sulphide light dependent resistors (LDR) or strain gauge elements, for the thermistor shown is of course permissible. The balanced bridge concept of Figure 8.31 may also be used to trigger conventional SCR-series load combinations. As a low power temperature controller for instance, a C5 could be used to switch a heater element, with a thermistor providing temperature feedback information to the trigger bridge.

For more information on temperature controls see Chapter 12 on zero voltage switching.

8.12.2 Mercury Thermostat/SCR Heater Control

The mercury-in-glass thermostat is an extremely sensitive measuring instrument, capable of sensing changes in temperature as small as 0.1°C. Its major limitation lies in its very low current handling capability — for reliability and long life, contact current should be held below 1 mA. In the circuit of Figure 8.33 the General Electric C5B or C106B SCR serve as both current amplifier for the Hg thermostat and as the main load switching element.

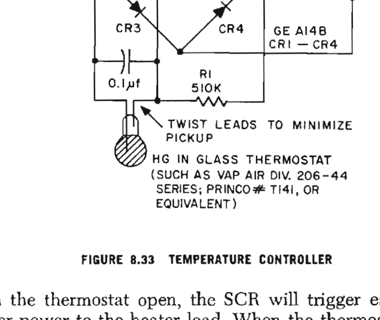


FIGURE 8.33 TEMPERATURE CONTROLLER

With the thermostat open, the SCR will trigger each half cycle and deliver power to the heater load. When the thermostat closes, the SCR can no longer trigger, and the heater shuts off. Maximum current through the thermostat in the closed position is less than 250 μA rms.

8.12.3 Touch Switch or Proximity Detector

The circuit shown in Figure 8.34 is actuated by an increase in capacitance between a sensing electrode and the ground side of the line. The sensitivity can be adjusted to switch when a human body is within inches of the insulated plate used as the sensing electrode. Thus, this circuit can be used as an electrically-isolated touch switch, or as a proximity detector in alarm circuits.

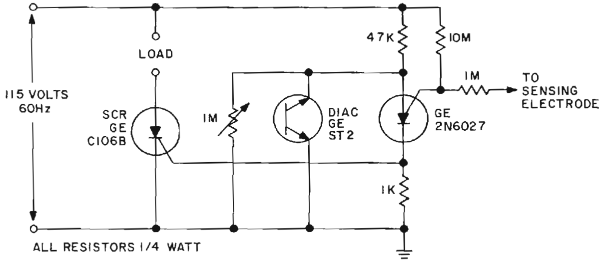


FIGURE 8.34 TOUCH SWITCH OR PROXIMITY DETECTOR

The GE 2N6027 Programmable Unijunction Transistor (PUT), will switch "ON" when the anode voltage exceeds the gate voltage by an amount known as the trigger voltage (approximately 0.5 volts). This anode voltage is clamped at the "ON" voltage of the diac (ST2). As the capacitance between the sensing electrode and ground increases (due to an approaching body), the angle of phase lag between the anode and gate voltages of the D13T increases until the voltage differential at some time is large enough to trigger this PUT. Because the anode voltage is clamped, it is larger only at the beginning of the cycle; hence, switching must occur early in the cycle, minimizing RFI.

Sensitivity is adjusted with the I megohm potentiometer which determines the anode voltage level prior to clamping. This sensitivity will be proportional to the area of the surfaces opposing each other.

8.12.4 Voltage Sensing Circuit

A low cost voltage or threshold detector is shown in Figure 8.35.

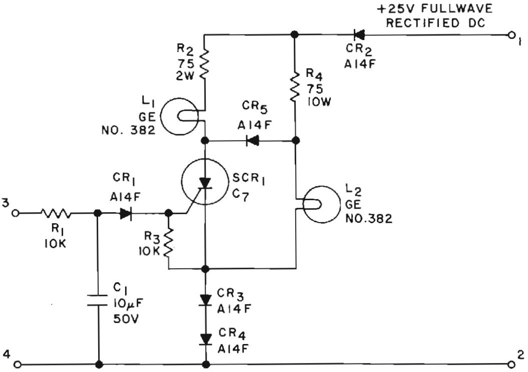


FIGURE 8.35 LOW COST VOLTAGE DETECTOR

When +25 V DC (full wave rectified) is applied between terminal #1 and 2, current will flow through R_4, L_2, CR_3 and CR_4. L_2 will be illuminated and L_1 will be dark. As soon as a voltage is applied between terminals #3 and 4 (3 positive) and a threshold of about 2.8 V is exceeded SCR_1 will turn on, actuating L_1. L_2 will be turned off because of CR_5.

The threshold voltage can be increased by adding more diodes to CR_1, CR_3 and CR_4 or replacing them by a zener diode.

This circuit is useful in detecting the voltage across an SCR in the on or off positions or indicating the output state of an operational amplifier, etc.

8.12.5 Single Source Emergency Lighting System

An emergency lighting system which maintains a 6 volt battery at full charge and switches automatically from the AC supply to the battery is shown in Figure 8.36.

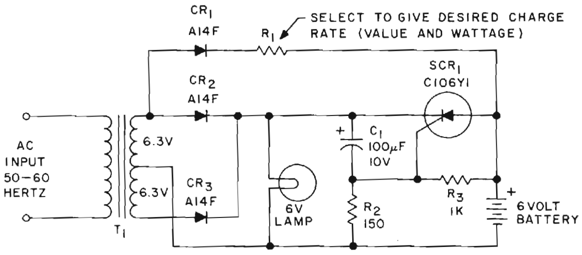


FIGURE 8.36 SINGLE SOURCE EMERGENCY LIGHTING SYSTEM

Transformer T_1 and diodes CR_2 and CR_3 supply DC voltage for the 6 V lamp load. CR_1 and R_1 supply the battery with charging current, which can be varied by R_1. The anode and gate of SCR_1 are kept at the battery voltage, while the cathode of SCR_1 is kept at a higher potential by C_1. Should the voltage on the cathode of SCR_1 fall below the battery voltage due to interruption of the AC input, SCR_1 will trigger and supply the lamp with power from the battery. When the AC reappears, SCR_1 will turn off automatically and the battery will re-recharge.

8.12.6 Liquid Level Control

When it is desirable to keep the fluid level of a liquid between two fixed points, this hybrid control is extremely useful. The control takes advantage of the best characteristics of both power semiconductors and electromechanical devices.

Two modes, for filling or emptying are possible by simply reversing the contact connections of K_1 as shown in Figure 8.37.

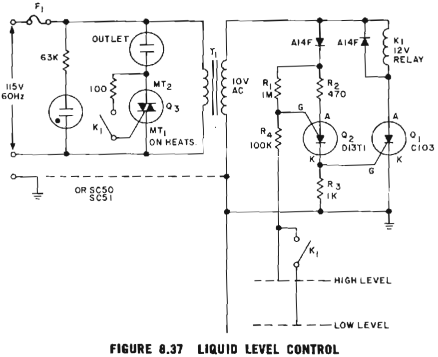


FIGURE 8.37 LIQUID LEVEL CONTROL

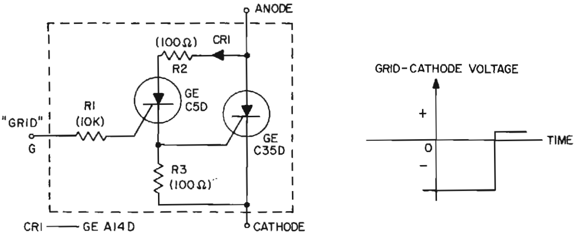
The loads can be either electric motors or solenoid operated valves, operating from AC power. Liquid level detection is accomplished by two metal probes, one measuring the high level and the other the low level.

The relay K_1 is energized by Q_1 which is controlled by Q_2, a PUT, whose gate form the detector. The PUT is normally off but when liquid rises to the high probe level, the impedance of the liquid creates a voltage divider and the PUT triggers. When the PUT conducts it turns on Q_1 which will pick up K_1. K_1 will turn on Q_3 activating the load and will also arm the low level probe which holds the circuit on until the liquid level drops below this probe. At this time the circuit is de-energized, turning off the load.

An inversion of the logic (keeping the container filled) can be accomplished by replacing the normally open contact on the gate of Q_3 with a normally closed contact.

8.13 THYRATRON REPLACEMENT

A thyratron tube is characterized by a very high signal input impedance, low pick-up and drop-out currents, and good power handling capabilities. On the other hand, it is fragile, requires filament power, is frequency limited by a long deionization time, and has a fairly high forward drop. While the solid-state equivalents to this device, using the C5 as a trigger element for a larger size SCR, can match the thyratron in input impedance, current handling ability and low pick-up current, they possess none of the gas tube's limitations. At the present time, however, the maximum forward blocking voltage attainable using a single C5 is 400 volts. This can be increased by series connecting additional SCR's (see Chapter 6).



(a) Equivalent Circuit

(b) Grid Voltage Waveforms

FIGURE 8.38 SIMPLE THYRATRON REPLACEMENT

Referring to Figure 8.38; with a negative potential on grid terminal "G", stabilizing gate bias is provided through R1 and R3 for the C5. When the "Grid" is driven positive, however, a maximum current of 200 microamps will trigger the smaller SCR into conduction. The C35D is triggered in turn by the C5, and can conduct up to 25 amps

rms load current. With the voltage grades shown, the "device" is capable of blocking voltages up to 400 volts. Over-all pick-up current is determined by the C5 rather than by the C35, a useful feature when the "thyratron" is operating into a highly inductive load. Diode CR_1 prevents transistor action in the C5 if positive grid voltage should coincide with negative anode potential.

General Electric is manufacturing the S26 and S27 solid state thyratrons which are 200 volt devices, but higher voltage devices such as the SL-3 and SL-4 and custom designs are available. (For more information on solid state thyratrons see also Reference 7.)

8.14 SWITCHING CIRCUITS USING THE C5 OR C106 SCR AS A REMOTE-BASE TRANSISTOR

8.14.1 "Nixie"® and Neon Tube Driver

The C5 SCR, when biased as a remote-base transistor (for detailed information on remote-base transistors see Chapter 1), makes an excellent high voltage transistor suitable for driving Nixie, neon and other type of high voltage digital readout displays. Collector voltage rating of the equivalent transistor equals or exceeds the $V_{BR(FX)}$ rating of the parent SCR (400 volts) while the common emitter current gain is approximately two (2). The circuit Figure 8.39 is self-explanatory; note however the connections to the C5 terminals. Where a memory feature is desirable (pulse initiation with load remaining energized until reset externally), the same basic circuit may be used, but with the C5 connected conventionally as an SCR.

® Trademark Burroughs Corporation.

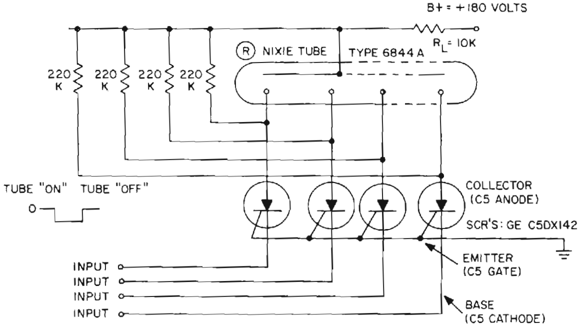
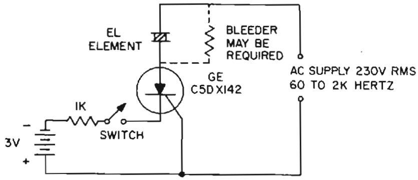


FIGURE 8.39 TRANSISTORIZED NIXIE® DRIVER

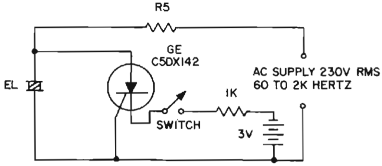
8.14.2 Electroluminescent Panel Driver

Either of the circuits of Figure 8.40 may be used to drive the elements of an electroluminescent display panel, depending on the input

logic required. Here, the high voltage capabilities of the C5 SCR are again combined with its usefulness as a transistor, in this case a *symmetrical* transistor, to control full-wave AC drive at high voltage and frequency, low current.



(a) Series Drive — No Signal, Display "Off"



(b) Shunt Drive — No Signal, Display "On"

FIGURE 8.40 ELECTROLUMINESCENT PANEL DRIVER

REFERENCES

1. "Using the Triac for Control of AC Power," J. H. Galloway, General Electric Company, Auburn, N. Y., Application Note 200.35.*
2. "Solid State Electric Heating Controls," R. W. Fox and R. E. Locher, General Electric Company, Auburn, N. Y., Application Note 200.58.*
3. "Regulated Battery Chargers Using the Silicon Controlled Rctifier," D. R. Grafham, General Electric Company, Auburn, N. Y., Application Note 200.33*
4. "Flashers, Ring Counters and Chasers," R. W. Fox, General Electric Company, Auburn, N. Y., Application Note 200.48.*
5. "Using Low Current SCR's," D. R. Grafham, General Electric Company, Auburn, N. Y., Application Note 200.19.*
6. "The D13T – A Programmable Unijunction Transistor Types 2N6027 and 2N6028," W. R. Spofford, Jr., General Electric Company, Syracuse, N. Y., Application Note 90.70.*
7. "The Solid State Thyratron," R. R. Rottier, General Electric Company, Auburn, N. Y., Application Note 200.36.*

***Refer to Chapter 23 for availability and ordering information.**

NOTES

9 AC PHASE CONTROL

9.1 PRINCIPLE OF PHASE CONTROL

"Phase Control" is the process of rapid ON-OFF switching which connects an AC supply to a load for a controlled fraction of each cycle. This is a highly efficient means of controlling the average power to loads such as lamps, heaters, motors, DC suppliers, etc. Control is accomplished by governing the phase angle of the AC wave at which the thyristor is triggered. The thyristor will then conduct for the remainder of that half-cycle.

There are many forms of phase control possible with the thyristor, as shown in Figure 9.1. The simplest form is the half-wave control of Figure 9.1(a) which uses one SCR for control of current flow in one direction only. This circuit is used for loads which require power con-

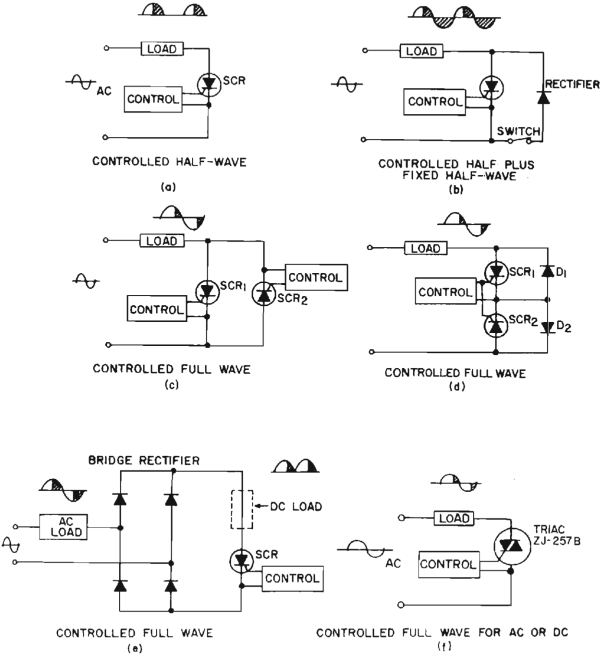


FIGURE 9.1 BASIC FORMS OF AC PHASE CONTROL

trol from zero to one-half of full-wave maximum and which also permit (or require) direct current. The addition of one rectifier, Figure 9.1(b), provides a fixed half-cycle of power which shifts the power control range to half-power minimum and full-power maximum but with a strong DC component. The use of two SCR's, Figure 9.1(c), controls from zero to full-power and requires isolated gate signals, either as two control circuits or pulse-transformer coupling from a single control. Equal triggering angles of the two SCR's produce a symmetrical output wave with no DC component. Reversible half-wave DC output is obtained by controlling symmetry of triggering angle.

An alternate form of full-wave control is shown in Figure 9.1(d). This circuit has the advantage of a common cathode and gate connection for the two SCR's. While the two rectifiers prevent reverse voltage from appearing across the SCR's, they reduce circuit efficiency by their added power loss during conduction.

The most flexible circuit, Figure 9.1(e), uses one SCR inside a bridge rectifier and may be used for control of either AC or full-wave rectified DC. Losses in the rectifiers, however, make this the least efficient circuit form, and commutation is sometimes a problem (see Section 9.3). On the other hand, using one SCR on both halves of the AC wave is a more efficient utilization of SCR capacity, hence the choice of circuit form is based on economic factors as well as performance requirements.

By far the most simple, efficient and reliable method of controlling AC power is the use of the bidirectional triode thyristor, the triac, as shown in Figure 9.1(f). Triac characteristics are discussed in Chapter 7. The fact that the triac is controlled in both directions by one gate and is self-protecting against damage by high-voltage transients has made it the leading contender for 120 and 240 VAC power control up to 6 KW at this writing.

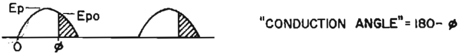
9.2 ANALYSIS OF PHASE CONTROL

Rectifiers and SCR's are rated in terms of *average* current since this is easily found by a DC ammeter. Most AC loads are more concerned, however, with the *RMS*, or effective, current, which is why triacs are rated in terms of RMS current.

Figures 9.2 and 9.3 show the relationships as a function of phase-angle, α, at turn-on, of average, RMS, and peak voltages as well as power in a resistive load. Since the SCR is a switch it will apply this voltage to the load, but the value of current will depend on load impedance.

As an example of the use of these charts, suppose it is desired to operate a 1200 watt resistive load, rated at 120 volts, from a 240 volt supply. Connection of this load directly to the supply would result in 4800 watts, therefore the desired operation is at ¼ maximum power capability. We may use, for this case, either a half-wave or full-wave form of control circuit.

Starting with the half-wave case and Figure 9.2, the ¼ power point is a triggering phase angle of 90 degrees. Peak output voltage E_{PO} is equal to peak input voltage, 1.41×240 volts or 340 volts.



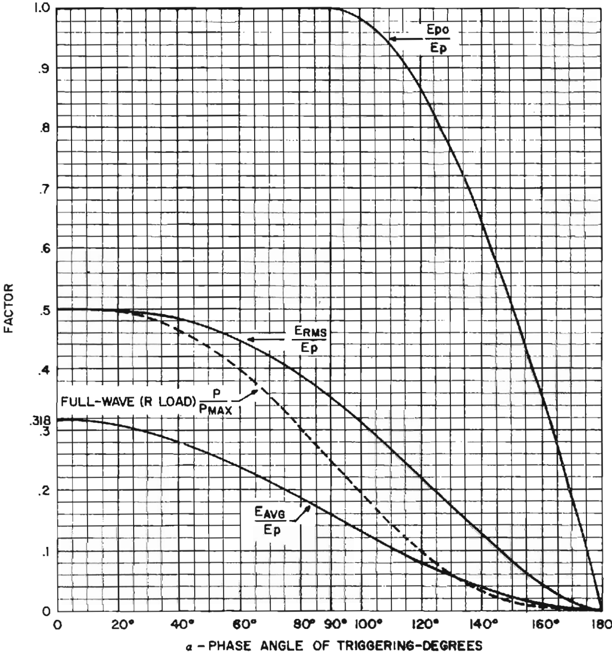


FIGURE 9.2 HALF-WAVE PHASE CONTROL ANALYSIS CHART

Oddly enough, the RMS voltage is .353 × 340 volts or 120 volts. Average voltage is .159 × 340 volts or 54 volts, which would be indicated by a DC voltmeter across the load. Since the load resistance is 12 ohms ($120^2/1200$), peak current is 340/12 = 28.3 amperes; RMS current is 120/12 = 10 amperes; and average current is 54/12 = 4.5 amperes, which would be indicated by a DC ammeter in series with the load. Power is $E_{RMS} \times I_{RMS}$ (since the load is pure resistance) which is 1200 watts. Note carefully that $E_{AVG} \times I_{AVG}$ is 243 but is *not* true power in the load. The SCR must be rated for 4.5 amperes (average) at a conduction angle (180 − α) of 90 degrees. Furthermore, the load must be able to accept the high peak voltage and current, and the line "power-factor" is 0.5 (if defined as $P_{LOAD} \div E_{LINE} \times I_{LINE\ RMS}$).

The other alternative is a symmetrical full-wave circuit, such as Figure 9.1(c), for which Figure 9.3 is used. The phase-angle of triggering is found to be 113 degrees for ¼ power. Peak voltage is .92 × 340 = 312 volts, only a slight reduction from the half-wave case. RMS voltage is again .353 × 340 = 120 volts. Average voltage is zero, presuming symmetrical wave form. RMS current is 10 amperes and power is 1200 watts, but peak current has been reduced to 26 amperes. To determine rating required of the two SCR's, each can be considered as a single half-wave circuit. From Figure 9.2, the average voltage, at 113 degrees, is .097 × 340 = 33 volts. Average current in each SCR is then 33/12 = 2.75 amperes at a conduction angle of 180 − 113 = 67 degrees.

In the case of a bridged SCR circuit, Figure 9.1(e), used for this same load, the average current through each rectifier is 2.75 amperes but the average current through the SCR is 5.5 amperes, corresponding to a total conduction angle of 134 degrees.

If a triac were used, its RMS current would of course be 10 amperes with a conduction angle of 67 degrees each half cycle, for a total conduction angle of 113 degrees. This corresponds to either two SCR's in inverse parallel or one SCR and four diodes in a bridge, but the triac has reduced the power components to just one.

Of particular importance to note in the analysis charts is the non-linearity of these curves. The first and last 30 degrees of each half-cycle contribute only 6 per cent (1.5% each) of the total power in each cycle. Consequently, a triggering range from 30° to 150° will produce a power-control range from 3% to 97% of full power, excluding voltage drop in the semiconductors.

Figure 9.4 shows a large variety of SCR circuits for the control of DC and AC loads, along with the appropriate equations for voltages and currents. This information may be used in the selection of the best circuit for a particular use, and for determining the proper ratings of the semiconductors. Figure 9.4 is from reference 8, which also gives the approach for derivation of the equations shown in the chart.

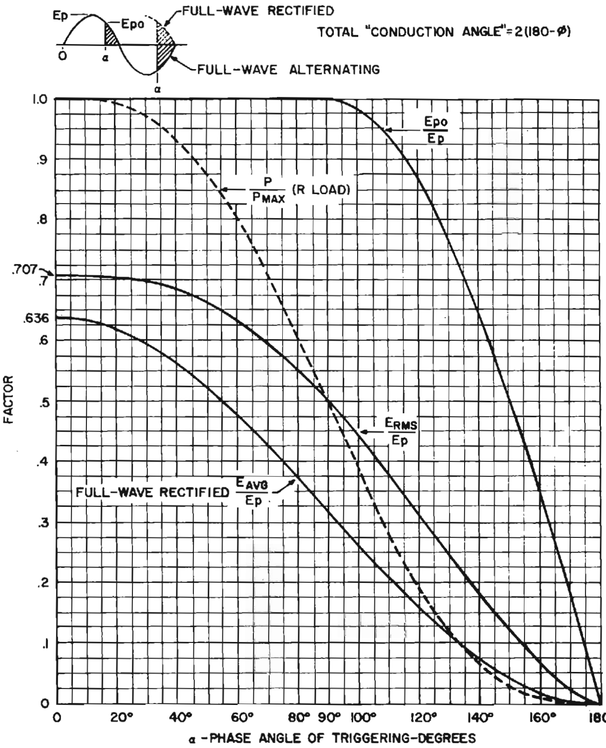
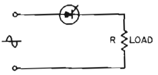
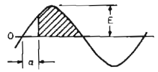
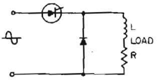
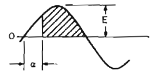
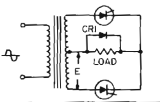
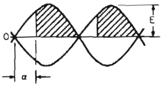
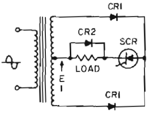
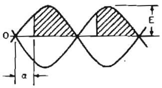
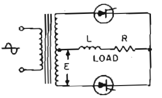
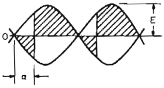
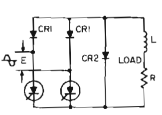
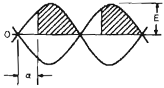


FIGURE 9.3 SYMMETRICAL FULL-WAVE PHASE CONTROL ANALYSIS CHART

CIRCUIT (a) NAME	CIRCUIT (b) CONNECTIONS	(c) LOAD VOLTAGE WAVEFORMS	(d) PEAK FORWARD VOLTAGE ON SCR	PEAK REVERSE VOLTAGE (e) ON SCR	PEAK REVERSE VOLTAGE (f) ON DIODE	(g) MAX. LOAD VOLTAGE ($\alpha = 0$) E_D = AVERAGE D-C VALUE E_a = RMS A-C VALUE
(1) HALF-WAVE RESISTIVE LOAD			E	E	—	$E_D = \frac{E}{\pi}$ $E_a = \frac{E}{2}$
(2) HALF-WAVE INDUCTIVE LOAD WITH FREE-WHEELING RECTIFIER			E	E	E	$E_D = \frac{E}{\pi}$
(3) CENTERTAP WITH RESISTIVE LOAD, OR INDUCTIVE LOAD WITH FREE-WHEELING RECTIFIER			E (POSSIBLY 2E IF LOAD OPEN)	2E	E	$E_D = \frac{2E}{\pi}$
(4) CENTERTAP WITH RESISTIVE OR INDUCTIVE LOAD–SCR IN D-C CIRCUIT			E	0	2E ON CRI / E ON CR2	$E_D = \frac{2E}{\pi}$
(5) CENTERTAP WITH INDUCTIVE LOAD (NO FREE-WHEELING RECTIFIER)			2E	2E	—	$E_D = \frac{2E}{\pi}$
(6) SINGLE-PHASE BRIDGE WITH 2 SCR'S WITH COMMON ANODE OR CATHODE. RESISTIVE LOAD, OR INDUCTIVE LOAD WITH FREE-WHEELING RECTIFIER			E	E	E (CRI AND CR2)	$E_D = \frac{2E}{\pi}$

† ASSUMES ZERO FORWARD DROP IN SEMICONDUCTORS WHEN CONDUCTING, AND ZERO CURRENT WHEN BLOCKING; ALSO ZERO a-c LINE AND SOURCE REACTANCE. INDUCTIVE d-c LOADS HAVE PURE d-c CURRENT.

FIGURE 9.4 CIRCUIT CONSTANTS OF SOME MAJOR PHASE CONTROLLED CIRCUITS FOR DC LOADS†

(h) LOAD VOLTAGE VS TRIGGER DELAY ANGLE α	(j) TRIGGER ANGLE RANGE FULL ON TO FULL OFF	MAX STEADY-STATE CURRENT IN SCR (k) AVERAGE AMP	(l) COND ANGLE	MAX STEADY-STATE CURRENT IN DIODE RECTIFIER (m) AVERAGE AMP	(n) COND ANGLE FOR MAX CURRENT	(p) ABILITY TO PUMPBACK INDUCTIVE LOAD ENERGY TO SUPPLY LINE	(q) FUNDAMENTAL FREQUENCY OF LOAD VOLTAGE (f = SUPPLY FREQUENCY)	(r) NOTES AND COMMENTS
$E_D = \frac{E}{2\pi}(1+\cos\alpha)$ $E_a = \frac{E}{2\sqrt{\pi}}(\pi-\alpha+\frac{1}{2}\sin 2\alpha)^{1/2}$	180°	$\frac{E}{\pi R}$	180°	—	—	—	f	
$E_D = \frac{E}{2\pi}(1+\cos\alpha)$	180°	$\frac{E}{2\pi R}$ (LOAD HIGHLY INDUCTIVE)	180°	$0.54(\frac{E}{\pi R})$	210°	NO	f	
$E_D = \frac{E}{\pi}(1+\cos\alpha)$	180°	$\frac{E}{\pi R}$	180°	$0.26(\frac{2E}{\pi R})$	148°	NO	2f	
$E_D = \frac{E}{\pi}(1+\cos\alpha)$	180°	$\frac{2E}{\pi R}$	360°	$CR1 = \frac{E}{\pi R}$ $CR2 = 0.26(\frac{2E}{\pi R})$ WITH HIGHLY INDUCTIVE LOAD	180° 148°	NO	2f	CR2 NECESSARY WHEN LOAD IS NOT PURELY RESISTIVE. FREQUENCY LIMITED BY RECOVERY CHARACTERISTICS OF RECTIFIERS AND SCR.
$E_D = \frac{2E}{\pi}\cos\alpha$ (ASSUMING CONTINUOUS CURRENT IN LOAD)	180°	$\frac{E}{\pi R}$	180°	—	—	YES	2f	
$E_D = \frac{E}{\pi}(1+\cos\alpha)$	180°	$\frac{E}{\pi R}$	180°	$CR1 = \frac{E}{\pi R}$ $CR2 = 0.26(\frac{2E}{\pi R})$	180° 148°	NO	2f	WITHOUT CR2, SCR'S MAY BE UNABLE TO TURN OFF AN INDUCTIVE LOAD. ALSO, CR2 RELEIVES SCR'S FROM FREEWHEELING DUTY.

FIGURE 9.4 (CONTINUED)

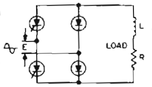
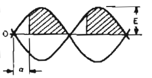
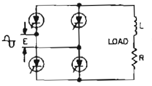
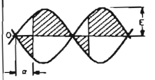
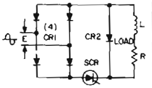
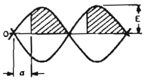
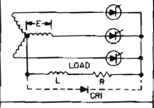
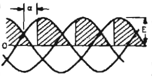
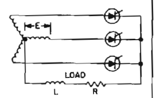
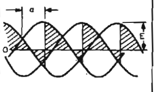
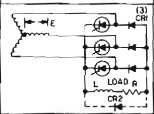
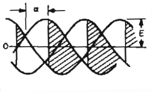
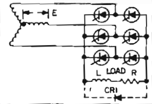
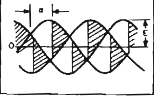
CIRCUIT (a) NAME	CIRCUIT (b) CONNECTIONS	LOAD VOLTAGE WAVEFORMS	(d) PEAK FORWARD VOLTAGE ON SCR	PEAK REVERSE VOLTAGE (e) ON SCR	PEAK REVERSE VOLTAGE (f) ON DIODE	(g) MAX. LOAD VOLTAGE ($\alpha = 0$) E_D = AVERAGE D-C VALUE E_A = RMS A-C VALUE
(7) SINGLE-PHASE BRIDGE WITH 2 SCR'S ON COMMON A-C LINE, RESISTIVE OR INDUCTIVE LOAD			E	E	E	$E_D = \frac{2E}{\pi}$
(8) SINGLE-PHASE BRIDGE WITH 4 SCR'S AND INDUCTIVE LOAD			E	E	–	$E_D = \frac{2E}{\pi}$
(9) SINGLE-PHASE BRIDGE WITH SINGLE SCR IN D-C CIRCUIT. RESISTIVE OR INDUCTIVE LOAD.			E	0	E (CR1 AND CR2)	$E_D = \frac{2E}{\pi}$
(10) THREE-PHASE HALF-WAVE WITH RESISTIVE LOAD OR INDUCTIVE LOAD WITH FREE-WHEELING RECTIFIER			E (POSSIBLY $\sqrt{3}$ E IF LOAD OPEN AND IF SCR'S HAVE HIGH REVERSE CURRENTS	$\sqrt{3}$E	E	$E_D = \frac{3\sqrt{3}E}{2\pi}$
(11) THREE-PHASE HALF-WAVE WITH INDUCTIVE LOAD (NO FREE-WHEELING RECTIFIER)			$\sqrt{3}$ E	$\sqrt{3}$E	–	$E_D = \frac{3\sqrt{3}E}{2\pi}$
(12) THREE-PHASE BRIDGE WITH 3 SCR'S RESISTIVE LOAD OR INDUCTIVE LOAD WITH FREE-WHEELING RECTIFIER			$\sqrt{3}$ E	$\sqrt{3}$E	$\sqrt{3}$ E	$E_D = \frac{3\sqrt{3}E}{\pi}$
(13) THREE-PHASE BRIDGE WITH 6 SCR'S. RESISTIVE LOAD, OR INDUCTIVE LOAD WITH FREE-WHEELING RECTIFIER			$\sqrt{3}$ E (1.5 E IF SCR'S SHUNTED BY RESISTANCE)	$\sqrt{3}$ E	$\sqrt{3}$ E	$E_D = \frac{3\sqrt{3}E}{\pi}$

FIGURE 9.4 (CONTINUED)

(h) LOAD VOLTAGE VS TRIGGER DELAY ANGLE α	(j) TRIGGER ANGLE RANGE FULL ON TO FULL OFF	MAX STEADY-STATE CURRENT IN SCR (k) AVERAGE AMP	(l) COND ANGLE	MAX STEADY-STATE CURRENT IN DIODE RECTIFIER (m) AVERAGE AMP	(n) COND ANGLE FOR MAX CURRENT	(p) ABILITY TO PUMPBACK INDUCTIVE LOAD ENERGY TO SUPPLY LINE	(q) FUNDAMENTAL FREQUENCY OF LOAD VOLTAGE (f = SUPPLY FREQUENCY)	(r) NOTES AND COMMENTS
$E_D = \frac{E}{\pi}(1+\cos\alpha)$	180°	$\frac{E}{\pi R}$	180°	$\frac{E}{\pi R}$	180°	NO	2f	DIODE RECTIFIERS ACT AS FREE-WHEELING PATH, CONDUCT $(\pi + \alpha)$ DEGREES WITH INDUCTIVE LOAD.
$E_D = \frac{2E}{\pi}\cos\alpha$ (ASSUMING CONTINUOUS CURRENT IN LOAD)	180°	$\frac{E}{\pi R}$	180°	—	—	YES	2f	WITH RESISTIVE LOAD OPERATION IS SAME AS CIRCUIT (7)
$E_D = \frac{E}{\pi}(1+\cos\alpha)$	180°	$\frac{2E}{\pi R}$	360°	$CR1 = \frac{E}{\pi R}$ $CR2 = 0.16\left(\frac{2E}{\pi R}\right)$	180° 148°	NO	2f	CR2 NECESSARY WHEN LOAD IS NOT PURELY RESISTIVE, FREQUENCY LIMITED BY RECOVERY CHARACTERISTICS OF RECTIFIERS AND SCR'S
$E_D = \frac{3\sqrt{3}E}{2\pi}\cos$ $(0 < \alpha < 30°)$ $E = \frac{3E}{2\pi}\left[1 + \cos(\alpha + 30°)\right]$ $(30° < \alpha < 150°)$	150°	$\frac{\sqrt{3}E}{2\pi R}$	120°	$0.16\left(\frac{3\sqrt{3}E}{2\pi R}\right)$	134°	NO	3f	
$E_D = \frac{3\sqrt{3}E}{2}\cos$ (ASSUMING CONTINUOUS CURRENT IN LOAD)	150°	$\frac{\sqrt{3}E}{2\pi R}$	120°	—	—	YES	3f	
$E_D = \frac{3\sqrt{3}E}{2\pi}(1+\cos\alpha)$	180°	$\frac{\sqrt{3}E}{\pi R}$	120°	$CR1 = \frac{\sqrt{3}E}{\pi R}$ $CR2 = 0.14\left(\frac{3\sqrt{3}E}{\pi R}\right)$	120° 132°	NO	3f	WITHOUT CR2, SCR'S MAY BE UNABLE TO TURN OFF AN INDUCTIVE LOAD, ALSO CR2 RELIEVES SCR'S FROM FREE-WHEELING DUTY
$E_D = \frac{3\sqrt{3}E}{\pi}\cos$ $(0 < \alpha < 60°)$ $E_D = \frac{3\sqrt{3}E}{\pi}\left(1 + \frac{\cos\alpha}{2} - \frac{\sqrt{3}}{2}\sin\alpha\right)$ $(60° < \alpha < 120°)$	120°	$\frac{\sqrt{3}E}{\pi R}$	120°	$0.056\left(\frac{3\sqrt{3}E}{\pi R}\right)$	212°	NO	6f	SCR'S REQUIRE TWO GATE SIGNALS 60° APART EACH CYCLE, ALTERNATELY A GATE SIGNAL DURATION > 60°

FIGURE 9.4 (CONTINUED)

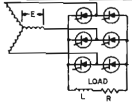
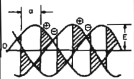
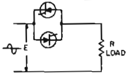
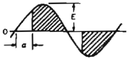
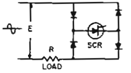
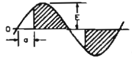
CIRCUIT (a) NAME	CIRCUIT (b) CONNECTIONS	(c) LOAD VOLTAGE WAVEFORMS	(d) PEAK FORWARD VOLTAGE ON SCR	PEAK REVERSE VOLTAGE (e) ON SCR	PEAK REVERSE VOLTAGE (f) ON DIODE	(g) MAX LOAD VOLTAGE ($\alpha = 0$) E_D = AVERAGE D-C VALUE, E_a = RMS A-C VALUE	(h) LOAD VOLTAGE VS TRIGGER DELAY ANGLE α	(j) TRIGGER ANGLE RANGE FULL ON TO FULL OFF	MAX STEADY-STATE CURRENT IN SCR (k) AVERAGE AMP	MAX STEADY-STATE CURRENT IN SCR (l) COND ANGLE	MAX STEADY-STATE CURRENT IN DIODE RECTIFIER (m) AVERAGE AMP	MAX STEADY-STATE CURRENT IN DIODE RECTIFIER (n) COND. ANGLE FOR MAX CURRENT	(p) ABILITY TO PUMPBACK INDUCTIVE LOAD ENERGY TO SUPPLY LINE	(q) FUNDAMENTAL FREQUENCY OF LOAD VOLTAGE (f = SUPPLY FREQUENCY)	(r) NOTES AND COMMENTS
(14) THREE-PHASE BRIDGE WITH 6 SCR'S WITH INDUCTIVE LOAD			$\sqrt{3}E$ (1.5E IF SCR'S SHUNTED BY RESISTANCE)	$\sqrt{3}E$	—	$E_D = \frac{3\sqrt{3}E}{\pi}$	$E_D = \frac{3\sqrt{3}E}{\pi} \cos \alpha$ (ASSUMING CONTINUOUS CURRENT IN LOAD)	120°	$\frac{\sqrt{3}E}{\pi R}$	120°	—	—	YES	6f	SCR'S REQUIRE TWO GATE SIGNALS 60° APART EACH CYCLE, ALTERNATELY A GATE SIGNAL DURATION > 60°
AC RESISTIVE LOADS															
(15) TRIAC OR INVERSE PARALLEL SCR'S WITH RESISTIVE LOAD			E	E	—	$E_a = \frac{E}{\sqrt{2}}$	$E_a = \frac{E}{\sqrt{2\pi}}(\pi - \alpha + \frac{1}{2} \text{SIN. } 2\alpha)^{1/2}$	180°	$\frac{E_a}{2.2R}$ OR $\frac{E}{\pi R}$	180°	—	—	—	f	WITH INDUCTIVE LOAD, LOAD VOLTAGE AND CURRENT DEPEND ON $\omega L/R$ AS WELL AS R AND α.
(16) SCR INSIDE BRIDGE WITH A-C RESISTIVE LOAD			E	0	E	$E_a = \frac{E}{\sqrt{2}}$	$E_a = \frac{E}{\sqrt{2\pi}}(\pi - \alpha + \frac{1}{2} \text{SIN } 2\alpha)^{1/2}$	180°	$\frac{E_a}{1.1R}$ OR $\frac{2E}{\pi R}$	360°	$\frac{E_a}{2.2R}$ OR $\frac{E}{\pi R}$	180°	—	f	INDUCTANCE IN D-C CIRCUIT MUST BE MINIMUM. FREQUENCY LIMIT DETERMINED BY RECOVERY CHARACTERISTICS OF RECTIFIERS AND SCRS WITH INDUCTIVE LOAD, LOAD VOLTAGE AND CURRENT DEPEND ON $\omega L/R$ AS WELL AS R AND α.

FIGURE 9.4 (CONTINUED)

9.2.1 AC Inductive Load Phase Control

The above discussion considered a phase controlled resistive load and using Figures 9.2 and 9.3 derived the required information to properly size the SCR's. In the real world most loads have some amount of inductance. Motors, solenoids; transformers and even some "resistive" heaters have inductive components as a part of their impedance. The effect of this reactance is that the RMS to average current ratio is lowered. In lowering this ratio, the dissipation of the device is also lowered and higher average currents can be safely passed through the SCR.

Figure 9.5 shows inverse parallel SCR's controlling a resistive load. Also shown are the associated current and voltage waveforms. The average current through either SCR is the average of that portion of the load-current waveform either above or below zero. It is on this waveform of current that the SCR rating is based.

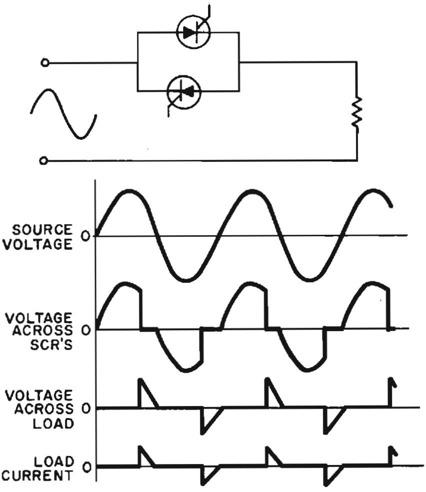


FIGURE 9.5 FULL-WAVE PHASE CONTROL OF RESISTIVE LOAD

Figure 9.6 shows such a rating. This is a curve of the average current versus maximum case temperature for a 235 ampere (RMS), C180 type SCR. Note that for different retard angles (nonconducting portion of the cycle) the maximum-allowable average current differs. This is due to the form factor (RMS/avg) changing with retard angle. Figure 9.7 shows how form factor changes with retard angle for a resistive load. Let's coordinate Figures 9.6 and 9.7. Note from Figure 9.7 that at 0 degree retard angle (full-cycle conduction) the form factor is 1.57. In order to maintain the maximum rated 235 Amps (RMS), the

average current must be limited to 150 amperes average (235/1.57 = 150). At 150 degree retard angle, the form factor is approximately 4, thus dictating a maximum average current of approximately 60 Amps.

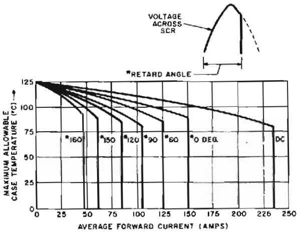


FIGURE 9.6 AVERAGE FORWARD CURRENT VERSUS CASE TEMPERATURE FOR TYPE C180 SCR

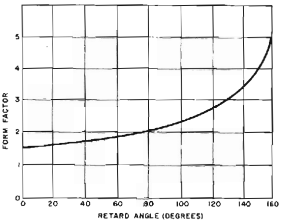


FIGURE 9.7 FORM FACTOR VERSUS RETARD ANGLE FOR PHASE-CONTROLLED RESISTIVE LOAD

If the load is slightly inductive, as in Figure 9.8, the waveforms change as shown. Note that the current waveform has been "softened" considerably. As expected, this softening improves (lowers) the form factor because the peak of the current waveform is reduced and its duration extended. Figure 9.9 shows the variation of form factor with

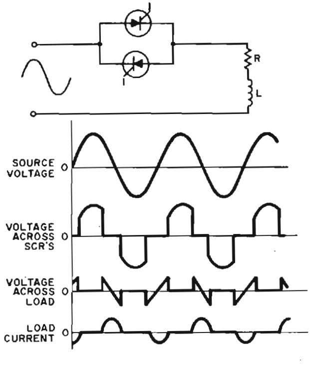


FIGURE 9.8 FULL-WAVE PHASE CONTROL OF INDUCTIVE LOAD

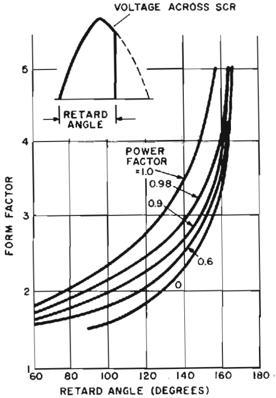


FIGURE 9.9 FORM FACTOR VERSUS RETARD ANGLE FOR PHASE-CONTROLLED LOADS OF DIFFERENT POWER FACTORS

retard angle for loads of different lagging power factor. Note the significant improvement in form factor at large retard angles with a slightly inductive load. At a retard angle of 150 degrees, a 25-percent reduction (improvement) in form factor is realized by changing the load power factor from unity to 0.9 inductive; better than 15-percent reduction in form factor is realized from a 0.98 power-factor load. Form factor decreases even more for power factors less than 0.9. This improvement in average-current capability at large retard angles can be quite significant. This is particularly true when using high-current SCR's, where 10, 20 or 40 Amps of additional capability can be a substantial economic factor. With the introduction of high-voltage (1000v to 2600v) SCR's, this additional current capability represents a substantial amount of additional kva handling capability.

Now you might say, "This is all fine, but I'm still saddled with the same old rating curves." This is true, but there's a suggestion on how to use these curves when the load is somewhat inductive. The procedure for determining the approximate amount of increase is as follows:

A. Average Current Versus Case Temperature
   1. Locate curve on spec sheet for retard angle in question.
   2. Determine new maximum average current from relationship.

$$I_{avg(max)} = \frac{I_{rms(max)}}{F_{PF,\alpha}}$$

where:

$I_{rms(max)}$ = Maximum-rms-current rating of SCR (from spec sheet)

$F_{PF,\alpha}$ = Form factor at given lagging power factor (PF) and retard angle (α)

   3. Draw maximum-average-current cutoff line as shown in Figure 9.10
   4. Plot remainder of curve by determining distance X:

$$X(°C) = \left(\frac{F_{PF,\alpha}}{F_{1.0,\alpha}}\right)(T_{c(max)} - T_{c(ss)})$$

$F_{PF,\alpha}$ = Form factor for power factor and retard angle in question

$F_{1.0,\alpha}$ = Form factor for *unity* power factor and retard angle in question

$T_{c(max)}$ = Max allowable case temperature

$T_{c(ss)}$ = Case temperature curve from spec sheet

B. Average Current Versus Average Power Dissipation
   1. Locate curve from spec sheet for retard angle in question.
   2. Mark maximum average current on curve as previously calculated in A.2. See Figure 9.11.
   3. Plot curve by determining distance Y:

$$Y\,(\text{watts}) = \left(\frac{F_{PF,\alpha}}{F_{1.0,\alpha}}\right)P_{ss}$$

where:

P_{ss} = Power dissipation curve from spec sheet

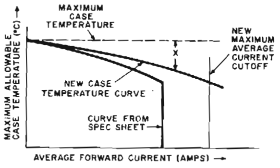


FIGURE 9.10

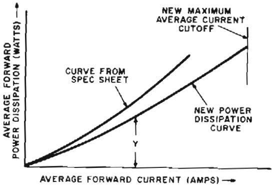


FIGURE 9.11

Figure 9.12 shows a set of actual curves for the C180 used with a 0.9 P.F. load at 150° conduction. Note the 25% improvement in current carrying capability and reduced power dissipation.

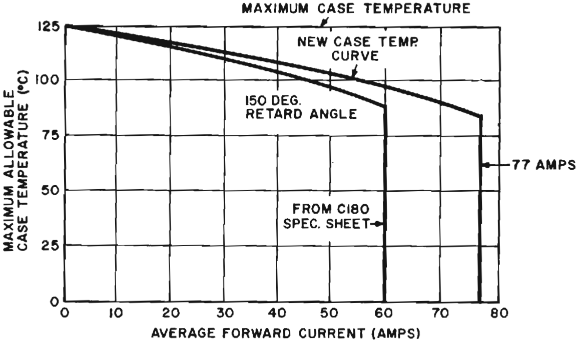


FIGURE 9.12(a)

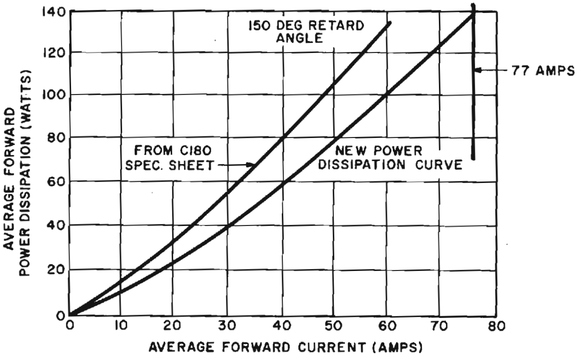
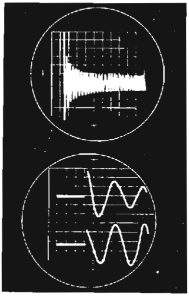


FIGURE 9.12(b)

9.2.2 Using Thyristors on Incandescent Lamp Loads

When incandescent lamps are switched on, there is a large current surge for the first several cycles. The ratio of surge or inrush to operating currents are, theoretically, inversely proportional to the filament's hot to cold resistance. Typical supply circuits of 100 to 200 kva capacity have given inrush currents of up to 25 times operating current. Time constants of inrush current decay for typical large lamps are on the order of 5 to 20 cycles of 60 Hertz line frequency.

Figure 9.13 shows a typical oscillogram of a GE 1500 watt projection lamp inrush current.



(a) Decay of Inrush Current (Scale: 40 A/Division)

(b) Top: Inrush Current
Bottom: Voltage Showing Switch Closure at Approximately 85 Electrical Degrees
(Current Scale: 100 A/Division)

FIGURE 9.13 INCANDESCENT LAMP INRUSH CURRENT

From Figure 9.13 it can readily be seen that the inrush surge is an important consideration. Thyristors typically have a capability for inrush for ratios of inrush to operating current anywhere from 8:1 to 12:1. It is important to note that lamp inrushes can be considerably higher. Table 9.1 presents lamp theoretical inrush currents for several of the more common lamps. In order to allow the designer to properly allow for this inrush Table 9.2 shows a list of recommendations of which thyristors should be used for a given lamp load.

Wattage	Rated Voltage	Type	Amps. Steady State Rated Voltage	Hot/Cold Resistance Ratio	Theoretical Peak Inrush (170 V pk) (Amps)
6	120	Vacuum	0.050	12.4	0.88
25	120	Vacuum	0.21	13.5	4.05
60	120	Gas Filled	0.50	13.9	9.70
100	120	Gas Filled	0.83	14.3	17.3
100 (proj)	120	Gas Filled	0.87	≅15.5	19.4
200	120	Gas Filled	1.67	16.0	40.5
300	120	Gas Filled	2.50	15.8	55.0
500	120	Gas Filled	4.17	16.4	97.0
1000	120	Gas Filled	8.3	16.9	198.0
1000 (proj)	115	Gas Filled	8.7	≅18.0	221.0

TABLE 9.1 Inrush Characteristics of Several Common Lamps

This table has been subdivided into four columns showing both 120 and 240 volt wattages. The table is then further divided into house wiring and industrial/commercial wiring. The house wiring column includes the limiting effect of a standard 20 ampere household circuit, whereas the industrial/commercial column assumes a zero impedance line. The final assumption of the table is that the lamps are normal incandescent lights and not high brightness types such as are used in projection systems. To use the projection bulbs the thyristor capability must be reduced *at least* an additional 10%.

	PERMISSIBLE LAMP WATTAGE			
	120 Volt Line		240 Volt Line	
Devices	House Wiring	Industrial/ Commercial Wiring	House Wiring	Industrial/ Commercial Wiring
Two C103's *	60	60		
Two C106's *	150	150	300	300
SC35/36	360	180	720	360
SC40/41, SC240/241	600	250	1,200	500
SC141	600	480	1,200	960
SC45/46, SC245/246	1,000	450	2,000	900
SC146	1,000	600	2,000	1,200
SC50/51, SC250/251	1,200	600	2,400	1,200
SC60	2,000	1,300	4,000	2,600
Two C45/46's		3,400		7,800
Two C50/52's		5,000		10,000
Two C350's		7,500		15,000
Two C178's		12,500		25,000
Two C180's		17,500		35,000
Two C290/1's		27,500		55,000
Two C530's		50,000		100,000

* Ballast Resistor Must Be Used In Series With Load—See Application Note 200.53.

TABLE 9.2 Maximum Lamp Wattage For Thyristors

9.3 COMMUTATION IN AC CIRCUITS

Commutation of the thyristor in AC circuits is usually no problem because of the normal periodic reversal of supply voltage. There are cases, however, which can lead to failure to commutate properly as the result of insufficient time for turn-off, or of excessive dv/dt of reapplied forward voltage, or both. Supply frequency and voltage, and inductance in load or supply, are determining factors.

Consider the inverse-parallel SCR circuit of Figure 9.14, with an inductive load. At the time that current reaches zero so that the conducting SCR can commutate (point A), a certain supply voltage exists which must then appear as a forward bias across the other SCR. The rate-of-change of this voltage is dependent on inductance and capacitance in the load circuit, as well as on reverse recovery characteristics of the SCR's. In certain cases, an L di/dt transient may be observed as the result of the SCR turning off when current drops below holding current, I_H. The addition of a series RC circuit in parallel with the SCR's, or with the load, can reduce the dv/dt to acceptable limits. The magnitude of C is determined by the load impedance and the dv/dt limitation of the SCR. The value of R should be such as to damp any LC oscillation, with a minimum value determined by the repetitive peak SCR current produced when the SCR's discharge the capacitor. Design data for dv/dt protection circuits is covered in depth in Section 16.3

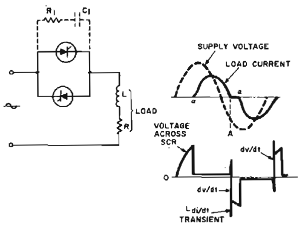


FIGURE 9.14 SUPPRESSION OF DV/DT AND TRANSIENTS FOR INDUCTIVE LOAD

An alternate solution is, obviously, the use of SCR's capable of turning off in a short time with a high applied dv/dt and a high voltage. In high-power circuits, this is often the best approach because of the size and cost of adequate RC networks.

Inductive AC loads in the bridged SCR circuit of Figure 9.15 have a slightly different effect. The rapid reversal of voltage at the input terminals of the bridge rectifier not only represents a high dv/dt, but it also reduces the time available for commutation. If the rectifiers used in the bridge have slow reverse-recovery time, compared with turn-off time of the SCR, the reverse-recovery current is usually enough to provide adequate time for commutation. Where this is not practical, a series R_1C_1 circuit at the input terminals of the bridge may be used. An atlernate form of suppression is to use R_2C_2 across the SCR, which will limit dv/dt, but a resistor R_3 is then required to provide a circulating current path (for current on the order of I_H) to allow sufficient commutating time. If capacitor C_2 is large, it can provide holding current to the SCR during the normal commutation period, and thus prevent turn-off until the capacitor is discharged.

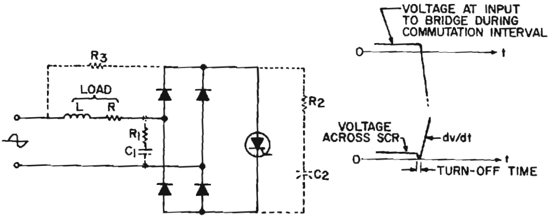


FIGURE 9.15 SUPPRESSION OF DV/DT AND INCREASING TURN-OFF TIME

The inductive AC load has a similar effect upon the commutation of the triac, and the solution is to either obtain a faster triac or suppress dv/dt with an RC network. This is discussed further in Section 16.3.

Inductive DC loads often require the addition of a free-wheeling diode, D_1 in Figure 9.16, to maintain current flow when the SCR is OFF. When an inductive DC load is used in the bridge circuit, Figure 9.16(c), the inductance causes a holding current to flow through the SCR and the bridge rectifier during the time line voltage goes through zero, preventing commutation. The addition of a free-wheeling diode, D_1, is required to by-pass this current around the SCR. The average current rating required for the diode D_1 is ½ maximum average load current for (a) and ¼ maximum average load current for (b) and (c).

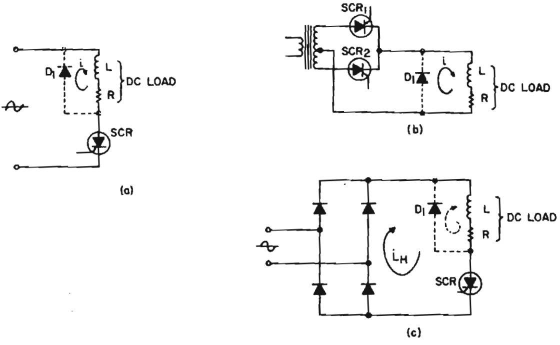


FIGURE 9.16 FREE-WHEELING DIODE BY-PASSES HOLDING CURRENT

9.4 BASIC TRIGGER CIRCUITS FOR PHASE CONTROL

Any of the relaxation oscillator pulse generators described in Chapter 4 may be adapted to phase control work. Since these are simply timing circuits, provision must be made for synchronizing them with the AC supply. This is usually done by taking the oscillator input voltage from the supply. There are many ways of connecting the various versions of the basic oscillator circuit, using the different semiconductor triggering devices and the thyristor, supply, and load circuits. Each combination has unique properties which must be considered in the selection of a circuit to perform a desired function.

9.4.1 Half-Wave Phase Control

The circuit of Figure 9.17 uses the basic relaxation oscillator to trigger the SCR at controlled triggering angles, α_t, during the positive half-cycles of line voltage. Since the adjustable resistor R_1 may go to zero resistance, diode D_1 is used to protect the triggering device and the gate of the SCR during the negative half-cycles. Certain triggering devices will permit the use of a fixed resistor R_2 instead of the diode, as will be shown later.

The waveforms of supply voltage, e, and voltage V_C, across the capacitor are shown in Figure 9.18. The magnitudes of R_1, C, E_p, and V_S determine the rate of charging the capacitor and the phase angle, α_t, at which triggering occurs. The earliest and latest possible triggering angles which can be obtained are indicated by α_1 and α_2 on the waveforms of Figure 9.18. If the switching current, I_S (see Chapter 4), of the trigger device is considered, the following relationships exist:

$$V_S = E_p \sin \alpha_1 \tag{9.1}$$

and

$$V_S + I_S R_1 = E_p \sin \alpha_2 \tag{9.2}$$

Since the maximum useful value of R_1 produces triggering at α_2, R_1 may be calculated for given values of e, C and V_S, but ignoring I_S for the moment, using the following equation:

$$R_1 = \frac{2\,E_p}{\omega C\,(V_S - V_O)} \tag{9.3}$$

Conversely, the peak voltage across the capacitor is

$$V_{CP} = \frac{2\,E_p}{\omega R_1\,C} + V_O \tag{9.4}$$

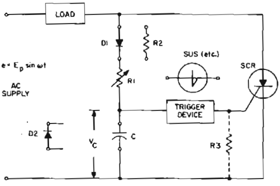


FIGURE 9.17 BASIC HALF-WAVE PHASE CONTROL CIRCUIT

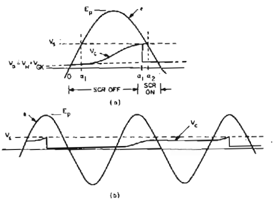


FIGURE 9.18 WAVE FORMS FOR FIGURE 9.17 (WITH D, AND SUS)

Equations 9.3 and 9.4 assume a low value of V_S compared with E_p, as would be the case when using an SUS trigger device on a 120 volt AC line.

From equation 9.4 it can be seen that the residual (or initial) voltage, V_O, left on the capacitor has a pronounced effect upon this simple trigger circuit. The residual voltage, V_O, is usually the sum of the minimum holding voltage, V_H, of the trigger, and the gate-to-cathode source voltage, V_{GK}, which appears when the SCR turns on.

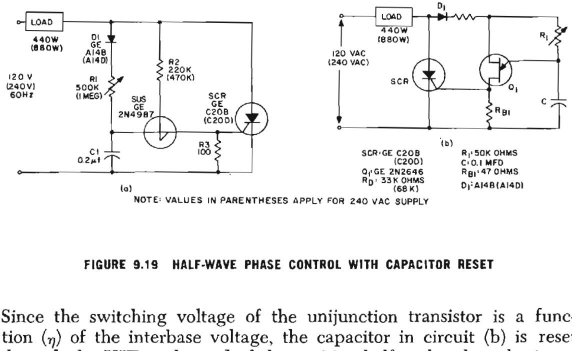
If the switching voltage is not reached during one positive half-cycle, the trigger device does not switch and a high residual voltage is left on the capacitor. The result, as shown in Figure 9.18(b) is "cycle-skipping" as the capacitor continues to charge each positive half-cycle until the trigger device switches. If the range of R_1 can be limited so that triggering always occurs each half-cycle under worst-case tolerance conditions of minimum E_p, minimum C, maximum V_S, minimum I_S, and minimum V_O, this cycle-skipping can be avoided. On the other hand, with the opposite tolerance conditions, the latest possible triggering angle may produce an unacceptable minimum power in the load.

The ultimate solution to cycle-skipping is to automatically reset the capacitor to a known voltage, V_O, a the end of each half-cycle even though V_S was never reached. One way of doing this is to substitute resistor R_2 in the place of diode D_2 in Figure 9.17. This causes the capacitor voltage to reverse on the negative half-cycle, yielding a nega-

tive value of V_O at the start of the positive half-cycle. If the triggering device does not conduct during the negative excursion of V_C, then V_O will be predictable for any given value of R_1. This connection provides one cycle for the residual voltage on C to decay, and eliminates cycle skipping. If the triggering device conducts when V_C is negative, a second diode, D_2, may be used to clamp V_C to approximately -1 volt during the negative half-cycle.

If a bilateral trigger is used, such as the SBS or a Diac, the diode D_2 is not required (provided R_2 adequately limits the negative current) but V_O, at the beginning of the positive half-cycle, will depend on the number of oscillations occurring during the negative half-cycle, hence upon setting of R_1. Changing R_1 will make an integral change in the number of negative oscillations, hence will make step changes in V_O. This action results in step changes in triggering angle.

Automatic reset of capacitor voltage is achieved in the circuits of Figure 9.19 by forcing the triggering device to switch at the end of the positive half-cycle. In circuit (a), resistor R_2 provides a negative current out of the gate of the SUS (see Chapter 4) when the line voltage goes negative, thus causing the SUS to switch and discharge the capacitor.



NOTE: VALUES IN PARENTHESES APPLY FOR 240 VAC SUPPLY

FIGURE 9.19 HALF-WAVE PHASE CONTROL WITH CAPACITOR RESET

Since the switching voltage of the unijunction transistor is a function (η) of the interbase voltage, the capacitor in circuit (b) is reset through the UJT at the end of the positive half-cycle when the interbase voltage dips toward zero.

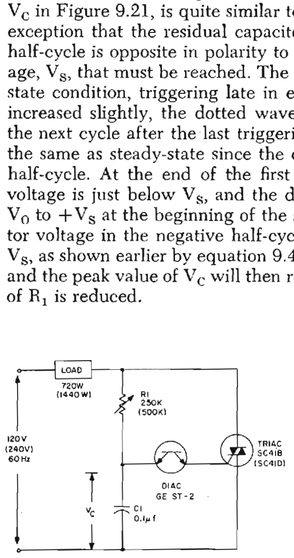
In the preceding examples, the supply voltage for the triggering circuit collapses when the SCR turns on. This connection avoids multiple oscillations and permits decreasing R_1 to zero without damage to the control circuit. If the triggering circuit were connected directly to the supply voltage instead of to the SCR anode, a fixed resistor, approximately 5000 ohms, in series with R_1 would be required to limit current.

Since this latter connection changes the control circuit from a two-terminal to a three-terminal circuit, wiring considerations in certain applications may prohibit its use.

9.4.2 Full-Wave Phase Control

Either of the half-wave control circuits of Figure 9.19 may be used for full-wave power control by connecting them "inside" the bridge rectifier circuit shown in Figure 9.1(e). The UJT circuit of Figure 9.19(b) requires no modification for this use, but the SUS circuit (a) requires changing R_2 to 22 K ohms, adding another 22 K ohms between gate of SUS and cathode of SCR, and deleting diode D_1. These revisions are needed to obtain the reset action of the SUS.

The most elementary form of full-wave phase control is the simple diac/triac circuit of Figure 9.20. The waveform of capacitor voltage, V_C in Figure 9.21, is quite similar to the half-wave case with the major exception that the residual capacitor voltage, V_O, at the start of each half-cycle is opposite in polarity to the next succeeding switching voltage, V_S, that must be reached. The waveform shown for V_C is a steady-state condition, triggering late in each half-cycle. If the resistor R_1 is increased slightly, the dotted waveform, V_C', shows what happens in the next cycle after the last triggering. At the start of this cycle, V_O is the same as steady-state since the diac had switched in the preceding half-cycle. At the end of the first half-cycle, however, the capacitor voltage is just below V_S, and the diac remains dormant. This changes V_O to $+V_S$ at the beginning of the second half-cycle. The peak capacitor voltage in the negative half-cycle is, therefore, considerably below V_S, as shown earlier by equation 9.4. In all succeeding cycles $V_O = V_{Cp}$ and the peak value of V_C will then remain well below V_S until the value of R_1 is reduced.



NOTE:
VALUES IN PARENTHESES ARE FOR 240VAC SUPPLY.

FIGURE 9.20 BASIC DIAC-TRIAC FULL-WAVE PHASE CONTROL

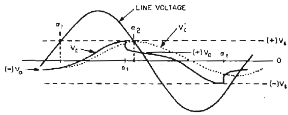


FIGURE 9.21 WAVEFORMS FOR FIGURE 9.20

Once triggering has ceased, reducing R_1 will raise V_C, but when V_S is reached again and the diac switches, V_O is suddenly reduced. This action increases the value of V_C on the next half-cycle, which causes triggering to occur at a much earlier phase angle. As a result, the load current suddenly snaps from zero to some intermediate value, from which point it may be smoothly controlled over the full range from α_1 to α_2.

The "snap-on" effect may be eliminated by using the ST4 asymmetrical silicon bilateral switch (ASBS), as shown in Figure 9.22. It was shown that the snap-on of the diac-triac phase control of Figure 9.20 was due to the fact that the capacitor was charging through a voltage of two times V_S each half cycle, but when the diac triggered the offset caused the capacitor to reach V_S earlier in the cycle. The ASBS has been designed to use this offset to an advantage. Figure 9.23 shows how this is accomplished. (Remember that the ASBS breakover voltage is about 8 volts in one direction and twice that in the other direction.) It can be seen that if R_1 of Figure 9.22 is set so that the ASBS can trigger at point A, the capacitor is essentially uncharged at the zero voltage crossing following point A. If the ASBS were symmetrical, it would indeed switch earlier in the next half cycle (at point C). But since the breakover voltage in that direction is twice that at point A, the capacitor continues to charge until point B. At this point the ASBS triggers and delivers half the capacitor's charge to the triac gate. At this time the capacitor is at the same voltage it was at before the ASBS triggered at all. The result is that the snap-on has been reduced to an almost negligible value with no increase in component count. Since some waveform asymmetry is present in the ASBS phase control circuit, its use may not be practical to drive loads where no significant dc component can be tolerated, e.g. fluorescent lamps, transformers, primaries, and the like.

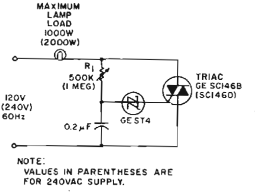


FIGURE 9.22 FULL-WAVE ASBS-TRIAC CONTROL FOR NEGLIGIBLE SNAP-ON

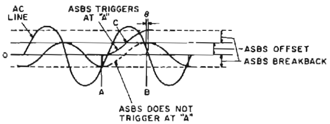


FIGURE 9.23 WAVEFORMS OF ST4 AT SNAP-ON

Figure 9.24 shows another circuit with very little snap-on effect. This circuit uses a second capacitor, C_2, to recharge C_1 after triggering, thus raising V_O to approximately V_S. The maximum, or latest, triggering angle, α_2, with this circuit is not limited to the point where the supply voltage is equal to V_S because the second capacitor will permit greater than 90° phase shift of V_{C1}. If, however, the diac should switch after the 180° point on the supply wave, it could very well trigger the triac at the beginning of the next half-cycle. Since this condition usually needs to be avoided, coupling resistor R_3 should be adjustable to permit compensation for wide-tolerance component values. If desired, R_3 may be set for a minimum power level in the load at maximum setting of R_1.

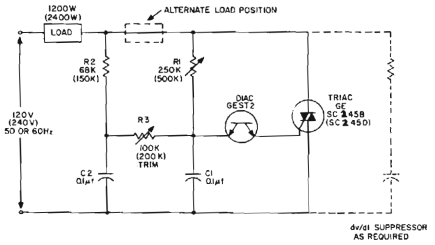


FIGURE 9.24 EXTENDED RANGE FULL-WAVE PHASE CONTROL CIRCUIT

9.5 HIGHER "GAIN" TRIGGER CIRCUITS FOR PHASE CONTROL

All of the previous circuits control phase angle of triggering by a resistor. To control over the full range, from minimum to maximum power, with the simple RC timing circuit requires a very large change in the value of R, presenting a low control "gain." For manual control, this is most adequate. For systems which must perform a function, in response to some signal, the simple RC circuits are usually inadequate, although a photoconductor or a thermistor could be used for control but only over very wide range of light or temperature change.

9.5.1 Manual Control

Figure 9.25 shows a conventional, manually-controlled triac circuit with a unijunction transistor. A zener diode clamps the control circuit voltage to a fixed level, as shown in Figure 9.26. Since the peak-point (or triggering) voltage, e_p, of the unijunction transistor emitter is a fixed fraction of the interbase volage, V_{BB}, as indicated by the dashed curve, the capacitor will charge on an exponential curve toward V_{BB} until its voltage reaches e_p. Assuming, for convenience, that e_p is 0.63 V_{BB}, triggering will occur at one time-constant. Therefore, to cover the range from 0.3 to 8.0 milliseconds, the product R_2C must change by the same amount. Since C is fixed, R_2 must then be varied over a 27:1 range. Not only is this a very large range, but the transfer characteristic from R_2 to average load voltage, V_L, is quite non-linear, as shown in Figure 9.27. These characteristics are usually satisfactory, however, for manual control.

Replacing the manually controlled resistor with a p-n-p transistor, shown in Figure 9.28(a), and applying a DC signal between emitter and base results in a higher current-gain but the range of base current must again be 27:1. The transfer characteristic, Figure 9.28(b), also remains non-linear.

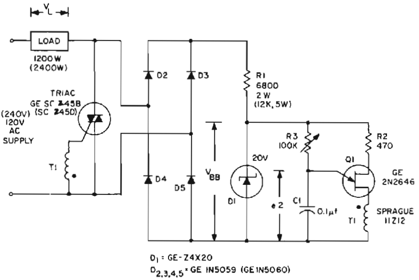


FIGURE 9.25 CONVENTIONAL PHASE-CONTROL CIRCUIT

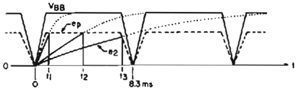


FIGURE 9.26 UNINJUNCTION TRANSISTOR WAVEFORMS

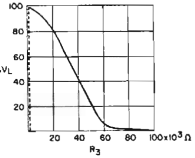


FIGURE 9.27 TRANSFER CHARACTERISTIC OF CONVENTIONAL CIRCUIT (FIGURE 9.25)

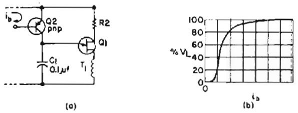


FIGURE 9.28 SERIES TRANSISTOR CONTROLLED RAMP

Control gain can be made very high by the use of a low resistance potentiometer, connected as shown in Figure 9.29(a). Since the exponential charging of C is very fast, and limited by the voltage-division of the pot, the transfer characteristic is again non-linear, as shown in Figure 9.29(b). If the zener clamp has any significant zener impedance, the clamped voltage will not be flat, but will have a slight peak at 90 degrees. This curvature can produce an abrupt discontinuity, or "snap," in the transfer characteristic as indicated by the dashed curve of Figure 9.29(b).

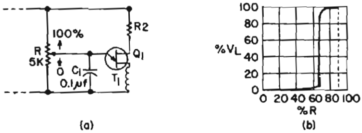


FIGURE 9.29 RESISTANCE CONTROLLED PEDESTAL

The use of an n-p-n transistor, Figure 9.30(a), will provide a high current-gain, but non-linearity and possible snap are still present, as indicated in Figure 9.30(b).

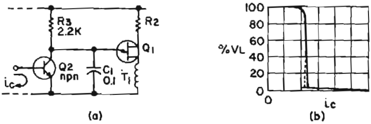


FIGURE 9.30 SHUNT TRANSISTOR CONTROLLED PEDESTAL

9.5.2 Ramp-and-Pedestal Control

If the circuits of Figure 9.25 and 9.29(a) are combined with diode coupling, as in Figure 9.31(a), the exponential ramp function can be caused to start from a higher voltage pedestal, as determined by the potentiometer. Transfer characteristic Curve 1 of Figure 9.31(b) is obtained when R_2 is set for a time-constant of 8 milliseconds. Higher

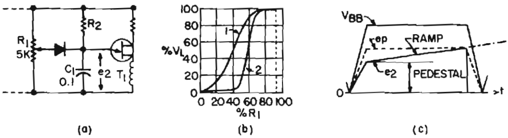


FIGURE 9.31 RESISTANCE CONTROLLED PEDESTAL WITH LINEAR RAMP

control gain is obtained (Curve 2) by making the R_2C_1 time-constant about 25 milliseconds. The voltage wave-shape observed across C_1 is

a nearly-linear ramp sitting on a variable-height pedestal, as in Figure 9.31(c). Small changes in pedestal height produce large changes in phase-angle of triggering. The linear relationship between height and phase-angle results, however, in a non-linear transfer function because of the shape of the sine-wave supply.

Both high gain and linearity are obtained by charging C_1 from the unclamped sinusoidal waveform, as in Figure 9.32(a). This adds a cosine wave to the linear ramp to compensate for the sinusoidal supply waveform, resulting in the linear transfer characteristics shown in Figure 9.32(b). System gain can be adjusted over a wide range by changing the magnitude of charging resistor, R_2, as indicated in Figure 9.32(c). By selecting a ramp amplitude of one volt, for example, and assuming a zener diode of 20 volts, then a change in potentiometer setting of only 5 percent results in the linear, full-range change in output.

The values shown in Figure 9.32(a) are typical for a 60 Hz circuit. The potentiometer resistance must be low enough to charge capacitor C_1 rapidly, in order to be able to trigger early in the cycle. This is the limiting factor on control impedance level. The logarithmic characteristic of diodes limits the control gain that can be achieved with a reasonably linear transfer characteristic. At a one-volt ramp amplitude, diode non-linearity is not pronounced, but a 0.1 volt ramp voltage, the

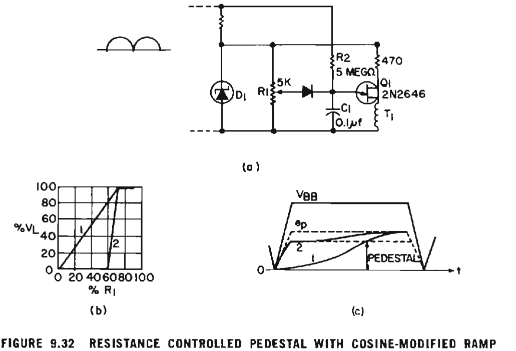


FIGURE 9.32 RESISTANCE CONTROLLED PEDESTAL WITH COSINE-MODIFIED RAMP

capacitor is charged primarily by diode current, thus obliterating the cosine-modified ramp. The sharper knee of a zener diode may be used to obtain higher gains, at the expense of requiring a higher voltage across the potentiometer. The third limiting factor is the peak-point current of the unijunction transistor. This current must be supplied entirely by R_2 and should be no higher than one-tenth the charging current on C_1, at the end of the half-cycle, in order to avoid distortion of the waveform. The 2N2647 unijunction transistor used in the example has a maximum peak-point current of two microamperes. For cases where a lower peak point current is required, the General Electric

D13T2 (2N6028), Programmable Unijunction Transistor is available with a peak point current as low as 150 nanoamperes. The fourth limitation is the zener impedance of diode D_1. This impedance must be very low in order to keep the peak-point voltage (triggering level) constant during the half-cycle. If this voltage changes 0.1 volt, then the ramp voltage should be on the order of 1 volt. The temperature effects on the unijunction transistor, and other components, must also be taken into consideration when attempting to work at very low ramp voltages.

In Figure 9.33(a), manual control is replaced by a bridge circuit for feedback control. Zener diode D_2 has a slightly lower zener-voltage than D_1 in order to hold the top of the clamped waveform more nearly flat. Resistors R_1 and R_2 form the voltage divider which determines pedestal height. Variation in either of these resistors can therefore provide the control function, although R_2 is generally used as the variable. Figures 9.33(b) and (c) show the use of a thermistor for temperature regulation and a photoconductor for light control, in either open-loop or closed-loop systems.

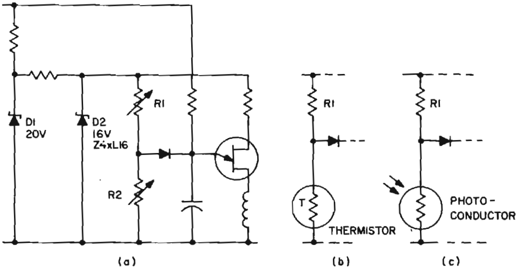


FIGURE 9.33 OHMIC-TRANSDUCER PEDESTAL CONTROL

To obtain a higher input impedance, an n-p-n transistor may be used as an emitter-follower, as shown in Figure 9.34(a). If the transistor has a current gain of 100, the values of R_1 and R_2 can be increased from 3000 ohms to 300 K ohms, thus greatly reducing power dissipation in the sensing element. This is particularly important when R_1 or R_2 is a thermistor. Resistor R_3 is required in the collector circuit of the transistor in order to limit charging current available to the UJT capacitor and thus prevent premature triggering of the UJT.

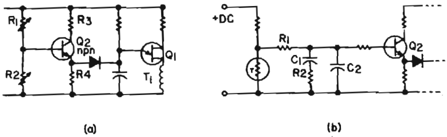


FIGURE 9.34 TRANSISTOR EMITTER-FOLLOWER CONTROL FOR AC OR DC INPUT

In many feedback-control systems, high gain and phase-shifts often produce instability, ranging from excessive overshoot to large oscillations, or hunting. The transistor permits use of a DC sensing circuit followed by an appropriate RC "notch-network" (R_1 C_1, R_2 C_2) to produce the required degree of damping. Since the cosine-modified ramp results in a uniform, linear response, system gain is constant and proper damping is much easier to obtain than in the case of the linear ramp where gain changes with phase-angle. System gain is controlled by the ramp charging resistor (R_2 of Figure 9.32), which can be made a secondary variable through the use of a thermistor or a photoconductor. To avoid excessive loading on the DC sensing circuit, a resistor is required in series with the base of the transistor. Upper and lower control limits may be obtained by the use of diode clamps.

The capability of working from a DC control signal permits a soft-start and soft-stop circuit, shown in Figure 9.35(a). This circuit features individually adjustable rates of start and stop, good linearity, upper and lower limit clamps, and manual or resistive master phase control by means of the top clamping level. For a typical UJT peak-point of 2/3 the interbase voltage, the ramp amplitude may be set at 1/3 interbase voltage and the pedestal clamped at 1/3 and 2/3 this voltage. The resulting performance characteristic is shown in Figure 9.35(b) and (c) for this condition, with the switch turned ON at t_1 and OFF at t_3.

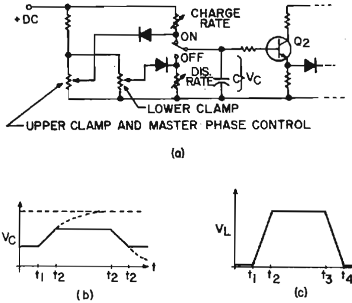


FIGURE 9.35 SOFT START AND STOP CONTROL

Remote control from an AC signal, such as an audio-frequency from a tape recorder or from a tachometer, or an RF carrier alone or with audio modulation, is shown in Figure 9.36. The offset voltage characteristic of a high-gain system provides immunity to noise and effectively decreases the band-width of the input resonant circuit. If offset is not desired, but high-gain is required, the input circuit may be biased, by the dotted resistors R_4 and R_5, to a voltage just below offset. The use of a standard ratio-detector will permit control by an FM signal directly.

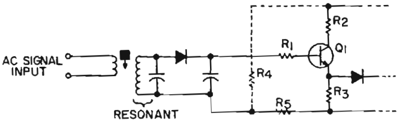


FIGURE 9.36 FREQUENCY-SELECTIVE AC AMPLITUDE CONTROL CIRCUIT

Alternate transistor connections are shown in Figure 9.37, providing a wide variety of performance characteristics. The emitter-follower circuit is simplified in Figure 9.37(a) for low-gain use. At high control gain (low ramp voltage) the emitter current requirement is very low, and the decrease in beta at such low currents causes excessive non-linearity. Standard common-emitter connections for n-p-n and p-n-p transistors, Figures 9.37(b) and (c), provide lower input impedance and higher voltage gain, but require temperature compensation in high-gain applications. In addition, the n-p-n circuit of Figure 9.37(b) results in a sense inversion which may or may not be desirable. Sense inversion is also obtained in the p-n-p emitter-follower of Figure 9.37(d). The excellent performance characteristics and low cost of the 2N2923 silicon n-p-n transistor, however, make the choice of the n-p-n emitter-follower circuit attractive, particularly since the temperature changes have very little effect on operation of this circuit.

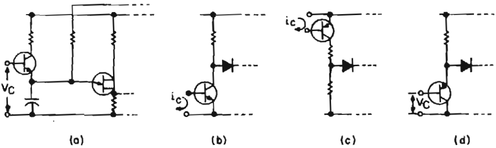


FIGURE 9.37 ALTERNATE TRANSISTOR PEDESTAL CONTROL CIRCUITS

An alternate form of the soft-start circuit is shown in Figure 9.38 using the clamping diode, D_1, to control pedestal height on a linear ramp. Capacitor C_1 may be several hundred microfarads and is charged slowly through R_2. R_1 continues the charging beyond emitter peak-point voltage to completely remove the effect of C_1 and to provide a discharge path when power is removed. The supply for this circuit must be obtained from the line, rather than from voltage across the triac, in order to completely charge C_1.

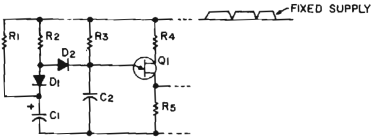


FIGURE 9.38 ALTERNATE SOFT-START CIRCUIT

9.5.3 A Wide Range Line-Voltage Compensation Control

In Figure 9.39, compensation for changes in supply voltage is obtained by R_2 and C_1 which add to the zener diode voltage a DC voltage proportional to supply voltage. This is used to supply interbase voltage for the UJT. Since pedestal height is fixed by the zener diode, reducing supply voltage reduces interbase and peak-point voltages of the UJT, thus causing triggering to occur earlier on the ramp. The size of R_2 is dependent on ramp amplitude, hence upon R_5. The voltage compensation feature does not interfere with use of the pedestal height in any other control form, such as a feedback control system. This system has been found capable of holding RMS output voltage constant within 5% for a 50% change in supply voltage. The bottom end of control is reached when supply voltage drops to desired output voltage.

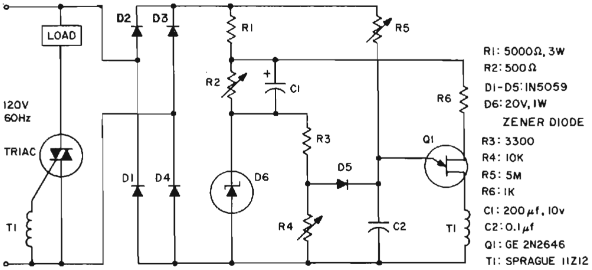


FIGURE 9.39 WIDE RANGE LINE-VOLTAGE COMPENSATION CONTROL

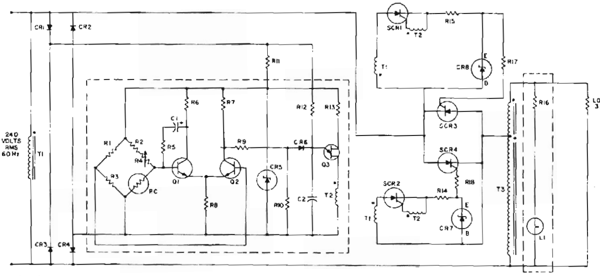
Current feedback control can be obtained by the use of voltage across a shunt resistor, but this requires rectification and filtering when AC is to be controlled since no current flows prior to triggering. In addition, a lamp may be used as the shunt, with a photoconductor sensing lamp output. Response time of the lamp and photoconductor is generally long enough to provide filtering, and the control is on the *square* of current, hence will hold constant RMS value rather than average value. A resistor-thermistor combination will also provide RMS control. A current-transformer may be used to produce a higher output voltage signal on AC with less power loss. If power loss in the shunt is detrimental, a magnetic-flux sensitive element such as a resistance transducer or a Hall-effect element may be used in a suitable coil and core. In these magnetic-flux sensors, the output will be a function of average current.

These circuits are typical of a wide variety, based on the ramp-and-pedestal concept for transfer from voltage, current, or impedance level to phase-angle of triggering for SCR's. Adjustable gain, linearity, selection of high or low input impedance, and operation from a DC input signal are attractive features for use in feedback or open-loop control systems, or in special function systems.

9.5.4 3 kw Phase-Controlled Voltage Regulator

Figure 9.40 is shown here because it exemplifies a method of regulating the RMS value of an unfiltered phase-controlled voltage across a resistive load.

If the voltage across the load was fed directly back to the control circuit and compared to a reference, there would be an undervoltage error when the SCR's are off and an overvoltage when the SCR's were on. Because of this unstable condition, this hypothetical system would not regulate. To obtain regulation (average or RMS regulation), one must have a stable feedback signal as well as a reference. In Figure 9.40 this condition is met by using L_1 and R_{16}, shown within the right hand dotted box. Since the light from a lamp is fairly stable on phase control, this light generated by the load voltage and proportional to it can be used as a feedback signal that is proportional to the RMS voltage of the load. In this example the light is coupled to the photocell, P.C. (the PL5B1 is an integral lamp photocell combination designed for this and similar uses). A change in the output voltage causes a change in light and therefore a change in the photocell resistance. This change in photocell resistance unbalances the resistor bridge. The bridge unbalance then changes the pedestal level of the ramp and pedestal phase control through use of the differential amplifier consisting of Q_1 and Q_2.



CR1 THRU CR4 - GE A14D
CR5 - GEZ4XL22
CR6 - GE A14F
CR7, CR8 - GE 1BL1423
C1 - 10μfd, 25 VDC GE 62F204
μfd MINIATURE TUBULAR WET SLUG CAP
C2 - 0.22μfd, 50 VDC
μfd ±10% GE 75F3R5-244A
Q1,Q2 - GE 2N2925

Q3 - GE 2N2646
SCR1, SCR2 - GE C6U or C106Y
SCR3, SCR4 - GE C135E or C35E
T1 - 220 V RMS PRIMARY
12 V RMS SECONDARY
100 MA RMS RATED
SECONDARY CURRENT
T2 - PULSE TRANSFORMER 1:1
ALADDIN PART NO 90-2398

T3 - TURNS RATIO 1:1.82, 4 KVA
R1 - 22 KΩ
R2 - 2.2 KΩ
R3 - 18 KΩ
R4 - 10 KΩ MULTI-TURN TRIM POT
R5 - 10 KΩ
R6 - 2.2 KΩ
R7 - 2.2 KΩ
R8 - 22 KΩ

R9 - 56 KΩ
R10 - 47 KΩ
R11 - 8.2 KΩ, 10 WATT
R12 - 1.5 MEG Ω
R13 - 1 KΩ
R14, R15 - 22Ω 2W
R16 - 9K ± 5%, 14 WATTS
R17 - 33Ω, 2W
R18 - 33Ω, 2W

L1 - INCANDESCENT LAMP OF GE PL5B1 (LAMP-PHOTOCELL) INTEGRAL HERMETICALLY SEALED UNIT
PC - CADMIUM SULFIDE PHOTOCELL OF GE PL5B1 (LAMP-PHOTOCELL) INTEGRAL HERMETICALLY SEALED UNIT
ALL RESISTORS ± 10% AND 1/2 WATT EXCEPT WHERE INDICATED

FIGURE 9.40 3 KW PHASE-CONTROLLED VOLTAGE REGULATOR

The system also has other important features which should be mentioned. For example, by placing a low resistance in series with the load and in parallel with the feedback lamp L_1, as shown in Figure 9.41, a current regulator is formed. In this circuit, the current through the load is maintained at a constant value.

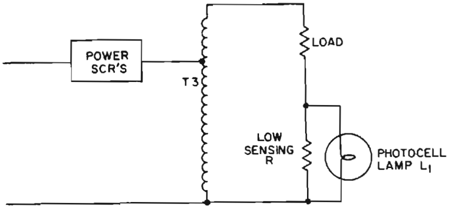


FIGURE 9.41 CIRCUIT CHANGES FOR CURRENT REGULATOR FOR FIGURE 9.40

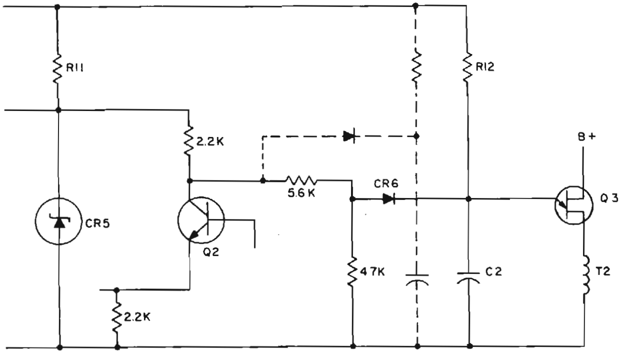


FIGURE 9.42 SOFT-START CIRCUITORY FOR FIGURE 9.40

An additional feature is that the 3 kw load could be a lamp. This would eliminate the need for the feedback lamp L_1. In this case the photocell could monitor, and the system would regulate, the light output of the load. If this were done, the soft-start circuit of Figure 9.41 might be necessary.

Note also C_1 and R_5 in Figure 9.40. These components constitute a "notch" network necessary for stabilization.

Figure 9.42 shows the regulation obtained by the voltage regulator with a 3 kw resistive load for a regulated true RMS load voltage of 300 volts and a nominal input line voltage of 220 volts RMS, 50 or 60 Hz.

Input Line Voltage	True RMS Load Voltage	Load Voltage Change	Response Time
220 V RMS (Nom)	300 (Nom)	——	Less Than 100 msec. for step change in input
190 V RMS	Approx. 299.0	$<$ (0.33%)	
250 V RMS	Approx. 299.0	$<$ (0.33%)	

FIGURE 9.43 TABLE OF REGULATION FOR CIRCUIT OF FIGURE 9.40

9.5.5 860 Watt Limited-Range Low Cost Precision Light Control

The system of Figure 9.44 is designed to regulate an 860 watt lamp load from half to full power. This is achieved by the controlled-half-plus-fixed-half-wave phase control method. Half power applied to an incandescent lamp results in 30% of the full light output. Consequently the circuit is designed to control the light output of the lamp from 30% to 100% of maximum.

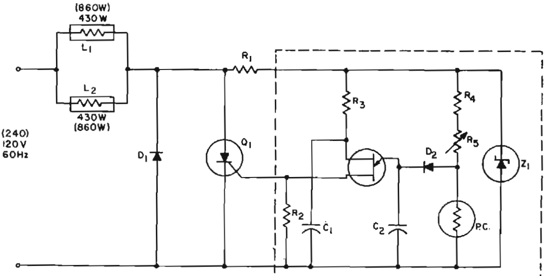
The operation of the closed loop is straightforward with the major features being the load L_1 and L_2, the error signal, photo cell, P.C., the feedback element, Q_2 the error detector, and R_5 the reference.

The method of obtaining the controlled-half-plus-fixed-half-wave is easily seen by realizing that D_1 and Q_1 are in inverse parallel and in series with the load. Also note that Q_1 will turn on during the positive half-cycle at a time dictated by the feedback elements, reference, and error detector located in the dotted block. Consequently, the positive half-cycle is controllable. The function of the dotted block is identical to the ramp and pedestal control of Figure 9.31. Now note that D_1 will conduct during the entire period of every negative half-cycle. Therefore, the negative half-cycle is continually applied to the load. This configuration results in a controllable positive and fixed negative half-cycle applied to the load. It is interesting to note that when D_1 conducts during the negative half-cycle it resets the unijunction firing circuit.

Again temperature and voltage stability of the dotted block is achieved by Z_1, common voltage references, and the stability of the unijunction.

This method of phase-control results in an unsymmetrical wave with a resulting DC component. Therefore, this waveform is not suitable for transformer-fed loads.

The system will regulate the light level to within $\pm 1\%$ for a $\pm 10\%$ change in amplitude of the supply voltage.



R_1 - 6.8KΩ, 2W (15K, 5W)
R_2 - 47Ω
R_3 - 1KΩ
R_4 - 680Ω
R_5 - 1KΩ, 1/2W POT
P.C. - GE A35

Q_1 - GE C122B (C122D)
Q_2 - GE 2N2646
D_1 - GE A41B (A41D)
D_2 - GE A14F
Z_1 - GE Z4XL16
L_1, L_2 - 430W INCANDESCENT LAMP

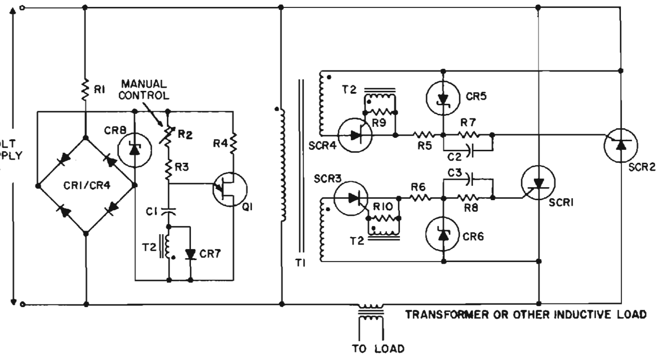
C_1 - .03μfd, 25V
C_2 - .01μfd, 25V
NOTE: ALL RESISTANCES 1/2W, 10% UNLESS OTHERWISE NOTED.
VALUES IN PARANTHESES FOR 240V

FIGURE 9.44 860W, LIMITED RANGE, LOW-COST PRECISION LIGHT CONTROL

9.6 TRIGGER CIRCUIT FOR INDUCTIVE AC LOADS

Inductive AC loads present two basic requirements of the trigger circuits in order to provide symmetry and proper control: a) synchronization must be obtained from the supply voltage rather than SCR voltage; b) the trigger signal must be continuous during most of the desired conduction period. Figure 9.45 shows a trigger circuit specifically designed to meet these requirements.

Unijunction transistor Q_1 is connected across the AC supply line by means of the bridge rectifier, CR_1 through CR_4, thus permitting Q_1 to trigger on both halves of the AC cycle.



R1 - 3.3K, 5 WATT
R2 - 250K, 2 WATT
R3 - 3.3K, 1 WATT
R4 - 330, 1/2 WATT
R5, R6 - 22Ω, 2 WATT
R7, R8 - 33Ω, 2 WATT
R9, R10 - 47Ω, 1/2 WATT
C1, C2, C3 - 0.1 MFD
Q1 - GE 2N2646
SCR1, SCR2 — CONTROLLED RECTIFIERS, AS REQUIRED
SCR3, SCR4 - GE C106F1 OR C103Y

CR1 TO CR4 - GE 1N5059
CR5, CR6 - GE 1N1765
CR7 - GE A14F
CR8 - GE 1N1776
T1 - ISOLATION TRANSFORMER 120/12.6/12.6 VAC; PRIMARY VOLTAGE DEPENDS ON LINE VOLTAGE (UTC FT-10 FOR 120V.)
T2 - PULSE TRANSFORMER PE 2229, UTC H51 OR SPRAGUE 11Z13 EQUIVALENT

FIGURE 9.45 TRIGGER CIRCUIT FOR PHASE CONTROLLED SCR's FEEDING INDUCTIVE LOAD

The time constant of potentiometer R_2 in conjunction with capacitor C_1 determines the delay angle α at which the unijunction transistor delivers its first pulse to the primary of pulse transformer T_2 during each half-cycle. These pulses are coupled directly to the gates of SCR_3 and SCR_4. Whichever of these SCR's has positive anode voltage during that specific half-cycle triggers and delivers voltage to its respective main SCR, firing it in turn. The low voltage AC supply for the "pilot" SCR's (SCR_3 and SCR_4) is derived from a "filament" type transformer T_1. Zener diodes CR_5 and CR_6, in conjunction with resistors R_5 and R_6, clip the AC gate voltage to prevent excessive power dissipation in the gates

of the main SCR's. The RC networks (R_7–C_2 and R_8–C_3) also limit gate dissipation in the main SCR's while delivering a momentarily higher gate pulse at the beginning of the conduction period to accelerate the switching action in the main SCR's.

If electrical isolation of a DC control signal from the AC voltage is required, the entire unijunction trigger circuit with its bridge rectifier and associated components can be connected to an additional secondary winding (approximately 110 volts) on transformer T_1. Total loading of this particular part of the circuit is less than 30 milliamperes. Of course, low level phase control signals for SCR_3 and SCR_4 can be secured from other circuits than the specific one shown, but this is incidental to the main objectives: driving SCR_1 and SCR_2 from a square wave source synchronized to the AC line.

Figure 9.46 is a smaller and lower-cost version of the inductive load phase control. The bridge rectifier D_1-D_4 supplies power to the UJT trigger circuit and supplies holding current to the SCR. If triggering should occur prior to turn-off of the triac, the SCR will be turned on and held by current through R_1. When the triac turns-off at a current zero, triac gate current will flow, depending on polarity, through D_5 or D_6, the SCR, and D_4 or D_2, thus re-triggering the triac. At the expense of higher voltage diodes and SCR, this circuit eliminates all transformers with their attendant cost, size and weight.

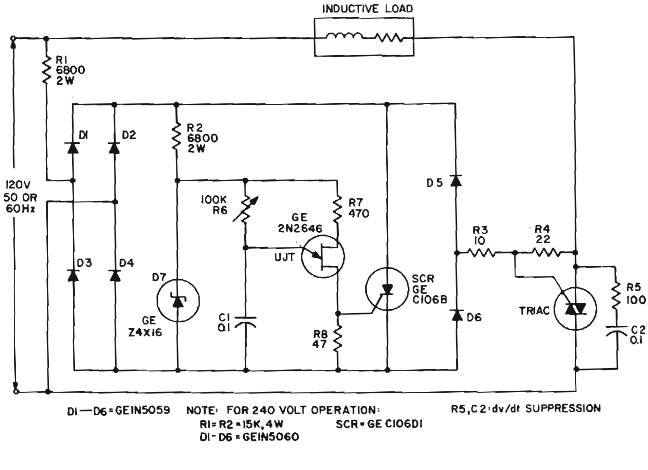


FIGURE 9.46 FULL-WAVE PHASE CONTROL FOR INDUCTIVE LOADS

For higher power-factor inductive loads, and where a small dissymmetry is permissible, the two-capacitor diac/triac circuit of Figure 9.24 may be used, with the load connected in the alternate position shown in that circuit. When R_1 is small, calling for maximum power, the trigger circuit supply is essentially the voltage across the triac, hence cannot attempt to trigger before commutation. When R_1 is large, the trigger circuit is largely powered from the supply voltage, thus providing good symmetry and very little DC component of load current.

9.7 PHASE CONTROL WITH INTEGRATED CIRCUITS

Up to this point the trigger circuits described have been fairly simple and straightforward, but it can be seen that the component count can get rather high. To achieve high performance the component tolerancy can cause the design to become cumbersome and expensive. To simplify design, while maintaining high performance, General Electric has designed and marketed a unique monolithic integrated circuit, the PA436 integrated phase control trigger circuit.

9.7.1 The PA436 Monolithic Integrated Phase-Control Trigger Circuit

The PA436 is a high-gain trigger circuit for phase control of triacs, or SCR's. It is specifically intended for the speed control of AC induction motors, but can also be used on purely resistive loads such as incandescent lamps. This circuit accepts a thermistor signal for temperature control of fans and blowers, or a DC tachometer signal for feedback speed regulation. Adjustable gain, zener-regulated voltage, ambient temperature compensation, and inductive load logic are primary attributes of this integrated trigger circuit.

The PA436 converts an analog input signal to a phase-controlled pulse for triggering thyristors. The signal is compared with a reference and the phase-angle of triggering is obtained by use of the ramp-and-pedestal technique described earlier in this chapter.

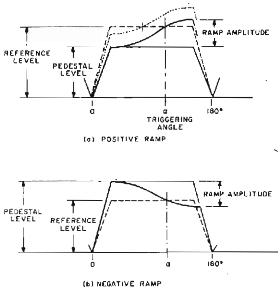


FIGURE 9.47 RAMP AND PEDESTAL WAVEFORM

Figure 9.47(a) shows the typical ramp-and-pedestal waveform, with positive cosine ramp, as is used in unijunction transistor phase control circuits. The PA436 operates with a negative cosine ramp, as shown in Figure 9.47(b), but with a positive pedestal and reference. A positive input signal establishes the pedestal level and a triggering pulse is generated when the ramp crosses the reference level. A *decrease* in signal produces a lower pedestal level and therefore, an earlier triggering pulse, hence an *increase* in load voltage. The "gain" of this type of control can be expressed in terms of change in load voltage per unit change in signal voltage. For convenience in measurement, using a rectifier type voltmeter, the load voltage is usually expressed as the full-wave-rectified average value. Alternate expressions of "gain" use either the absolute or relative change in signal required to shift the triggering angle from 150° to 30°, which represents changing power in a resistive load from 3% to 97% of full power. The absolute change in signal level required for this triggering range is the same as the ramp amplitude. The relative change in signal is the ratio of ramp amplitude to reference level, usually expressed as a percentage. Since the full range of power is covered by a smaller range of triggering angles with inductive loads, the load power factor can change gain upwards by as much as twice.

Inductive loads, such as induction motors, require a certain logic in the triggering circuit in order to achieve reasonable symmetry between the positive and negative portions of the alternating voltage. The PA436 provides this inductive-load logic by taking the time reference for the ramp-and-pedestal waveform from the zero crossing of line voltage and by a lock-out gate that prevents trigger pulses from occurring before the zero crossing of line current.

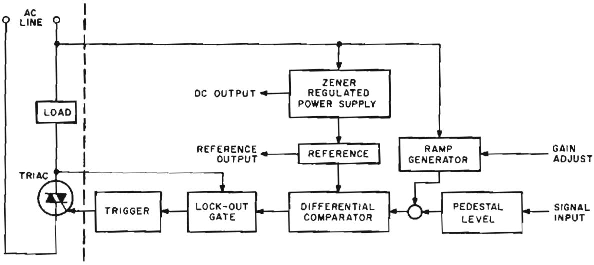


FIGURE 9.48 BLOCK DIAGRAM, PA436 PHASE CONTROL IC

The block diagram of Figure 9.48 shows the functions performed within the PA436. The DC input signal establishes a pedestal level to which is added a negative cosine ramp that is derived from the supply voltage and is externally adjustable. The resulting waveform is com-

pared with a zener regulated reference wave in the differential comparator which produces an output signal when the ramp is below the reference level. The lock-out gate blocks this signal from the trigger pulse generator until after line current has passed through zero and voltage has appeared across the triac.

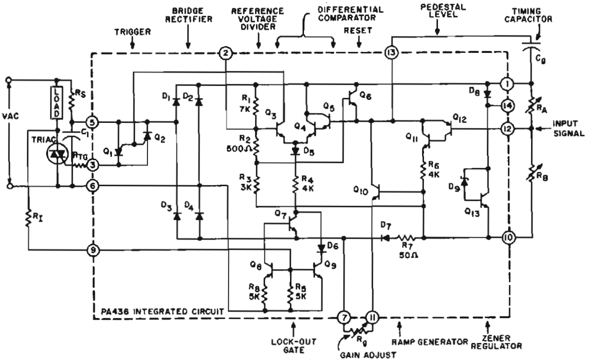


FIGURE 9.49 CIRCUIT DIAGRAM, PA436 PHASE CONTROL IC

The internal circuit of the PA436 is shown in Figure 9.49, along with a typical external circuit. Operating supply voltage for the circuit is obtained from the AC line through current-limiting resistor R_S and the bridge rectifier, and is clamped by the zener diode D_9 through transistor Q_{13} and diode D_8. The clamped waveform appearing between terminals 1 and 10 is the supply for the pedestal and reference levels. Note that virtually all circuit current returns through resistor R_7 and diode D_7, and that this current waveshape is a full-wave rectified sinusoid.

A DC signal, such as from external divider R_A and R_B, charges external timing capacitor C_g to the pedestal level through the p-n-p emitter-follower Q_{12}, supplemented by Q_{11}, with current limited by R_6. Capacitor C_g continues charging by a half-sine-wave current through Q_{10} and external emitter resistor R_g, forming the cosine ramp. This current waveshape is obtained by the voltage drop of supply current through R_7, applied to the base of Q_{10}. Amplitude of the ramp charging current is determined by the external emitter feedback resistor R_g, hence this resistor value establishes ramp amplitude. Diode D_7 compensates for the base-emitter voltage of Q_{10}.

The reference voltage level is obtained directly from the zener-clamped supply voltage by divider resistors R_1, R_2 and R_3. Reference voltage is brought out on terminal 2 and can be modified, if necessary, by external resistors to terminals 1 or 10.

The differential amplifier Q_3, Q_4 and Q_5, compares capacitor voltage to the reference voltage. The Darlington connection of Q_4 and Q_5, in addition to presenting a high impedance to the timing capacitor, provides an extra base-emitter voltage offset to compensate for the base-emitter drop of the pedestal emitter-follower Q_{12}. The apparent reference level (i.e. the voltage required at terminal 12 to trigger at the beginning of the ramp) only differs from the voltage at terminal 2 by the relatively small differences in base-emitter voltages of Q_3, Q_4, Q_5, and Q_{12}.

Common mode current of the differential comparator, through D_5 and R_4, is controlled by the lock-out gate D_6, Q_7, Q_8 and Q_9. When load current is flowing through the triac, there is insufficient base drive on either Q_8 or Q_9 to enable conduction of common-mode current, hence the comparator is inhibited from producing an output signal to the trigger. When voltage appears across the triac, current through external resistor R_I enables the lock-out gate and permits normal functioning of the comparator. The value of R_I determines the triac voltage required to enable the comparator.

Trigger pulses are generated by the bilateral switch formed by Q_1 and Q_2 which discharge the external capacitor C_1 into the gate of the triac. Q_1 and Q_2 are triggered by conduction of Q_3, in the comparator, when the ramp voltage drops below the reference level, but only if common mode current can flow through the lock-out gate. Since the trigger pulses alternate with the same polarity as the AC line voltage, they are ideally suited for triggering triacs directly, or pairs of SCR's through a 1:1 pulse transformer.

In order to avoid a carry-over of information from one half-cycle to the next, the timing capacitor must be reset to a fixed level at the end of each half-cycle. This reset function is accomplished by Q_6 which is biased off by dividers R_1, R_2 and R_3 until supply voltage approaches zero. The capacitor voltage then provides a base drive to Q_6, thereby discharging the capacitor to the base-emitter voltage drop.

9.7.2 Circuit Design With the PA436

Selection of external circuit components is based upon the ratings and characteristics of the PA436, as follows:

R_S: Minimum value is peak line voltage divided by supply current peak rating ($I_{5\text{-}6}$). Maximum value must supply sufficient current to obtain zener clamping over desired triggering range, including current to external loading between terminals 1-10 and 14-10.

C_1: Must store sufficient charge to trigger the external thyristor. 0.1 μf will trigger all GE triacs. Peak discharge current must be limited to pulse rating I_3.

R_{TG}: The current limiting resistor (R_{TG}) of 82 ohms is used to limit the peak trigger pulse output current to its maximum rating of 150mA.

R_I: Minimum value is peak line voltage divided by enable current peak *rating*, I_9. Maximum value must supply the maximum *characteristic* enable current over the desired triggering range.

C_g: } R_g: } Select to produce desired gain from peak sinusoidal ramp current specification, I_{13} ramp. Calculate the cosine ramp amplitude by:

$$V_{ramp} = \left(\frac{2\, I_{13}}{\omega C_g}\right) \left(\frac{10{,}000}{R_g}\right) \text{volts}$$

To this cosine ramp amplitude there must be added a linear ramp amplitude which is caused by the comparator darlington base current, $I_{13\ bias}$, where

$$V_{ramp} = \frac{7\, I_{13}}{C} \times 10^{-3}\ \text{volts}$$

Normal range of values for C_g is from 0.1 μF to 0.01 μF, and R_g from 7.5k to 100k ohms.

R_A: } R_B: } Normal range of $(R_A + R_B)$ is 10k to 200k ohms. Lower values can produce excessive loading on the supply. Higher values limit charging current for C_g and cause a peak at the leading edge of the pedestal that reduces control gain at the earlier triggering angles. Current gain of the pedestal emitter follower determines this effect.

DC Control Signal Source: When a self-contained DC source is used, such as a tachometer, it should be well filtered and have an output impedance between 2k and 100k ohms. Where a DC supply voltage is needed to create the control signal, a filter capacitor may be connected between terminals 10 and 14. Loading on this capacitor should be 10k ohms or higher to minimize charging current. When such a filter capacitor is used, care should be taken to ensure that triggering cannot occur before the capacitor is charged to zener voltage each half-cycle. This can generally be handled by proper selection of enable current through R_1 and/or by adding a small capacitance between terminals 9 and 6 for a slight phase shift of enable current.

RF Interference Filters: See Chapter 16.

dv/dt Suppression Circuits: See Chapter 5.

9.7.3 PA436 in High Power Circuits

When using the PA436 in higher power circuits it is usually necessary to provide a means of gate coupling and gate pulse amplification. The circuits of Figure 9.50 show five different methods.

For circuits using an SCR-diode pair, Circuit A is the simplest. The circuit uses SCR_2 as a pilot SCR to deliver adequate gate current to SCR_1, the main load current SCR. The capacitor C_1 provides a hard fire gate signal to allow the circuit to be used for circuits with high load current di/dt's.

The circuits B, C and D are for inverse parallel SCR's. Since the PA436 was designed specifically to trigger triacs a triac can in some cases be used as the pilot SCR. Circuit B shows this type of connection. The two A14F diodes prevent reverse gate voltage from appearing on the reverse biased SCR. Circuit C operates in much the same way as B

only in C the triac has been replaced by a transformer with the triac in its secondary. In this manner the triac circuit can be used regardless of how high the line voltage becomes.

Circuits D and E use SCR's as the pilot and coupling devices. Circuit D uses a single SCR as a remote base transistor on the negative half cycle to provide gate current to SCR_2. Circuit E provides for hard firing of the load carrying SCR's at the expense of two pilot SCR's and a pulse transformer.

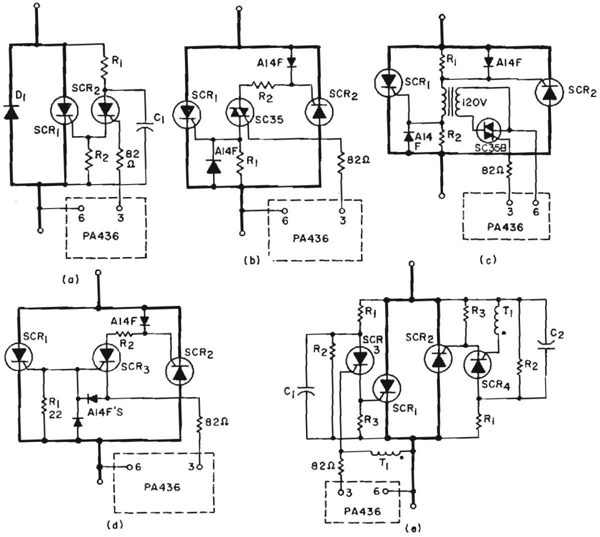


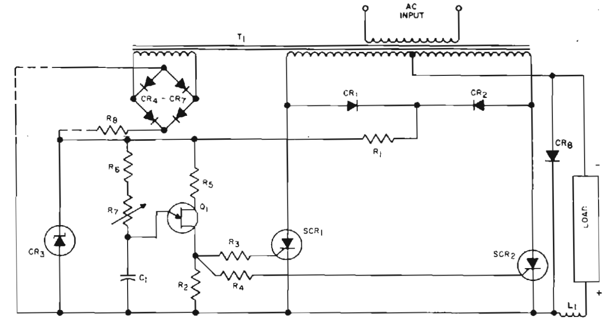
FIGURE 9.50 GATING CIRCUITS FOR HIGHER CURRENT SCR's TRIGGERED BY THE PA436

9.8 TYPICAL PHASE-CONTROLLED CIRCUITS FOR DC LOADS

Figure 9.51 illustrates the use of SCR's in a typical single phase center-tap phase-controlled rectifier. By varying R_7, the DC voltage across the load can be steplessly adjusted from its maximum value down to zero. As in the AC phase-controlled switch, a single UJT (Q_1) is used to develop a gate signal to fire both SCR's on alternate half-cycles. Whichever of the two SCR's has positive anode voltage at the time the gate pulse occurs will fire, thus applying voltage to the load for the remainder of that half-cycle. The firing angle can be adjusted by means of R_7. At 60 Hz, the firing angle of this circuit can be varied from approximately 10° to 180° (fully off).

If the secondary voltage applied to the SCR anodes is less than approximately 100 volts RMS, a separate voltage supply should be used for the UJT control. In Figure 9.51 an additional 117 VAC wind-

ing on T_1 in conjunction with a diode bridge CR_4–CR_7 can be substituted for CR_1, CR_2, and R_1 if the main secondary voltage is low. A more steeply rising square wave of voltage with sufficient amplitude is thereby provided for control purposes. If the load requires filtering, inductance L_1 and free-wheeling diode CR_8 may be added, as shown.



R_1 — 3.3K, 5 WATT IF SEC VOLTAGE OF T_1 IS 117 VOLTS EACH SIDE OF CENTERTAP	R_6 — 2.7K, 1/2 WATT	SCR_1, SCR_2 — AS REQUIRED BY LOAD
R_2 — 47 Ω, 1/2 WATT	R_7 — 50K LINEAR POT	CR_1, CR_2, CR_4, CR_7 — G E IN5060
R_3, R_4 — 22 Ω, 1/2 WATT	R_8 — 3.3K, 5 WATT	CR_3 — IN1776 REGULATING DIODE
R_5 — 390 Ω, 1/2 WATT	C_1 — 0.2 MFD	Q_1 — G E 2N2646
	L_1 — AS REQUIRED FOR FILTERING OPTIONAL	CR_8 — AS REQUIRED BY LOAD CURRENT

FIGURE 9.51 PHASE-CONTROLLED DC POWER SUPPLY

When feedback is required a somewhat more elaborate circuit is required. In order to keep the component count within reasonable limits, the circuit of Figure 9.52 was designed. It uses the PA436 inte-

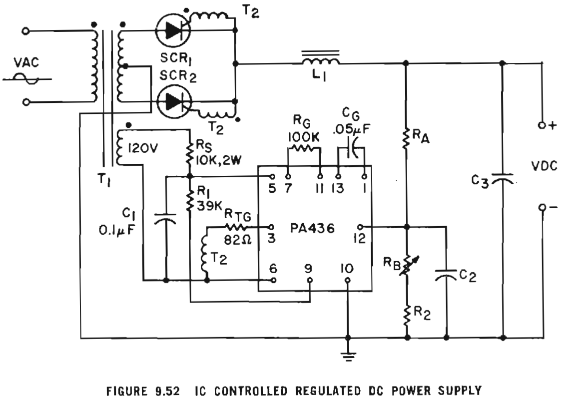


FIGURE 9.52 IC CONTROLLED REGULATED DC POWER SUPPLY

grated circuit phase control which is explained in the previous section, in conjunction with two SCR's. The feedback is obtained from the resistor divider of R_A, R_B, and R_2. When the voltage at pin twelve (12) of the PA436 drops below the set point the phase firing angle is increased to deliver more power to the load. The components can easily be tailored to almost any voltage and current output desired.

9.8.1 A 1.2 KW, 60 V Regulated DC Power Supply

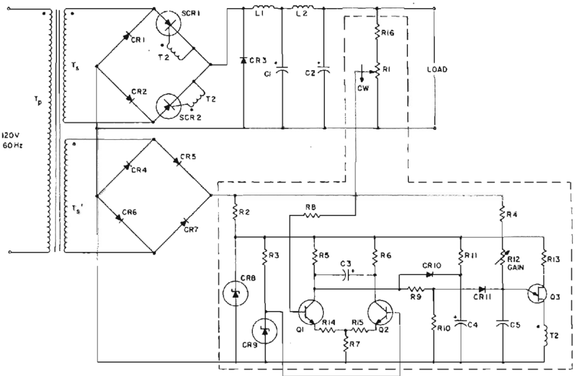
Figure 9.53 shows a regulated DC power supply which utilizes a cosine modified ramp and pedestal control. Unlike the previous circuits, this circuit uses two diodes (CR_1, CR_2) and two SCR's (SCR_1, SCR_2) to form the main current path. This allows the use of a con-center-tapped transformer. By phase controlling the SCR's, control can be maintained from 7 to 21 volts or 21 to 60 volts by changing the turns ratio of T_8; with a maximum load of 20 amperes in each range.

The function of the feedback element (R_1), reference (CR_9), and error detector (Q_3), all located in the dotted block, is to provide regulation by properly phase controlling the SCR's. The basic operation of the dotted block is very similar to Figure 9.33. By comparing a portion of the DC output voltage, as sampled by the wiper of R_1, with the stable reference of CR_9, an error is generated by Q_3. Consequently by adjusting R_1 clockwise, the regulated output will increase until it reaches its maximum value. At maximum output, of course, the system has no regulating ability. The minimum amplitude is fixed by CR_9.

A lower voltage CR_9 could be used which would allow a lower minimum output voltage.

The dotted block incorporates some interesting features. For example, the cosine-modified ramp and pedestal allow the use of the gain pot R_{12}. This should be adjusted for maximum regulation, overshoot, etc. Also note that the combination of CR_{10}, R_{11} and C_4 constitutes a soft-start circuit. This feature protects the supply when starting under heavy loads. In addition, stability of the dotted block is achieved by CR_8 ,CR_9, the differential amplifier of Q_1 and Q_2, common voltage points and the unijunction Q_3.

Figure 9.54 shows the performance of the supply. The response times could be reduced if desired at the expense of increased ripple.



CR1, CR2 - GE A40A
CR3 - GE A28A
CR4, CR5, CR6, CR7 - GE 1N5059
CR8 - GE Z4XL14
CR9 - GE F16H1
CR10, CR11 - GE A14F
R1 - 5KΩ, 1/2W POT
R2 - 2.2KΩ, 7W
R3 - 680Ω
R4 - 470KΩ
R5, R6, R7 - 3.3KΩ
R8 - 10KΩ

R16 - 10KΩ (USE FOR 21-60 VOLT RANGE ONLY)
R14, R15 - 33Ω
R9 - 4.7KΩ
R10 - 22KΩ
R11 - 22KΩ
R12 - 1.0 MEG Ω, 1/2W POT
R13 - 1KΩ
C1 - 1300μfd, 200VDC GE 43F3074CA6
C2 - 23,400μfd, 75WVDC GE 86F1805
C3 - 100μfd, 30 WVDC GE WET SLUG 62F403
C4 - 100μfd, 25 WVDC
C5 - 0.1μfd, 10%

T - 1KVA FOR $\frac{T_p}{T_s} = 4$
2KVA FOR $\frac{T_p}{T_s} = 2$
$\frac{T_p}{T_s'} = 1$, 100 MA T_s - FOR ALL CONDITIONS
T2 - SPRAGUE 11Z13
L1 - 1/2 MILLIHENRY, 20 AMP DC
L2 - 10 MILLIHENRY, 20 AMP DC
Q1, Q2 - GE 2N3391
Q3 - GE 2N2646
SCR1, SCR2 - GE C30A

NOTE: ALL RESISTORS 1/2 WATT, 10% UNLESS OTHERWISE SPECIFIED

FIGURE 9.53 1.2KW, 60V REGULATED DC POWER SUPPLY

Load Voltage volts DC	Ripple - 120 Hz millivolts peak-to-peak	Response Time milliseconds	Load Regulation Percentage	T_1 Ratio
10	40 at 2.5 Amps I_L 70 at 20 Amps I_L	100 - 2.5 to 20 Amps 100 - 20 to 2.5 Amps	2% for 2 to 10 Amps I_L .03% for 10 to 20 Amps I_L	4:1
15	60 at 2.5 Amps I_L 360 at 15 Amps I_L	—	—	4:1
20	40 at 2 Amps I_L 880 at 20 Amps I_L	200 - 2 to 8 Amps I_L 150 - 8 to 2 Amps I_L No Check for V_{Line}	1% for 2 to 8 Amps I_L 2% for 8 to 20 Amps I_L ±1/2% for ±15% Swing in V_{Line} at input to T 10 Amp Load	4:1
25	800 at 20 Amps	—	2% for 2.5 to 10 Amps I_L 1% for 10 to 20 Amps I_L	2:1
40	700 at 20 Amps	200 - 3 to 20 Amp I_L	1/2% for 3 to 20 Amps I_L 1/2% for 3 to 8 Amps I_L	2:1
50	200 at 10 Amps	—	±0.4% for ±15% Swing in V_{Line} at input to T I_L = 10 Amps	2:1
60	500 at 20 Amps 280 at 12 Amps	150 - 2.5 to 12 Amps I_L 75 - 12 to 20 Amps I_L	2% for 2.5 to 12 Amps I_L 1.5% for 12 to 20 Amps I_L	2:1

FIGURE 9.54 PERFORMANCE OF FIGURE 9.53

9.9 POLYPHASE SCR CIRCUITS

The use of controlled rectifiers is by no means limited to single-phase AC circuits. They may be used in polyphase circuits just as conventional two element semiconductor rectifiers. Regardless of the particular circuit configuration the two basic requirements that must be met are the supplying of a trigger turn-on signal at the appropriate time and provision in the circuit external to the controlled rectifier for turn-off.

With regard to turn-off, the reversal of the line voltage across the device in common rectifier circuit configurations will return the controlled rectifier to a forward blocking state; this is often referred to as line commutation. On commutating, the rectifier is subjected to reverse voltage which facilitates the turn-off process. For this reason, common AC rectifier circuits do not impose unusual turn-off requirements on the controlled rectifier as do certain types of inverter or DC chopper circuits in which forward voltage is reapplied to the controlled rectifier immediately following turn-off. However, depending on the amount of phase retard the controlled rectifier and its associated rectifiers may be subjected to full peak reverse blocking voltage immediately after having conducted full rated current. This type of service is conducive to the generation of recovery voltage transients. Particularly, in cases where SCR's are used in series in a leg of such a circuit, steps must be taken to force proper sharing of these transients between all the devices in the leg. This is discussed more fully in Chapter 6.

The question of utilizing controlled rectifiers in polyphase circuits involves providing appropriately timed triggering signals in accordance with the type of circuit used and the degree of phase control required. For example, the circuit of Figure 9.55 shows the popular three phase bridge circuit in which the forward legs are controlled and the back legs consist of uncontrolled conventional two terminal rectifiers. This circuit will give full continuous control from zero to 100% of its DC output when triggering signals capable of being phase shifted over 180 electrical degrees are supplied as shown in Figure 9.56(a).

The triggering circuit discussed in Section 9.9.2 will provide such triggering signals. If triggering signals are supplied as shown in Figure 9.56(b) such that they can be phase-shifted over 120 electrical degrees, the circuit will deliver full control from about 25% to 100% of full output power to the load. A circuit to do this is discussed in Section 9.9.1.

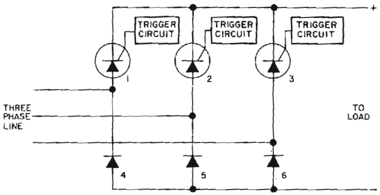


FIGURE 9.55 THREE PHASE BRIDGE CIRCUIT WITH THREE CONTROLLED LEGS

In some special cases it is desirable to control all six elements of the three phase bridge circuit. Regenerative braking of a DC machine where either field or armature reversing is provided is an example of such a case. For this case, triggering signals capable of being phase-shifted over 120 electrical degrees must be supplied as shown in Figure 9.56(c).

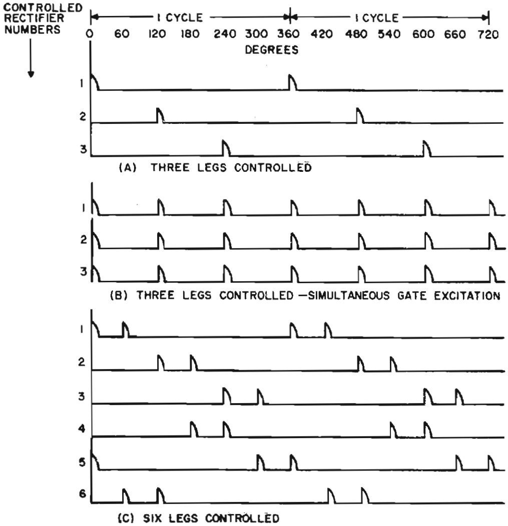
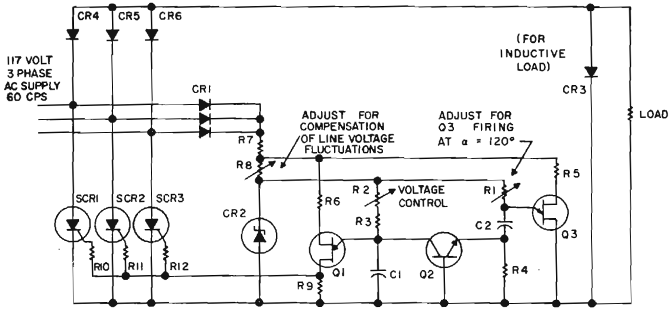


FIGURE 9.56 TRIGGERING PULSES FOR THREE PHASE BRIDGE CIRCUIT

9.9.1 Simple Three Phase Firing Circuit (25% to 100% Control)

This section describes a simple three-transistor SCR firing circuit that provides stepless control of the DC output voltage from a three-phase bridge between 25% and 100% of maximum output voltage, and also full interruption of output voltage. Means are incorporated to provide automatic compensation for line voltage fluctuations and for phase unbalance without closed-loop feedback.

This circuitry is readily applicable wherever stepless control is not required over the full range from zero to 100% of the maximum DC output voltage. Its main features are its simplicity, low cost, compactness, and reliability. Its inherent characteristics provide symmetrical output in all three phases without the need for special matching and adjustment of individual circuits, and the circuit is insensitive to power factor or phase reversal. It lends itself readily to electrical feedback techniques and does not require a separate control voltage supply. No magnetic components are needed.



CR1 — (3) GE 1N5059
CR2 — 20 VOLT, 1 WATT ZENER DIODE, Z4X20B
CR3, CR4, CR5, CR6 — AS REQUIRED FOR LOAD (e.g. A40B)
SCR1, SCR2, SCR3 — AS REQUIRED FOR LOAD (e.g. C35B)
Q1, Q3 — G E 2N2646 Q2 — G E 2N2923
R1 — 10K POT
R2 — 20K POT
R3 — 470 Ω

R4 — 100 Ω
R5, R6 — 390 Ω
R7 — 3.3 K, 2 W
R8 — 500 Ω POT, 2 W
R9 — 100 Ω
R10, R11, R12 — 25 Ω
C1 — 0.5 MFD
C2 — 1.0 MFD

FIGURE 9.57 SIMPLE THREE PHASE FIRING CIRCUIT

Figure 9.57 illustrates the complete firing circuit. CR_1 supplies positive line voltage to the control circuit whenever the anode voltage on an SCR swings positive with respect to the positive DC bus. This voltage is clipped at 20 volts by zener regulator CR_2 and supplies a conventional unijunction transistor relaxation oscillator firing circuit of a type described in detail in Chapter 4. R_2 controls the firing angle of Q_1 by regulating the charging rate to capacitor C_1. The pulse of voltage developed across R_9 as unijunction Q_1 discharges C_1 is coupled simultaneously to the gates of all three controlled rectifiers, SCR_1, SCR_2, and SCR_3, through R_{10}, R_{11}, and R_{12}. Whichever SCR has the most positive anode voltage at the instant of the gate pulse starts conduction at that point.

The circuit composed of transistors Q_2 and Q_3 prevents Q_1 from firing at any delay angle greater than 120°. If triggering pulses are retarded beyond 120°, the output voltage rises abruptly to 100% as the following phase is fired at the beginning of its cycle. Q_3 is an independent unijunction oscillator which initiates its timing cycle at the same instant as Q_1. R_1 is set at a fixed value so that Q_3 fires at an angle slightly less than 120°. Two modes of operation are possible:

1. If Q_1 triggers before retard angle $\delta = 120°$; it fires the SCR whose positive anode voltage is providing the interbase bias for the unijunctions through CR_1. Firing this SCR shorts the control circuit supply voltage. The interbase bias voltage of Q_3 drops to zero, causing Q_3 to fire and discharge C_2 in preparation for the next cycle. This is the mode of operation when Q_1 is

controlling the DC output voltage between 25% and 100% of maximum. In this mode, Q_2 and Q_3 have no effect on the functioning of the bridge.

2. If Q_1 is delayed beyond $\delta = 120°$, Q_3 fires, discharging C_2 through the base-emitter junction of Q_2, saturating this device, and discharging C_1 through Q_2. This alternate mode of discharging C_1 does not impose a pulse on the SCR gates, and the DC output voltage is therefore zero in this mode.

Instead of mechanical manipulation of potentiometer R_2 to control the DC output voltage, electrical signals can be used to control the output by inserting a transistor in series with R_2 in the charging path for C_1, or alternately a transistor in shunt with C_1. Both methods are readily useful in conjunction with feedback systems and are described in Chapter 4, and in Section 9.5.

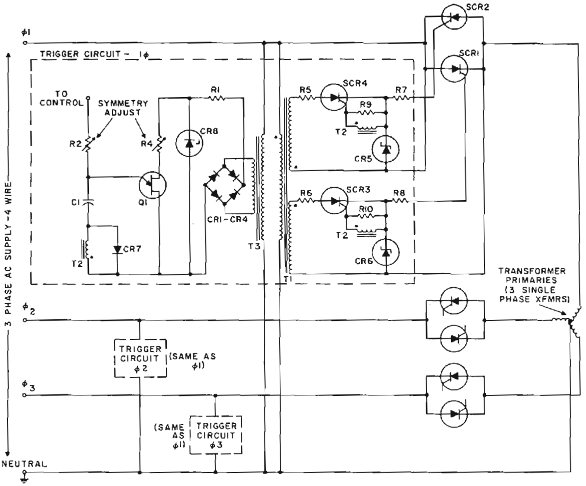
The success of this circuit depends on Q_3 maintaining its firing angle at slightly less than 120°. For this reason, base 2 of unijunction transistor Q_3 is connected through R_5 to a point separated from the clipped and regulated voltage across CR_2 by resistor R_8. This acts to maintain the timing cycle of Q_3 fixed at slightly less than 120° regardless of normal line voltage variations. Without this precaution, a drop in line voltage would make Q_3 fire at a somewhat greater angle than 120° due to the lesser slope on the front of the clipped sine wave voltage being applied to R_1.

R_8 serves another useful purpose. By connecting base 2 of unijunction transistor Q_1 to the top of R_8, a marked degree of regulation of the DC output voltage is provided for AC line voltage fluctuations. If the line voltage rises, the interbase bias voltage and therefore the peak-point emitter voltage on Q_1 rises depending on the setting of R_8. Since the emitter charging circuit through R_2 is conneced to the fixed voltage across regulator CR_2, the firing angle is phased back and the output DC voltage is maintained constant. For a decrease in line voltage, this action advances the firing angle to maintain the output constant. This inherent action is instantaneous and does not depend on a change in the actual output voltage to take corrective action. Where unequal phase voltages exist, this circuit also acts to balance the contribution of the individual phases to the DC output voltage, thus reducing the fundamental frequency ripple content in the DC. Since the compensation provided by R_8 is not constant at all firing angles, R_8 should be adjusted for optimum action near the voltage level at which operation will normally take place.

With a three-phase 117 VAC supply, the circuit in Figure 9.57 can be varied steplessly over DC output voltages from 40 volts to 150 volts DC, a range of 3.75 to 1. It can also be turned off completely. With line voltage variations of ±10%, R_8 can be adjusted to provide essentially constant DC output voltage at both extremes of line voltage. Test data with $R_8 = 350$ ohms, with 10 ohms of load, and with G-E C35B cells as the SCR's showed that for a variation in AC line input voltage from 130 volts to 100 volts the DC output varied from 93 volts to 92 volts.

9.9.2 Full Range Three Phase Control System

Figure 9.58 illustrates a phase-controlled circuit for a four wire AC system feeding three wye-connected transformers. One pair of SCR's is connected in series with each of the lines and the transformer neutral is connected to the system neutral. Trigger circuits similar to the single phase type are connected from line to neutral of each phase. For illustrative purposes, a unijunction transistor is used to trigger the pilot SCR's. So that all three trigger circuits can be controlled simultaneously with a single adjustment or electrical signal, each unijunction circuit is isolated from the power circuit by a transformer T_3. This permits the three unijunction circuits to be electrically inter-connected at any convenient point. Several variations for controlling the three unijunctions from a master signal are shown in Figure 9.59. The most suitable type depends on whether manual or electrical control is desired, also the magnitude and impedance level of the available master control signal.



R1 – 3.3K, 5 WATT
R2 – SEE FIG. 9.69
R4 – 10K, 1 WATT
R5, R6 – 22 Ω, 2 WATT
R7, R8 – 33 Ω, 2 WATT
R9, R10 – 47 Ω, 1/2 WATT

C1 – 0.1 MFD
Q1 – G-E 2N2646
SCR1, SCR2 – AS REQUIRED
SCR3, SCR4 – GEC106F1
CR1 TO CR4 – GE1N5060
CR5, CR6 – G-E 1N1765
CR7 – G-E A14F
CR8 – G-E 1N1776

T1 – ISOLATION TRANSFORMER WITH 12.6 VOLT, 1/4 AMP, SECONDARIES, PRIMARY AS REQUIRED FOR SPECIFIC LINE VOLTAGE

T2 – PULSE TRANSFORMER PE 2229, H51 OR EQUIVALENT

T3 – ISOLATION TRANSFORMER WITH 120 VOLT, 50 MA SECONDARY, PRIMARY AS REQUIRED FOR SPECIFIC LINE VOLTAGE (FOR 120 VOLT PRIMARY, TRIAD N-51X)

FIGURE 9.58 PHASE CONTROL FOR THREE PHASE, FOUR WIRE POWER SYSTEM FEEDING WYE CONNECTED TRANSFORMERS

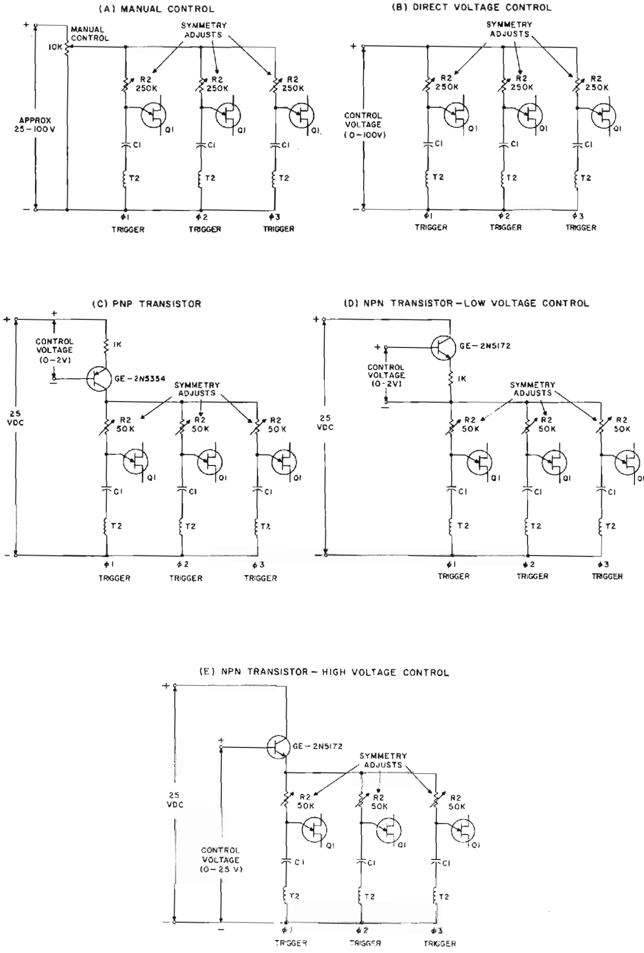


FIGURE 9.59 CONTROL CIRCUITS FOR THREE PHASE CIRCUIT OF FIGURE 9.58

Adjustments are provided in each unijunction circuit for establishing symmetrical firing between the phases. R_4 in each circuit is set so that all three unijunctions trigger at the same emitter voltage (voltage across C_1 and primary of T_2). R_2 is then adjusted for equal tracking of all three phases to a single control signal, such as the manual control setting in Figure 9.59(a).

Proper operation of the circuit of Figure 9.58 requires significant currents to be carried in the neutral connection and care must be taken in designing the power conductors and supply for this purpose. This circuit will not work over the complete voltage range with a delta connected transformer. Neither will it provide smooth control of the load voltage without the neutral connection between the supply and the wye connected transformers. In either of these two cases discontinuities in the load voltage occur as the control signal is varied.

9.9.3 Use of the PA436 Phase Control Integrated Circuit in Three Phase Circuits

Due to the excellent temperature compensation built into the PA436, it is quite suitable for phase controlling three phase circuits. Over a 25°C temperature range, tracking of three PA436's can easily be held to within a firing angle error of less than 5 electrical degrees. However, minor variations of the PA436 results in some dissymmetry of the positive and negative firing angles. For the control of inductive loads, it is therefore recommended that the PA436 be used in a single polarity pulse mode.

Figure 9.60 shows the PA436 being used in the lines of a delta or wye connected load. To obtain smooth control, it is necessary to use an SCR-rectifier combination as shown. This is necessary since the SCR-SCR combination requires either long gate pulses or a trigger sequence as shown in Figure 9.56(c) when used on a three wire system. With point "0" connected to a four wire system's neutral point the use of an SCR pair is mandatory. The neutral provides a path for the current during operation at short conduction angles. The control input circuit for the three PA436's is discussed below. R_5 is used to establish an artificial neutral in conjunction with C_2 which provides a phase to neutral voltage which can be used as a reference for the system.

A DC power supply application for the PA436 is shown in Figure 9.61. This circuit has the same power circuit as that of Section 9.9.1, but since three separate triggers are used smooth control can be achieved from 3 to 97% of full power. It should be noted that Pins 10 and 6 are not connected together. These terminals are not common to one another within the PA436 and may never be tied together. Since a different voltage exists at these two points the PA436's can never share a common control input and timing voltage for all three phases. Note also that the control input Pin 10 of phase 1 is not tied to the corresponding pins of phases 2 and 3. Again because each phase's Pin 10 is at a different potential than the common Pin 6.

To provide control for three isolated PA436's three floating dc power supplies are needed. Figure 9.62 shows one way of accomplishing this. The PA237 is a high gain ac amplifier with sufficiently low output impedance to drive the three supplies. It can be driven directly from an ac error signal or a dc error signal which modulates the ac reference source by means of a field effect transistor. The control time constant is limited by the filters needed for the three independent

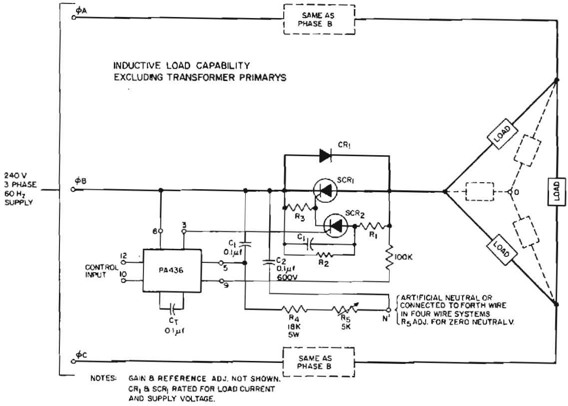


FIGURE 9.60 PHASE CONTROL OF THREE PHASE CIRCUITS CONTROLLING LINE CURRENTS

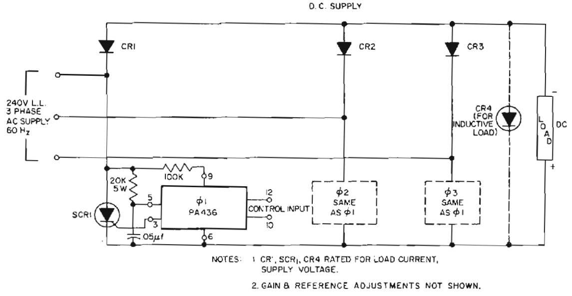


FIGURE 9.61 THREE PHASE DC POWER SUPPLY USING PA436's

power supplies. If for closed loop applications a shorter time constant is desired the reference AC frequency should be raised. This will reduce the needed R-C filter time constant on each supply and yet maintain the same filtering action.

In order to insure proper tracking of the control trigger angles between phases, gain and reference adjustments are needed on two phases. They are shown on phases A and B as potentiometers R_{10} and R_{13} in phase A and R_{21} and R_{24} in phase B.

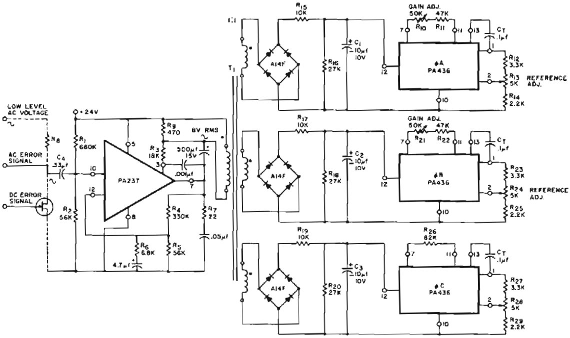


FIGURE 9.62 THREE PHASE FLOATING POWER SUPPLY CONTROL CIRCUIT USING PA237 FOR CONTROL OF PA436's

The three floating power supplies can be powered from a PA436 and a SC35B triac as shown in Figure 9.63. The circuit uses the PA436 in a single phase mode which provides smooth continuous control of the AC voltage supplied to the three floating DC supplies.

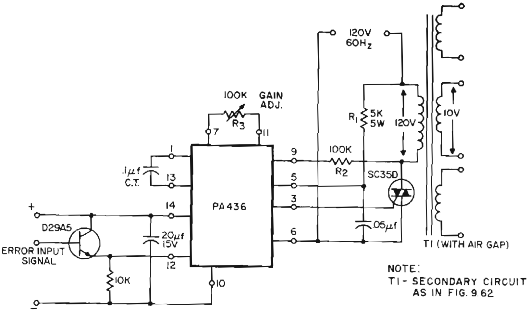


FIGURE 9.63 THREE PHASE FLOATING POWER SUPPLY CONTROL CIRCUIT USING PA436 FOR PHASE CONTROL

There may be applications where it is desirable to common the control inputs of the PA436's and float only the AC timing line voltages as shown in Figure 9.64. This would provide rapid response to control input variations at the expense of necessitating three pulse transformers and three control transformers to provide the AC timing line voltages.

Figure 9.64(a) as shown is suitable only for resistive loads since its lockout circuit is not sensing SCR pair voltages. Figures 9.64(b) and (c) provide for inductive load operation by means of light coupling between the SCR pair and the PA436's. This is accomplished by means

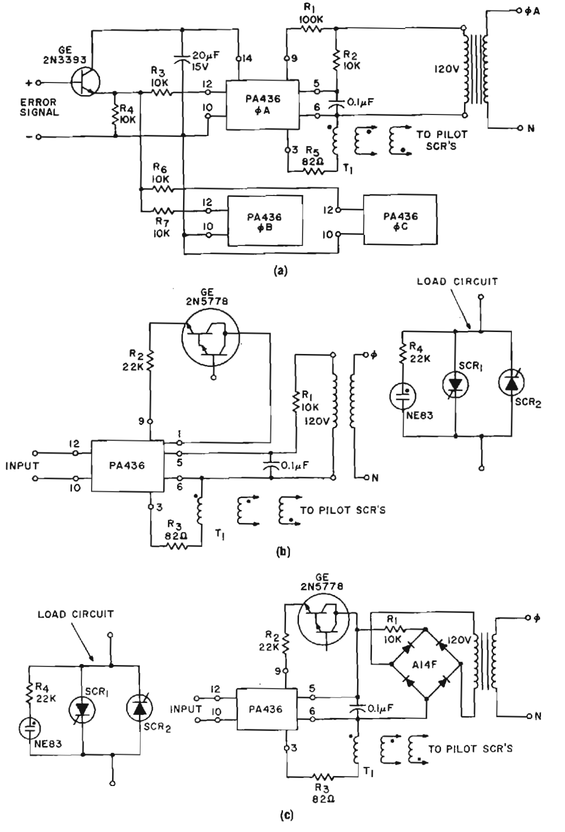


FIGURE 9.64 VARIATIONS OF PA436 POLYPHASE CIRCUIT FOR COMMON INPUT

of a neon bulb placed across each SCR pair and coupled to the L14B's which control the PA436 inductive lockout circuit.

The circuit shown for Figure 9.64(c) is suitable for controlling transformer primaries. The trigger angle timing is forced to be symmetrical between alternate positive and negative load half cycles because the PA436 only sees positive half cycles provided by the rectifier bridge. Therefore identical circuitry is used to provide the timing for alternate trigger pulses. Because of this inherent trigger timing symmetry no DC voltage should be impressed across the driven transformer primary.

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*See Chapter 23 for availability and ordering information.

10 MOTOR CONTROLS EMPLOYING PHASE CONTROL

10.1 INTRODUCTION

Since the AC power line is so universally convenient, and since phase control is the most convenient way of regulating this power source, it is little wonder that phase control has been used to control such a wide variety of motor types. Most of the motors so controlled however were not designed for this type of operation and were used because they were available or were low priced. Often the simplicity of the control circuits is due to a dependence on motor characteristics, and an improper motor selection will cause poor circuit operation. Also, even the best control circuit is only part of an overall system, and can be no more successful than the overall system design.

Most motors are given their ratings based on operation at a single speed, and depend on this speed for proper cooling. Attempts to use a motor at a lower speed can cause heating problems. The lubrication of bearings can also be inadequate for low-speed operation. The presence of odd order harmonics in the phase-controlled wave form, can produce some odd side effects in induction motors. The speed vs. torque characteristic of a particular induction motor may make it totally unsuitable for use with a variable voltage control system. Some controls for universal series motors depend heavily on the existence of a significant residual magnetism in their magnetic structures, a characteristic that the motor vendor could be inadvertently trying to minimize.

These potential problems are brought up to a point out the importance of checking with the motor manufacturer to insure that the motor used is the proper one for this type of use.

The use of a properly chosen and designed motor with a control of this type can however allow a wide versatility in application. For instance a temperature compensated furnace blower control can replace a wide variety of motor sizes and speeds. Now a single, standard motor can be used with the variable requirements in different installations, being compensated by means of electrical adjustments at the control. In some cases, where the maximum speed of the motor is set by the control, the need for designing overvoltage capability into the motor is eliminated, thus allowing some saving in the motor design.

10.2 BRUSH-TYPE MOTORS CONTROLLED BY BACK EMF FEEDBACK

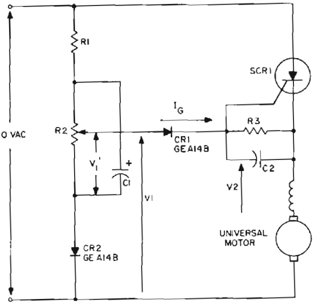
In order for a circuit to govern the speed of a motor, it must be able to somehow sense the speed of that motor. The most easily available way to get this information from brush-type motors is by looking at the back EMF generated by the motor during the time that the

controlling SCR is off. In the case of separately excited shunt field wound, and permanent magnet field motors, this EMF is directly proportional to speed. In series motors, the field is not energized at this time, and residual magnetism must provide the back EMF used by the circuit. Unfortunately, the residual magnetism is a function of the past history of motor current, so the voltage the circuit sees is not a function of speed alone.

Care must also be taken in these circuits that brush noise does not interfere with circuit operation.

10.2.1 Half-Wave Universal Series Motor Controls

The universal series motor finds use in a wide variety of consumer and light industrial applications. It is used in blenders, hand tools, vacuum cleaners, mixers, and in many other places. The control circuits to be described here can provide the effect of an infinitely variable tap on the motor.



(A)

	LOW UP TO 1 AMP NAMEPLATE	MEDIUM UP TO 3 AMP NAMEPLATE	HIGH UP TO 15 AMP NAMEPLATE
R2	10K 1W	1K 2W	1K 2W
R1	47K 1/2 W	3.3K 2W	3.3K 2W
R3	1K 1/2W	150K 1/2W OPTIONAL	150K 1/2W OPTIONAL
C1	0.5µf 50V	10µf 50V	10µf 50V
C2	0.1 µf 10V	0.1µf 10V OPTIONAL	0.1µf 10V OPTIONAL
SCR1	GE C106B	GE C228X70	GE C33B

Note for 220V, 50/60 Hz Operation: Double value of R_1 and use at Least 400 V Semiconductors (SCR & Diodes)

(B)

FIGURE 10.1 UNIVERSIAL SERIES MOTOR CONTROL WITH FEEDBACK

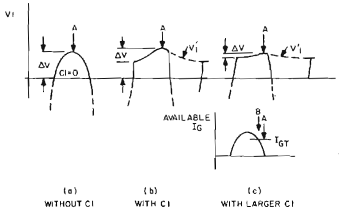


FIGURE 10.2 WAVESHAPES FOR FIGURE 10.1

The half-wave circuits of Figures 10.1, 10.3 and 10.4 supply half wave DC to the motor. In order to have full-speed operation with these circuits, the motor must be designed for a nominal voltage of around 80 volts for operation on 120 volt AC lines or 170 volts for operation at 240 VAC. Brush life of a motor driven by half-wave supply may be somewhat shorter than for a corresponding motor on full-wave AC.

The three half-wave circuits shown employ residual back-EMF feedback to provide increased motor power as the speed of the motor is reduced by mechanical loading. This back EMF voltage is dependent on the residual magnetism of the motor which is determined by the magnetic structure of the motor and the characteristics of the iron. Care must be taken to ensure that the motor used has sufficient residual magnetism. For more information see Reference 1.

The circuit of Figure 10.1 operates by comparing the residual back EMF of the motor V_2 with a circuit generated reference voltage V_1. If the capacitor C_1 is not present, the voltage V_1 is the result of the divider network composed of R_1 and the potentiometer R_2. Current flows in this branch only during the positive half-cycle due to diode CR_2. The voltage at V_1 then is a half sine wave with a maximum value at time "A" (Figure 10.2(a)). If the residual back EMF is greater than this maximum (the motor is going faster than the selected speed), CR_1 will be reverse biased and the SCR will not be triggered and will not supply power to the motor during this half cycle. As the motor slows down and its back EMF drops, V_2 will become slightly less than V_1 at time "A," causing current to flow through CR_1 and the gate of SCR_1, thus triggering the SCR. The speed at which CR_1 conducts occurs may be varied by adjusting potentiometer R_2 which changes the magnitude of V_1. Notice that the smallest impulse of power that can be applied to the motor is one-quarter cycle, since the latest point in the cycle that the SCR can trigger is at the peak of the AC line voltage.

If the motor is loaded down so that its speed and back-EMF continue to drop, the time at which V_1 becomes greater than V_2 comes earlier in the cycle causing the SCR to trigger earlier, supplying more power to the motor. If, however, the motor is lightly loaded and running at a low speed, one-quarter cycle power may be enough to change the motor speed by a considerable amount. If this happens, it may take a considerable number of cycles to return to the speed at which the SCR will again trigger. This causes a hunting or "cogging" effect which is usually accompanied by an objectionable amount of mechanical noise.

In order to alleviate this problem, the smallest increment of power available must be reduced from a full-quarter cycle to that amount required to just compensate for the motor energy lost per cycle. To accomplish this, capacitor C_1 is added to the circuit. The capacitor voltage becomes a sinusoid in shape during the positive half cycle. This voltage is phase shifted by an amount determined by the circuit time constant and an exponential decay during the negative half cycle.

Figure 10.2(b) shows the results on V_1. Two main effects may be observed. The first is that the latest possible triggering point "A" is delayed, thereby considerably reducing the smallest increment of power. The second is that the amount of change of V_2 required to go

from minimum power to full power, ΔV, is reduced, providing a more effective control. Increasing C_1 even more produces the results of Figure 10.2(c). It can be seen that the triggering point "A" comes still later, and ΔV becomes still smaller. Care must be taken however not to go too far in this direction, for increasing C_1 decreases ΔV and increase the loop gain of the system which could lead again to instability and hunting.

It is important that the impedance level of the network formed by R_1, R_2 and C_1 be low enough to supply the current required to trigger the SCR without undue loading. It can be seen in Figure 10.2(c) that this current available for triggering from this network approaches a sine wave, with its peak at 90°. If the current required to trigger the SCR is I_{GT} as shown, the latest possible firing point would be at "B," not at "A" as one would believe from the voltage wave shape.

In many cases, good low-speed operation without a restrictive specification on gate current to fire would require such a low impedance network that the power ratings of the resistors and the capacitor size would become unwieldly and expensive. In such cases, a low-voltage trigger device such as an SUS can act as a gate amplifier as in Figure 10.3. Use of the SUS in this circuit allows a much higher impedance network to be used for R_1, R_2 and C_1; hence allowing smaller size and lower cost components. In this circuit the reference voltage V_1 must exceed the back EMF V_2 by the breakover voltage of SUS_1, which is about 8 to 10 volts. When SUS_1 triggers it discharges C_2 into the gate, supplying a strong pulse of current to trigger SCR_1. This eliminates any need to select SCR's for gate trigger current, and eliminates any circuit dependence on the trigger current of the particular SCR used.

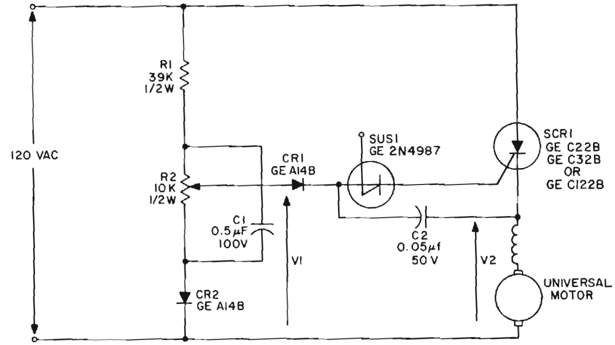


FIGURE 10.3 SUS TRIGGERED UNIVERSAL SERIES MOTOR SPEED CONTROL WITH FEEDBACK

Another method of eliminating gate trigger characteristics from the control's performance is to use a system such as shown in Figure

10.4. Although this circuit also uses the motor counter EMF as a feedback signal, the balance of the system is different. The area enclosed by the dashed box contains a cosine modified ramp and pedestal circuit very similar to those described in Section 9.5.2. In this system R_4 and R_5 form the pedestal with R_2 and R_3 providing the ramp current. As explained in Chapter 4 the Programmable Unijunction Transistor, Q_1, has a variable standoff ratio which is determined by the gate voltage divider, which, for this circuit, consists of resistors R_6 and R_7.

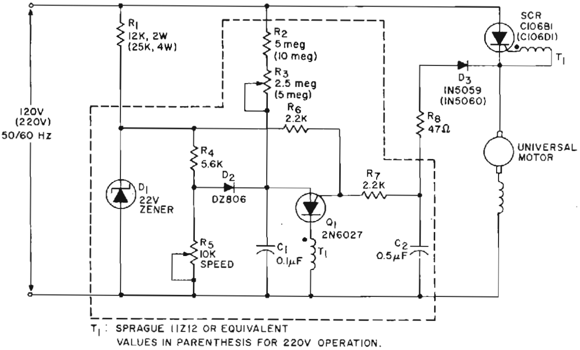


FIGURE 10.4 PROGRAMMABLE UNIJUNCTION TRANSISTOR TRIGGERED UNIVERSAL MOTOR CONTROL WITH FEEDBACK

The system operates as follows. At the beginning of the positive half cycle as the line voltage rises the zener blocks current until the voltage across it reaches 22 volts, at this time the zener clamps the voltage across it to 22 volts. During the first part of the cycle the capacitor C_1 is charged to a voltage determined by the R_4, R_5 divider. At the same time in the gate circuit the voltage on C_2 is building up. When the voltage on C_2 equals the back EMF plus the forward drop of D_3 the diode conducts and clamps the voltage on C_2 to that value. It can be seen as the motor speed varies this level will change with speed. When the capacitor C_1 voltage exceeds the gate of Q_1 then Q_1 turns on and triggers the SCR by transferring the charge on C_1 to the SCR gate through the pulse transformer T_1. It can be seen that if the speed is lower than desired the firing angle will advance due to the higher pedestal and conversely if the speed is too high the triggering angle will be retarded.

10.2.2 Full-Wave Universal Series Motor Control

Figure 10.5 shows the circuit of a full wave series motor speed control with feedback which requires that separate connections be

available for the motor armature and field. The full wave bridge supplies power to the series networks of motor field, SCR_1 and armature R_1 and R_2. Basically this circuit works on the same principle as that of Figure 10.1(a) using the counter EMF of the armature as a feedback signal. When the motor starts running, the SCR triggers as soon as the reference voltage across the arm of R_2 exceeds the forward drop of CR_1 and the gate to cathode drop of SCR_1. The motor then builds up speed, and as the back EMF increases, the speed of the motor adjusts to the setting of R_2 in the same manner as the circuit of Figure 10.1(a).

Motor Current	SCR	CR2-5
6 A 25A	C22B or C122B C32B	A15B A44B/A45B

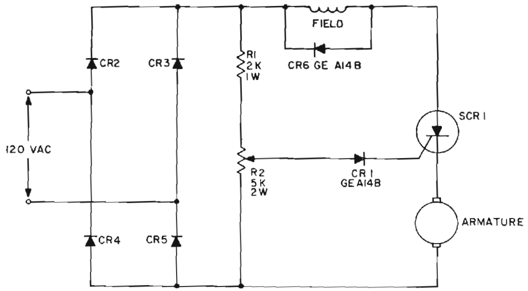


FIGURE 10.5 FULL WAVE DC CONTROL WITH FEEDBACK

One of the drawbacks of this circuit is that at low speed settings, the anode to cathode voltage of the SCR may not be negative for a sufficient time for the SCR to turn off because of the decreased back EMF. When this happens, the motor receives full power for the succeeding half cycle and the motor starts hunting. Furthermore, this circuit is limited by the fact that SCR_1 cannot be fired consistently later than 90°. A capacitor on the arm of R_2 is not a cure because there will be no phase shift on the reference due to full wave rectified charging.

10.2.3 Shunt Wound and P-M Field Motor Control

The shunt-wound DC motor is well suited for use with solid state speed control systems to provide smooth, wide-range control of speed. The speed of a shunt motor is inherently reasonably constant with changes in torque, thus permitting speed control to be achieved by controlling the voltage applied to the armature. The use of a small compound series winding can make the speed virtually independent of torque. Likewise, a small amount of feedback of speed information

into the control that supplies armature voltage will reduce variations of speed with torque.

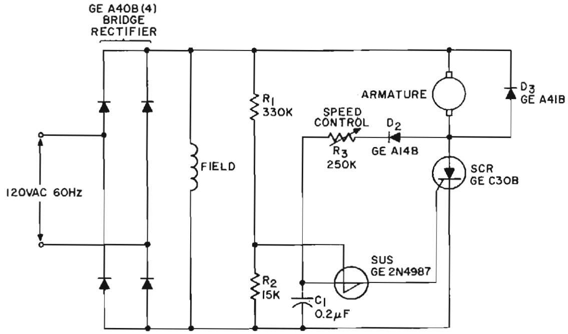


FIGURE 10.6 SPEED CONTROL FOR 1/2 HP, 115 VOLT SHUNT-WOUND DC MOTOR

Figure 10.6 shows a simple and low-cost solid state speed control for shunt-wound DC motors. This circuit uses a bridge rectifier to provide full wave rectification of the AC supply. The field winding is permanently connected across the DC output of the bridge rectifier. Armature voltage is supplied through the SCR and is controlled by turning the SCR on at various points in each half cycle, the SCR turning off only at the end of each half cycle. Rectifier D_3 provides a circulating current path for energy stored in the inductance in the armature at the time the SCR turns off. Without D_3, the current will circulate through the SCR and the bridge rectifier thus preventing the SCR from turning off.

At the beginning of each half cycle the SCR is in the off-state and capacitor C_1 starts charging by current flow through the armature, rectifier D_2, and the adjustable resistor R_3. When the voltage across C_1 reaches the breakover voltage of the SUS trigger diode, a pulse is applied to the SCR gate, turning the SCR on and applying power to the armature for the remainder of that half cycle. At the end of each half cycle, C_1 is discharged by the triggering of the SUS, resistor R_1, and current through R_1 and R_2. The time required for C_1 to reach breakover voltage of the SUS governs the phase angle at which the SCR is turned on and this is controlled by the magnitude of resistor R_3 and the voltage across the SCR. Since the voltage across the SCR is the output of the bridge rectifier minus the counter EMF across the armature, the charging of C_1 is partially dependent upon this counter EMF, hence upon the speed of the motor. If the motor runs at a slower speed, the counter EMF will be lower and the voltage applied to the charging circuit will be higher. This decreases the time required to trigger the SCR, hence increases the power supplied to the armature and thereby compensates for the loading on the motor.

Energy stored in armature inductance will result in the current flow through rectifier D_3 for a short time at the beginning of each half cycle. During this time, the counter EMF of the armature cannot appear hence the voltage across the SCR is equal to the output voltage of the bridge rectifier. The length of time required for this current to die out and for the counter EMF to appear across the armature is determined by both speed and armature current. At lower speeds and at higher armature currents the rectifier D_3 will remain conducting for a longer period of time at the beginning of each half cycle. This action also causes faster charging of capacitor C_1, hence provides compensation that is sensitive to both armature current and to motor speed.

This circuit provides a very large range of speed control adjustment. The feedback signal derived from speed and armature current improves the speed regulation over the inherent characteristics of the motor.

Another circuit which operates on a similar system is the one of Figure 10.7. The advantage of this circuit is that for motors whose field current is less than 4 amperes only four stud mounted semiconductors are needed since diodes D_3 and D_4 carry only field current. The second and probably more important point is that these SCR's can under no condition fail to turn off.

In the circuit SCR_1 and SCR_2 conduct current on alternate half waves but are triggered from the same trigger circuit. The SCR's therefore carry only one half the current of the SCR in Figure 10.6. Diodes D_1 and D_2 conduct both armature and field current where, as mentioned above, D_3 and D_4 conduct only field current. For currents up to 1.5 ampere the GE A14B rectifier can be used, for up to 4.5 amperes the GE A15B. The advantage of these units is that they are lead mounted and therefore need no heat sinking except for their tie points.

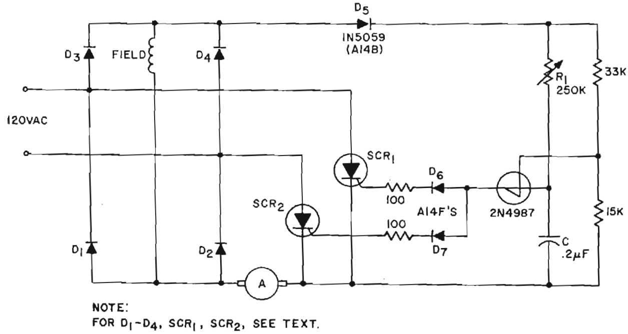


FIGURE 10.7 SCR SHUNT OR PM MOTOR SPEED CONTROL

In this circuit the small amount of feedback which is required for a shunt motor is the sensing of the armature back EMF. The back EMF is in the charging path for the capacitor C so the charging is delayed

an amount determined proportional to the back EMF.

Inductance of the field winding of a shunt motor is generally rather large, resulting in a significant length of time required for the field current to build up to its normal value after the motor is energized. In general, it is desirable to prevent application of power to the armature until after the field current has reached approximately normal value. This sort of soft start function is readily added. For information on soft starting, see Chapter 9 and Reference 2.

This relatively simple approach is capable of moderately good speed regulation on the order of 10 percent. For higher performance, a tachometer feedback circuits as discussed in Section 10.4.3 can be substituted for the trigger circuit.

10.3 BRUSH-TYPE MOTOR CONTROL—NO FEEDBACK

In many cases speed regulation is not required in the control. Where the load characteristics are relatively fixed, or where the motor drive is part of a larger overall servo system, a non-regulating control circuit may be used. In some cases, these non-regulating circuits can provide a considerable cost saving over regulated types.

10.3.1 Half-Wave Drive for Universal, Shunt or P-M Motors

Figure 10.8 illustrates one of the simplest and least expensive half wave circuits. It uses one SCR with a minimum amount of components. The series network of R_1, P_1, and C_1 supplies a phase shift signal to the neon bulb which triggers the SCR. Thus, by varying the setting of potentiometer P_1, the gate signal of the SCR is phase shifted with respect to the supply voltage to turn the SCR on at varying times in the positive AC half cycles. V_c fires the neon bulb on both positive and negative half cycles. The negative half cycles can be disregarded since both the trigger pulses and the anode voltage of the SCR are negative.

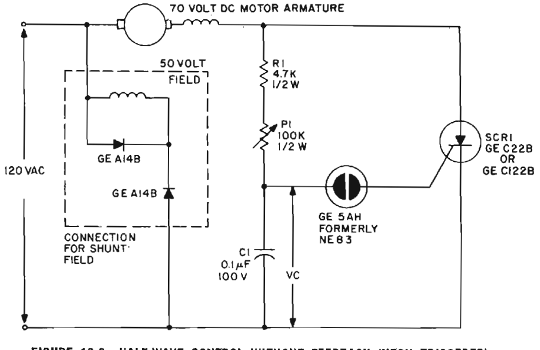


FIGURE 10.8 HALF-WAVE CONTROL WITHOUT FEEDBACK (NEON TRIGGERED)

By replacing the neon with a trigger device, such as a Diac (the GE ST2) or a Silicon Unilateral Switch (the GE 2N4987), the performance and reliability of the circuit of Figure 10.8 can be improved considerably because semiconductor trigger devices are longer-lived and have a more stable triggering point than neon bulbs. Also, because of their lower trigger voltage, these solid state trigger devices give a wider control range. The values of the R-C phase shift network would have to be increased to compensate for the lower breakover voltages of these devices.

10.3.2 Full-Wave AC Drive for Universal Series Motors

Since the universal series motor is generally designed to run on the 50 or 60 Hz AC lines, the simplest approach to a non-regulating control is the full wave phase control circuit of Figure 10.9. More details on the operation of this type of circuit can be found in Chapter 9.

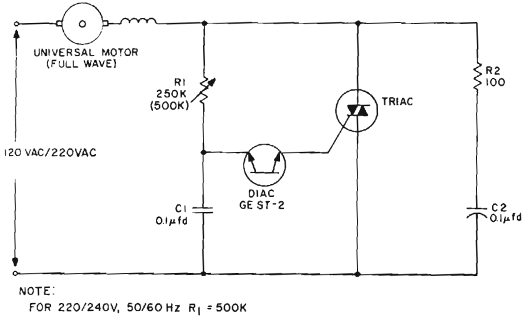


FIGURE 10.9 BASIC NON-REGULATED FULL-WAVE AC PHASE CONTROL FOR UNIVERSAL MOTORS

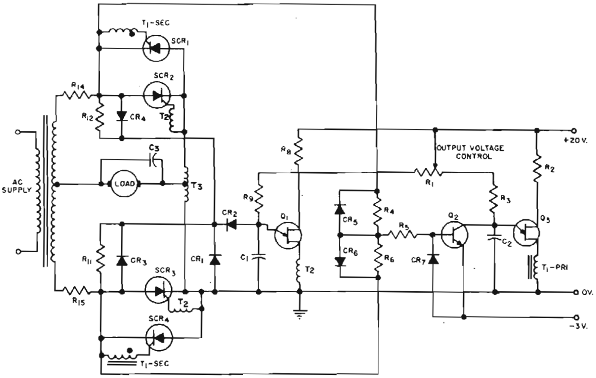
10.3.3 Full-Wave DC Motor Drives

SCR's are well suited for supplying both armature power and field excitation to DC machines.

A full wave reversing control or servo as shown in Figure 10.10 can be designed around two SCR's with common cathode (SCR_2, SCR_3) and two SCR's with common anodes (SCR_1, SCR_4). In this circuit SCR_2 and SCR_3 are controlled by UJT Q_1 and the other pair, SCR_1 and SCR_4, are controlled by UJT Q_3. Transistor clamp Q_2 synchronizes the triggering of Q_3 to the anode voltages across SCR_1 and SCR_4.

Potentiometer R_1 can be used to regulate the polarity and the magnitude of output voltage across the load. With R_1 at its center position, neither UJT triggers and no output voltage appears across the load. As the arm of R_1 is moved to the left, Q_1 and its associated SCR's begin to trigger. At the extreme left-hand position of R_1, full output voltage appears across the load. As the arm of R_1 is moved to the right of center, similar action occurs except the polarity across the load is reversed.

If the load is a DC motor, plugging action occurs if R_1 is reversed abruptly. R_{14} and R_{15} are used in series with each end of the transformer to limit fault current in the event a voltage transient should trigger an odd- or even-numbered SCR pair simultaneously. Commutating reactor T_3 and capacitor C_3 limit the dv/dt which one pair of SCR's can impress upon the opposite pair.



R_1 — 100K LINEAR POT
R_2, R_8 — 470 OHMS, 1/2 WATT
R_3, R_9 — 2700 OHMS, 1/2 WATT
R_4, R_6 — 10K, 2 WATTS
R_5 — 4700 OHMS, 1/2 WATT
R_{11}, R_{12} — 2200 OHMS, 2 WATTS
R_{14}, R_{15} — 2 OHMS, 500 WATTS OR LESS, DEPENDING ON RATING OF LOAD
C_1, C_2 — 0.2 MFD
$SCR_1, SCR_2, SCR_3, SCR_4$ — GE SCR (VOLTAGE RATING DEPENDENT ON SECONDARY TRANSFORMER VOLTAGE)
$CR_1, CR_2, CR_3, CR_4, CR_5, CR_6$ — GE 1N5060
CR_7 — GE A14F
Q_1, Q_3 — GE 2N1671A
Q_2 — GE GET 2222
T_1, T_2 — PE2231, SPRAGUE 11Z13 OR EQUIVALENT
T_3, C_3 } AS REQUIRED BY LOAD

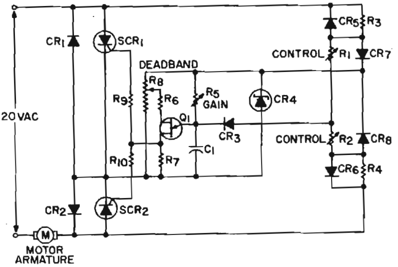
FIGURE 10.10 FULL WAVE REVERSING DRIVE

10.3.4 Balanced-Bridge Reversing Servo Drive

A phase-sensitive servo drive supplying reversible half wave power to the armature of a small permanent magnet or shunt motor is shown in Figure 10.11. The power circuit consists of two half-wave circuits back-to-back (SCR_1, CR_1; and SCR_2, CR_2) triggered by unijunction transistor, Q_1, on either the positive or negative half-cycle of line voltage depending on the direction of unbalance of the reference bridge resulting from the value of the sensing element R_1. R_1 can be a photo-resistor, a thermistor, a potentiometer, or an output from a control amplifier.

The potentiometer R_8 is set so that the DC bias on the emitter of unijunction transistor, Q_1, is slightly below the peak-point voltage at which Q_1 triggers, by an amount dependent upon the deadband desired. With R_1 equal to R_2 the bridge will be balanced, UJT (Q_1) will not trigger and no output voltage appears across the load. If R_1 is increased thus unbalancing the bridge, AC signal will appear at the emitter of the UJT causing the emitter to be biased above the trigger voltage during one half-cycle of the AC. Q_1 will trigger and, since SCR_2 is forward biased, SCR_2 will trigger. When R_1 is decreased,

similar action occurs except that SCR_1 will trigger, reversing the polarity across the load.



CR1, CR2, SCR1, SCR2 : AS REQUIRED BY LOAD
R1 : 3.3K } SEE NOTE
R2 : 3.3K }
R3 : 3.3K, 2W
R4 : 3.3K, 2W
R5 : 2 MEGOHMS
R6 : 1K
R7 : 47Ω
R8 : 2500Ω
R9 : 47Ω
R10 : 47Ω
C1 : 0.1μf
Q1 : GE 2N2646
CR4 : GE 1N1776
CR5-8 : GE 1N5060
CR3 : GE DT230A

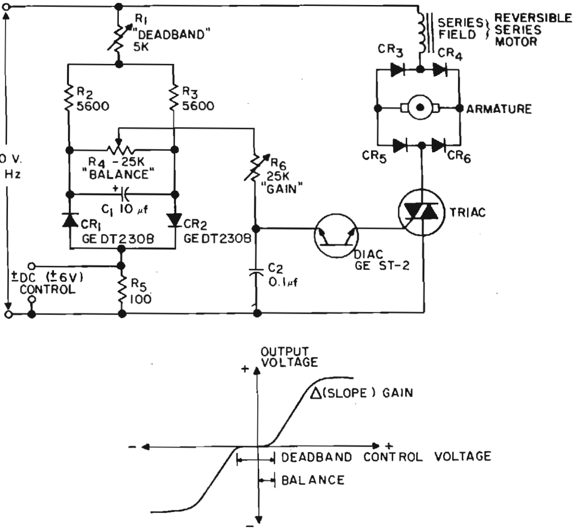
NOTE:
EITHER R1 OR R2 MAY BE A VARIABLE RESISTANCE TRANSDUCER, SUCH AS THE GE B425B PHOTOCONDUCTOR, OR A THERMISTOR, OR A POSITION SENSING POTENTIOMETER.

FIGURE 10.11 BALANCED-BRIDGE REVERSING SERVO DRIVE FOR SHUNT-WOUND MOTORS

If instead of a shunt wound motor, the servo motor is series wound, a circuit similar to Figure 10.12 can be used. In this circuit the triac is triggered only on either the positive half wave or the negative half wave. Since the armature is within a bridge the armature voltage is of one polarity regardless of which half cycle the triac is energized. The field winding current, on the other hand, is reversed with a change of triac triggering polarity. The triac control circuit features control of all the control parameters, gain, balance and deadband and also provides for an analog control voltage input. If desired the balance pot can be replaced by a pair of resistive transducers or a positioning potentiometer.

10.4 INDUCTION MOTOR CONTROLS

There are a wide variety of induction motor types and within these a wide range of possible characteristics. Some of these characteristics can make a given motor type unsuited for control by means of phase control. The most obvious difficulty is that induction motors tend to be more frequency sensitive than voltage sensitive, while phase control generates a variable-voltage, constant-frequency source. If the motor was not designed for use with phase control, the motor designer may have accentuated this problem in order to get better speed regu-



Motor Current	Diodes $CR_3 - CR_6$	Triac
1.5 A	A14B	SC141B
4.5 A	A15B	SC141B
4.5 A	A40B / A41B	SC51B

FIGURE 10.12 BALANCED BRIDGE REVERSING SERVO DRIVE FOR SERIES-WOUND MOTOR

lation. In general, the motor used should be as voltage sensitive as possible. Variable voltage drive of induction motors is a compromise, one usually dictated by economics but very satisfactory in properly implemented applications. A variable frequency drive would be superior in some applications, but generally far more expensive than phase control. Information on variable frequency inverters that can be used for drives can be found in Chapter 11.

Certain types of single phase induction motors, notably split-phase and capacitor start motors, require a switched start winding. Since there is a torque discontinuity when the start switch cuts in or drops out, it would be impossible to control the speed of the motor around these points. This means that where the higher starting torque of a switched start winding is required, the motor should be designed so

that the switching point is below the range of speed over which phase control is desired.

Another important consideration is the power factor of the motor. An overly inductive motor can require a fair degree of sophistication in the control in order to avoid the problems associated with phase control of inductive loads. This topic is covered in detail in Section 9.6.

10.4.1 Non-Feedback Controls

Unlike brush type motors, induction motors give no convenient electrical indication of their mechanical speed. This means that direct speed feedback is not nearly as easily available. For some applications like fixed fan loads, direct voltage adjustment with no feedback yields satisfactory performance. An example is the circuit of Figure 10.9 when working with a permanent split capacitor motor or with a shaded pole motor. The need for the proper motor-load combination is shown by the speed torque curves of Figure 10.13. In the case of a low rotor resistance, Figure 10.13(a), it can be seen that varying the voltage of this motor will produce very little speed variation, while the higher rotor resistance motor of Figure 10.13(b) would give satisfactory results.

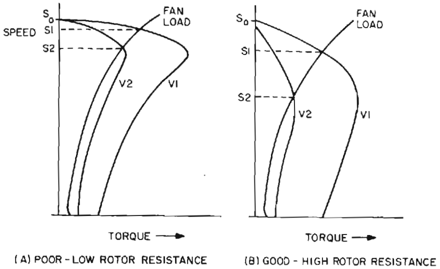


FIGURE 10.13 INDUCTION MOTOR SPEED-TORQUE CURVES FOR USE WITH A FAN-TYPE LOAD

10.4.2 Indirect Feedback

Often the problem of speed regulation of induction motors may be bypassed by considering the complete system control problem. As an example, consider the problem of controlling the speed of the blower in a hot air heating system in response to the temperature of the air. It can be seen that what is of prime interest is the temperature of the air, not the precise speed of the motor. This kind of analysis can lead to the circuit of Figure 10.14.

In this circuit, thermistor R_3 acts in response to air temperature to control the power supplied to the motor. Resistor R_1 and its phase control network serve to set a minimum blower speed, to provide con-

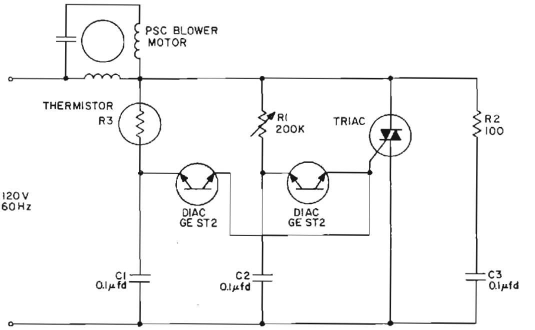
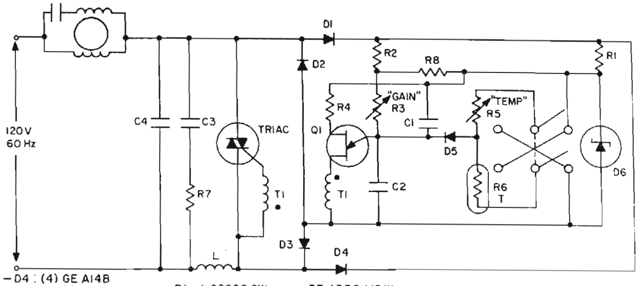


FIGURE 10.14 FURNACE BLOWER CONTROL

tinuous air circulation and to maintain motor bearing lubrication.

Figure 10.15 gives an example of a more sophisticated control system, capable of a much higher control gain. This could be used to control a blower motor in response to room temperature for heating control, or in response to cooling coil temperature to prevent air conditioner freeze-up.



D1 – D4 : (4) GE A14B OR (1) GE B102
D5 : GE A14 A
D6 : GE 1N1776
Q1 : GE 2N2646
C1 & C2 : 0.1μf, 50V

R1 : 6800Ω 2W
R2 : 470KΩ 1/2W
R3 : 5 MEG 1/2W
R4 : 1KΩ 1/2W
R5 : 10KΩ 1W
R6 : SEE NOTE

R7 : 33Ω 1/2W
C3 : 0.02μf, 200V
T1 : XFMR 1:1 : SPRAGUE 11Z12 OR EQUIV.
C4 : 0.1μf 400V
R8 : 470KΩ 1/2W

NOTE: IN THE ABOVE ARRANGEMENT CIRCUIT IS SET UP FOR A HEATING APPLICATION. IN A COOLING APPLICATION R6 & R5 ARE INTERCHANGED. R6 SHOULD BE A THERMISTOR WHICH WILL AFFORD 3KΩ TO 5KΩ AT TEMPERATURE DESIRED. "TEMP ADJ" R5 SHOULD BE SET UP TO PROVIDE FULL "ON" AT DESIRED UPPER TEMP. OF THE THERMISTOR R6. "GAIN" R3 OR "BANDWIDTH" MAY THEN BE SET FOR "FULL OFF" (ZERO SPEED) CONDITION AT DESIRED "LOWER TEMP" OF R6.

FIGURE 10.15 TEMPERATURE CONTROL OF SPEED; SHADED POLE AND TSC MOTORS

This is a ramp-and-pedestal system designed for the control of fan or blower motors of the shaded pole or permanent split capacitor

type in response to temperature of a thermistor. The circuit includes RF noise suppression and dv/dt suppression.

10.4.3 Speed Regulating Control of Induction Motors

In order to actually regulate the speed of an AC induction motor by means of phase control, it is necessary to provide speed information to the circuit by means of a small tachometer generator. Such a generator could be made quite inexpensively, as high precision is not necessarily required. In addition, the speed torque characteristics of the motor should be quite voltage sensitive such as that of Figure 10.13(b). A motor such as that of Figure 10.13(a) would be quite difficult to control in a stable manner, as the open loop system characteristics would be highly nonlinear through the controlled speed range. The drop-out point of the start switch, if present, should be below the lowest desired controlled speed.

Figure 10.16 shows a general block diagram of such a control system. For a practical circuit, a ramp and pedestal control circuit, with inductive load consideration (as shown in Figure 9.35) can be combined with the input connection shown in Figure 10.17. This con-

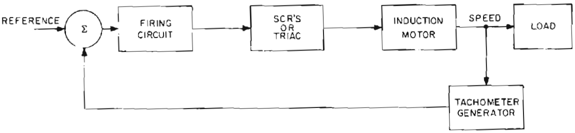


FIGURE 10.16 BLOCK DIAGRAM OF AN INDUCTION MOTOR SPEED CONTROL SYSTEM

nection is shown for an AC tachometer in the 4 to 6 volt range. The R_1-C_2 time constant is chosen to give adequate filtering at the lowest desired speed and tachometer frequency, consistent with system sta-

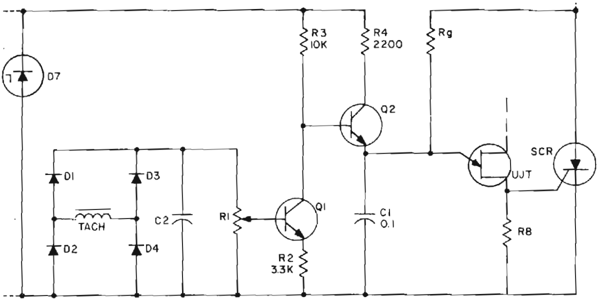


FIGURE 10.17 AC TACHOMETER CONNECTION TO A RAMP AND PEDESTAL TRIGGERING CIRCUIT

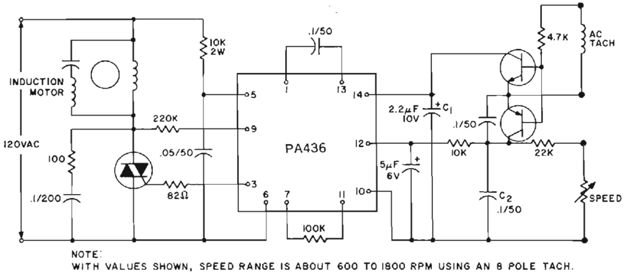


FIGURE 10.18 INDUCTION MOTOR SPEED CONTROL USING THE PA436 AND A FREQUENCY DEPENDENT TACHOMETER CIRCUIT

bility requirements. This system is also applicable to multiphase controls as well as DC motor drives.

For higher performance systems the PA436 can be used. Either ac or dc tachometers can give adequate speed control. Figure 10.18 shows an induction motor speed control using an ac tachometer. Each time the ac tachometer output swings positive, C_1 and C_2 are charged, and on the negative swing C_1 is discharged. The speed control potentiometer controls the discharge of C_2 and hence the apparent feedback voltage presented to pin 12 of the PA436. Section 9.7 can be referred to for details of the PA436

Figure 10.19 shows two other tachometer connections that can be used with the PA436. In these connections it is important that the output voltage of the tachometer is proportional to speed and has a voltage of at least 4 volts at minimum speed.

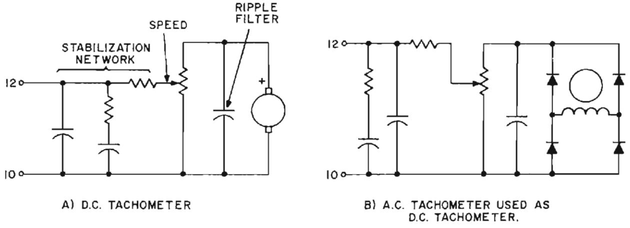


FIGURE 10.19 OTHER PA436 TACHOMETER INPUTS

10.5 SOME OTHER MOTOR CONTROL POSSIBILITIES

In addition to controlling or varying the speed of a motor, there are several other control functions which can be done using solid-state control.

One of the simplest functions is the use of a triac as a static switch for contactor replacement. When used with a reversing-type permanent split capacitor motor, a pair of triacs can provide a rapidly responding, reversing motor control, as shown in Figure 10.20. S_1 and S_2 can be

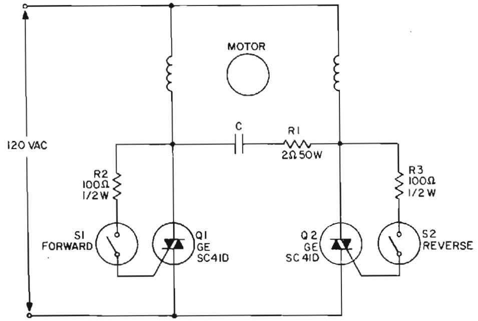


FIGURE 10.20 TRIAC CONTROL OF A REVERSIBLE PERMANENT SPLIT CAPACITOR MOTOR

reed switches, or the triacs can be gated by any of a number of other methods. Also, use of a solid-state static switching circuit, with an appropriate triggering circuit, can provide a motor overtemperature control which senses motor winding temperature directly.

In this circuit it is important to insure that the triacs have sufficient voltage rating. It can be seen that if one triac is on the other triac must block voltage that is greater than line voltage due to the L-C ring between the capacitor and the motor winding. As a rule of thumb the triac voltage rating should be 1.5 times the capacitor's voltage rating.

The second point regarding Figure 10.20 is that R_1 be sized correctly to insure that if one triac is switched on when the other is conducting, the surge current from the capacitor discharge is limited to a safe value.

10.5.1 Single-Phase Induction Motor Starters

In many cases, a capacitor start or a split-phase motor must operate where there is a high frequency of starts, or where arcing of the mechanical start switch is undesirable, such as where explosive fumes could be present in the neighborhood of the motor. In such cases, the mechanical start switch may be replaced by a triac. The gating and dropout information may be given to the triac in several ways.

Perhaps the simplest form of connection is to use a conventional current or voltage sensitive starting relay as pilot contacts for a simple triac static switch as shown in Figure 8.1(a).

Another method is that shown in Figure 10.21 which shows the triac gated on by the motor current through a small current transformer. As the motor speeds up, the current drops off and no longer trigger the triac. A variation of this is to replace the current transformer with a small pickup coil, which is mounted near the end windings of the motor. This gives a somewhat more precise signal for the triac.

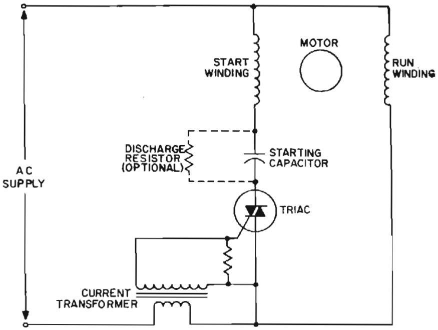


FIGURE 10.21 TRIAC MOTOR STARTING SWITCH

Where a tachometer generator is already sensing the speed of the motor, this same signal can be used to control a triggering circuit for the triac. With this arrangement the dropout speed can be precisely set, so as to be outside the desired speed control range.

REFERENCES

1. "Speed Control for Universal Motors," A.A. Adem, General Electric Company, Auburn, New York, Application Note 200.47.*
2. "Speed Control for Shunt-Wound DC Motors," E. Keith Howell, General Electric Company, Auburn, New York, Application Note 200.44.*
3. "Phase Control of SCR's With Transformer and Other Inductive AC Loads," F. W. Gutzwiller and J. D. Meng, General Electric Company, Auburn, New York, Application Note 200.31.*
4. "Using the Triac for Control of AC Power," J. H. Galloway, General Electric Company, Auburn, New York, Application Note 200.35.*

*Refer to Chapter 23 for availability and ordering information.

NOTES

11 ZERO VOLTAGE SWITCHING

11.1 INTRODUCTION

When a power circuit is switched "on" and "off", high frequency components are generated that can cause interference problems (see also Chapter 17). When power is initially applied, a step function of voltage is applied to the circuit which causes a shock excitation. Random switch opening chops current off, again generating high frequencies. In addition, abrupt current interruption in an inductive circuit can lead to high induced voltage transients.

The latching characteristics of thyristors are ideal for eliminating interference problems due to current interruption since these devices can only turn off when the on-state current approaches zero, regardless of load power factor.

On the other hand, interference free turn-on with thyristors requires special trigger circuits. It has been proven experimentally that general purpose AC circuits will generate minimum electromagnetic interference (EMI) if energized at zero voltage.

The ideal AC circuit switch therefore consists of a contact which closes at the instant when voltage across it is zero, and opens at the instant when current through it is zero. This has become known as "zero voltage switching."

Zero voltage switching is not new. First proposed in 1959[1], it is rapidly gaining considerable acceptance, particularly with regard to electrical heating applications.[2,3] This chapter will consider both discrete and monolithic integrated zero voltage switching circuits, its attendant benefits and problems, and potential uses of zero voltage switching at frequencies higher than 50 or 60 Hz.

11.2 ELECTROMAGNETIC INTERFERENCE

Each time a circuit is energized or de-energized, one must be concerned with the electrical disturbance which this may cause.[4] Each time a thyristor energizes a resistive circuit, load current goes from zero to the load limited current value in a few microseconds. The frequency analysis of such wave forms shows an infinite spectrum of energy in which the amplitude is inversely proportional to frequency. In applications where phase control is used, the AM broadcast band would suffer severe interference, for example, with less problems with TV and FM as shown in Figure 11.1. This curve shows a plot of quasi-peak microvolts of conducted interference. This is one of two basic types of radio frequency interference. In addition to that which is conducted through the power lines, there is the question of radiation from the circuit itself. This can be minimized by keeping the physical size

of the current loops formed by the thyristors and the EMI filter network to a minimum. In addition to these two forms of radiation, there are also questions concerning telephone interference and acoustical noise. The uppermost curve in Figure 11.1 is for a typical unsuppressed 600 watt lamp dimmer design using thyristor switches. Notice also that a curve is given for a typical food mixer and for a noisy 40 watt fluorescent lamp. Thus it can be seen that thyristor control is not alone in producing interference in the AM band, while for FM and TV, the thyristor interference is negligible compared with the other conventional components.

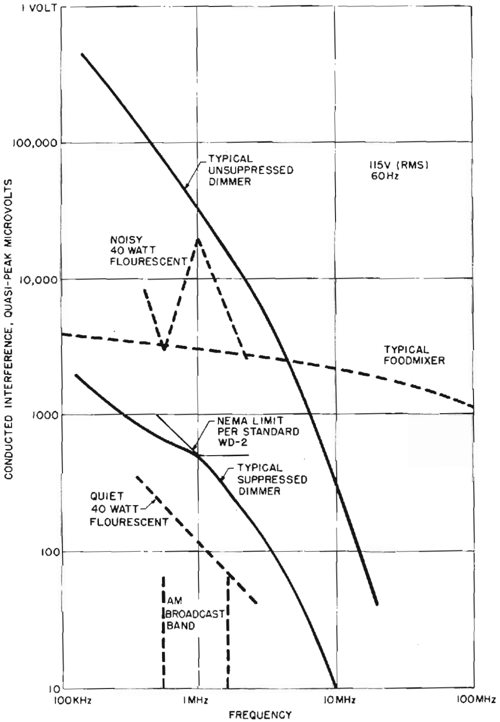


FIGURE 11.1 CONDUCTED INTERFERENCE FROM SEVERAL SOLID STATE POWER SWITCHING CIRCUITS[5]

The "suppressed" dimmer has an LC filter network to slow the rate of rise of current and absorb the higher frequencies. Chapter 17 details the design of these filters. It can be seen that the simple LC filter just manages to meet the NEMA WD-2 limit and that a single inductor would not. For large loads, these filters not only become bulky and expensive but they also will dissipate much power, and zero voltage switching becomes a more and more attractive alternative.

Figure 11.2 compares the behavior of the same LC suppressed phase control circuit with two synchronously switched circuits. At 1 MHz, the noise figure of the synchronously switched circuits is an order of magnitude lower than the filtered phase control circuit.

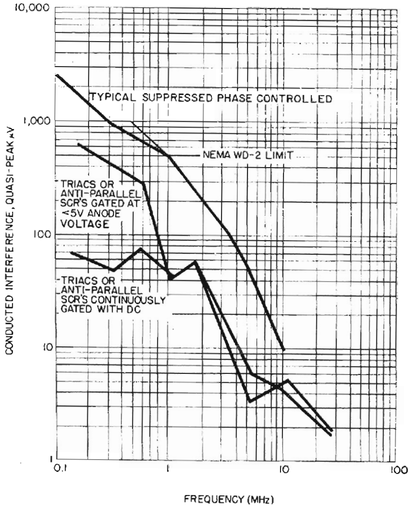


FIGURE 11.2 COMPARISON OF NOISE PERFORMANCE OF FILTERED PHASE CONTROL CIRCUIT & ZERO VOLTAGE SWITCHING CIRCUITS[5]

It is interesting to note the superior performance of the continuously gated triac circuit at the lower frequencies. The DC gating signal assures that the triac (or SCR) is always "on", that it does not unlatch at zero current due to an unsufficient holding current. The DC gating signal would have less interference than a pulsed gate signal if the pulse occurs when the anode voltage is greater than 5 volts.

Figure 11.2 also shows that the criterion to meet the NEMA WD-2 interference limit is that the triac or SCR must be turned on before the line voltage rises above 5 volts. Table 11.1 shows the times and angles for 5 volts for different voltages and frequencies.

	Voltage (RMS)					
	24		115		220	
Frequency (Hz)	Θ(°)	T (μsec)	Θ	T	Θ	T
50	8.47	471	1.76	97.9	.92	51.2
60	8.47	392	1.76	81.6	.92	42.6
400	8.47	58.8	1.76	12.2	.92	6.4

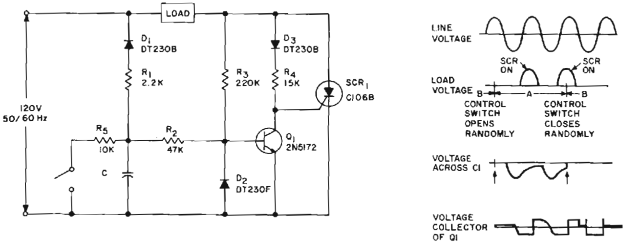
TABLE 11.1 THIS TABLE SHOWS THE ANGLE AND THE TIME AT WHICH POINT THE POWER VOLTAGE EXCEEDS 5 VOLTS

11.3 DISCRETE ZERO VOLTAGE SWITCHING CIRCUITS

Discrete zero voltage triggering circuits abound so that the intent of this section is to show some of the more typical ones, how they work, what they can do, their limitations, etc. The important idea is to ensure that the thyristor turns on before the instantaneous voltage across it exceeds 5 volts in order to meet the NEMA WD-2 EMI limits.

11.3.1 Basic Switching Circuit

The circuit shown in Figure 11.3 accomplishes ideal switching for a half-wave circuit.[6] Other variations (including full wave) will be discussed later.



(a) Ideal Half Wave Switching Circuit

(b) Associated Voltage Half-Wave Forms

FIGURE 11.3 HALF WAVE ZERO VOLTAGE SWITCHING CIRCUIT

When transistor Q_1 is cut off, positive anode voltage on SCR_1 causes gate current to flow through D_3 and R_4, triggering SCR_1 into conduction. When transistor Q_1 is biased into conduction, current through R_4 is shunted away from the gate of SCR_1 through the collector of Q_1.

The contacts of switch S_1 (or the value of resistance connected across its contacts) control the conduction state of Q_1. With the contacts open, the negative half-cycle of the supply charges capacitor C_1 to the peak of the supply voltage through R_1 and D_1. As the AC supply voltage drops from its negative peak, capacitor C_1 discharges through D_2 and R_2, thus applying a cutoff bias to Q_1. This causes SCR_1 to

trigger as soon as the AC supply voltage swings positive through zero, thus providing synchronous closing. The SCR's latching characteristics maintain it in the conducting state for the remainder of the positive half cycle and open the circuit synchronously at the point where load current reaches zero naturally. Although the contacts of switch S_1 are open during the random interval A indicated in Figure 11.3(b), the SCR conducts only for complete half cycles.

If the control contacts are closed, capacitor C_1 does not charge during the negative half cycle. Q_1 is therefore driven into saturation at the beginning of the positive half cycle before SCR_1 can be triggered, and gate current is shunted away from SCR_1 for the remainder of that cycle regardless of subsequent switching of the control contacts during the positive half cycle. Also no bypass resistor (R_{GK}) is required for sensitive gate SCR's since the gate is shorted by the transistor. The following design criteria must be followed for the circuit of Figure 11.3(a):

1) The resistance of R_4 must be less than the line voltage at which switching should occur (typically 3 to 5 volts) divided by the maximum gate current required to trigger the SCR. This latter requirement highlights the desirability of an SCR with sensitive gate triggering characteristics.

$$R_4 = \frac{3\text{ V}}{I_{gt}} = \frac{3\text{ V}}{200\ \mu\text{a}} \approx 15\text{ K}\,\Omega$$

The lower limit of R_4 is determined by the collector current limit of Q1.

2) R_3 in turn must provide sufficient base drive to Q_1 to keep Q_1 in saturation throughout the cycle when C_1 is in the discharged state. Using 15 as a conservative figure for the current gain of the 2N5172:

$$R_3 = 15 \cdot R_4 \approx 220\text{ K}$$

3) R_2 should be substantially less than R_3. Pick

$$R_2 = 47\text{ K}\,\Omega$$

4) The time constant of R_2C_1 must be sufficient to extend bias current for Q_1 into the positive half cycle, and hence should be approximately ½f. For 60 Hz:

$$R_2C_1 = 8.3\text{ msec}$$

$$C_1 = \frac{8.3\text{ msec}}{47\text{ K}} \approx .2\ \mu\text{f}$$

5) Resistor R_5, which limits the capacitor discharge current through the contacts when S_1 is closed, must be low compared to R_1. This will prevent C_1 from charging when the control contacts are closed.

Pick $R_5 = 10$ K

11.3.2 Two Transistor Switching Circuit

Figure 11.4 is an extension of Figure 11.3 in that Q_1 along with S provides the gating signal while Q_2 detects the zero voltage crossing. Switch S could be connected between base and emitter of Q_1 to provide inverse logic, i.e., SCR_1 off with S closed.

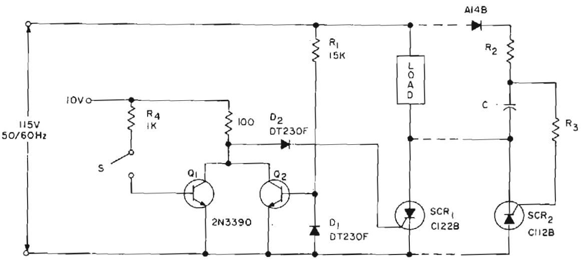


FIGURE 11.4 TWO TRANSISTOR ZERO VOLTAGE SWITCHING CIRCUIT. DOTTED PORTION AT RIGHT FOR INTEGRAL CYCLE CONTROL

Diodes D_1 and D_2 perform the same function as D_2 and D_4 of Figure 11.3, namely protection of low voltage components during the negative half cycle. The forward junction voltage drop of D_2 ensures that SCR_1 is not triggered on while either Q_1 or Q_2 are on.

The same rule applies to specify R_1 as shown in Step 2 of Section 11.2. Again the lower limit of R_1 is determined by the allowable base current of Q_2. The use of darlington transistors for Q_1 and Q_2 would allow larger values for R_1 and R_4 but this would also necessitate an additional diode in the gate circuit to compensate for the higher saturation voltage of this type of transistor.

The dotted in connections are for integral cycle control. SCR_2 is slaved to SCR_1 by R_2, R_3 and C (see Section 8.3). The elimination of any possible half-waving prevents saturation effects even in critical elements like transformers having marginally designed magnetic cores.

11.3.3 CSCR Zero Voltage Switch

Another useful zero voltage switch can be easily assembled using a complementary or n-gate SCR, such as the C13Y. If switch S of Figure 11.5 is closed, the C13Y can be turned on by gate current flow through resistors R_1, R_2 and diode D_1. However, as soon as the line voltage rises above 5 volts, diode D_1 becomes reversed bias and the C13Y can no longer turn-on. Since the gate of the C13Y is sampling the SCR anode voltage, this circuit may be used with any load power factor. Resistor R_3 should be chosen so that the leakage current through D_1 does not damage the gate of the C13Y.

$$R_3 < \frac{V_{GRM} + 5\ V}{I_R} \qquad (11.1)$$

where: V_{GRM} = C13Y gate avalanche voltage, typically 5 volts

I_R = reverse leakage current of D_1.

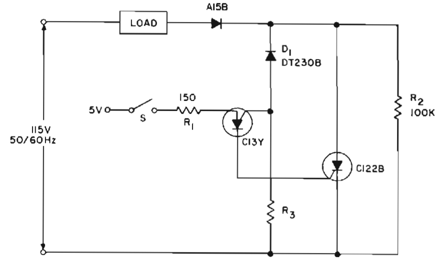


FIGURE 11.5 CSCR ZERO VOLTAGE SWITCHING CIRCUIT

This circuit is easily scaled up for 220 volt operation.

11.3.4 Triac Zero Voltage Switching Circuits

In Figure 11.6, the triac will be gated on at the start of the positive half cycle by current flow through the 3 μf capacitor as long as the C103 SCR is off. The load voltage then charges up the 1 μf capacitor so that the triac will again be energized during the subsequent negative half cycle of line voltage. Note that a selected gate triac will be required because of the III+ triggering mode (see Chapter 7.)

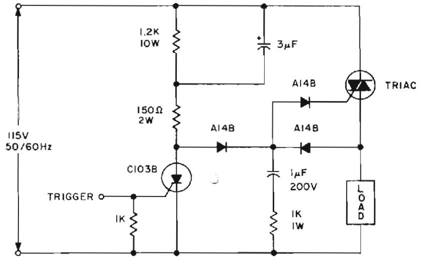


FIGURE 11.6 TRIAC ZERO VOLTAGE SWITCH

Zero point switching is assured by the SCR. A change state of the C103 from "off" to "on" during the positive half-cycle will have no effect on the triac since it will already be latched on. Furthermore, if the C103 is turned on at the start of the cycle, the triac cannot be triggered at any time during that cycle since the C103 will say on until reverse biased.

The major difficulty encountered with this circuit involves triggering the triac during the positive half cycle. Because of the high gating current requirements of the triac, line voltage often reaches 10-15 volts before the triac fires. Larger capacitors and smaller resistances would advance this firing angle but would also increase the power dissipation in the gate, in the C103 and in the components themselves.

11.3.5 Improved Zero Voltage Triac Switches

Since the problem of triggering the triac early in the cycle occurs only for the positive half-cycle (the 1 μf capacitor applies DC to the gate of the triac during the next zero voltage crossing so that the triac does not commutate off), one solution is pilot triggering with a sensitive gate SCR.

In Figure 11.7, the pilot C106 SCR is turned on very shortly after the voltage starts to rise by R_1 assuming the C103 SCR is off, which in turn triggers the triac. Negative half cycle triggering occurs as before. The maximum voltage to trigger the C106B is:

$$V_M = I_{GT(max)} \cdot R_1 + 4 \cdot V_F$$

where V_F = PN junction drops

$$\approx (200\ \mu a)(10\ K) + (4)(.6\ V)$$
$$= 4.4\ V$$

Diode D_1 is required in order to prevent the 1 μf capacitor from charging negatively during the negative half cycle when the triac is on. If it does, it triggers the pilot SCR when the C103 has just turned on.

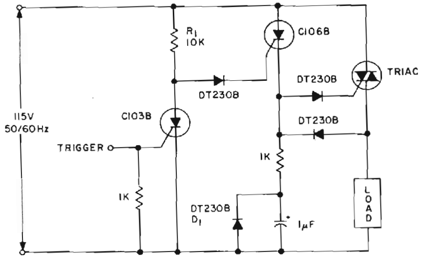


FIGURE 11.7 IMPROVED ZERO VOLTAGE TRIAC SWITCHING CIRCUIT

Both the circuits of Figures 11.6 and 11.7 require selected gate triacs. Figure 11.8 allows the use of the standard type since the gate modes are now I−, III−, i.e., negative gate triggering.

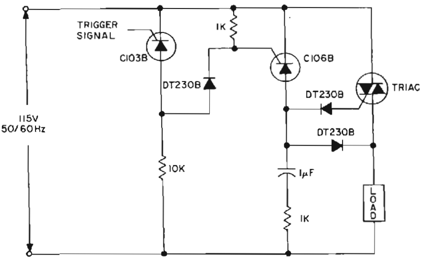


FIGURE 11.8 ZERO VOLTAGE TRIAC CIRCUIT USING STANDARD TYPE TRIACS

11.3.6 Transistorized Zero Voltage Trigger

Figure 11.9 shows a zero voltage triggering circuit that also includes its own regulated power supply. The circuit operation is as follows:

1) The power supply capacitor C_1 is charged up to the zener voltage of D_6 through diode D_5 and R_2, typically 6-7 volts.

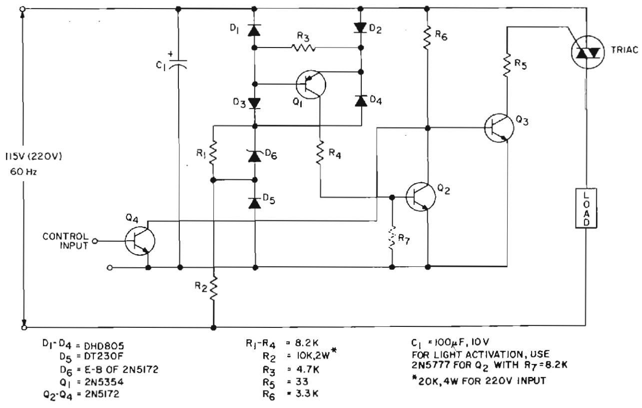


FIGURE 11.9 TRANSISTORIZED ZERO VOLTAGE SWITCH

2) Transistor Q_3 supplies the triac triggering current (negative gate drive) from the capacitor via R_5. Command signals to trigger the triac can be inputed at the base of Q_3.
3) Transistor Q_1, steering diodes D_1 – D_4 and resistors R_1 and R_2 constitute the zero voltage detector. When the line voltage has risen 3-5 volts positively, current through diodes D_2, D_3, R_2 and R_3 turn on Q_1, which in turn saturates Q_2 and thereby inhibits further gate drive. During the negative half cycle, diodes D_1 and D_4 would conduct.

The triac triggering pulse will be about 100 microseconds long for 115, 60 Hz operation and will be centered around the zero voltage crossing point. Therefore the latching current available at the end of this pulse determines the minimum load that can be successfully controlled.

Operation of all these circuits (plus those to follow) on 50-400 Hz is no problem, although a specially selected triac would be required for 400 Hz supplies. All of the discrete elements respond fast enough so that the decision to trigger the power semiconductor is made before the supply voltage exceeds 5 volts.

11.4 USE OF THE GEL300 — A MONOLITHIC ZERO VOLTAGE SWITCH

The GEL300 is primarily a combination trigger circuit and threshold detector to provide zero voltage switching control of resistance loads when used with thyristors such as triacs or SCR's. This circuit provides a differential input stage, designed to sense resistance bridges, with enough connections brought out to provide a wide variety of useful connections. Output of this device can be adapted to provide minimum RFI temperature control or to drive small relays or lamps.

Figure 11.10 shows the schematic of the GEL300. It is obvious

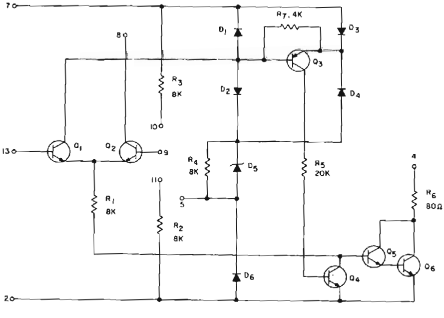


FIGURE 11.10 CIRCUIT DIAGRAM OF THE GEL300 IC OFFERED IN A 14 PIN DIP. NUMBERS REFER TO PIN CONNECTIONS

that the main differences between this figure and Figure 11.9 is the addition of an input stage consisting of transistors Q_1 and Q_2 connected in a differential amplifier configuration and a balanced resistor pair (R_1 and R_2), which can be used as one side of a resistance bridge. The circuit is so designed so that when Q_1 is conducting, its collector current inhibits all output from the circuit (Q_5 and Q_6). Otherwise, the IC behaves exactly as explained before and the same precautions concerning triac selection hold true (see also Chapter 12 for more details concerning the use of the GEL300 in heating control circuits, in low power circuits, staging heaters, sensors, etc.

11.4.1 Output and Power Connections

There is a wide variety of input and output connections for the GEL300. The basic AC connection for triggering a triac is shown in Figure 11.11. This figure is also the schematic (less R_a and R_b), of the power control (S200) module available from GE.

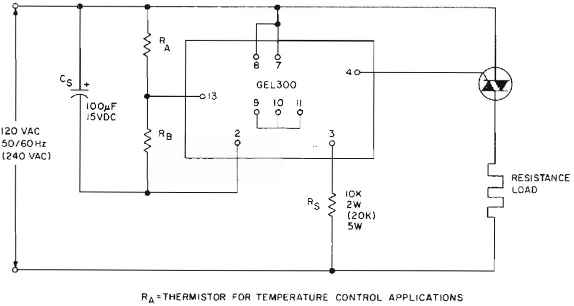


FIGURE 11.11 BASIC POWER CONTROL CONNECTION

If it is necessary to control a pair of SCR's, the connection of Figure 11.12(a) could be used. In this connection, the SCR's are driven by means of the pulse transformer T_1. Since the GEL300 output pulse is quite long, and normally starts before line zero crossing, it is necessary to shift the pulse so that the output of the pulse transformer occurs at the proper time for triggering. This may best be accomplished by advancing the pulse from the GEL300 with a leading network as shown in the same figure. The output pulse to the SCR is taken from the pulse that is generated from stored energy when the pulse in the primary stops. This circuit scheme might also be used where isolation between the line and the firing circuit is required. To provide a completely isolated low voltage control circuit, isolation transformer T_2 can be added. T_2 need only supply about 15 mA at 24 VAC.

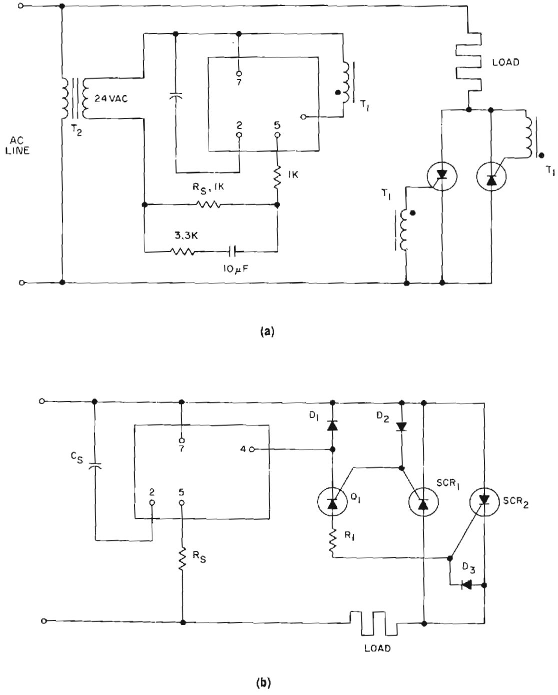


FIGURE 11.12 SCR TRIGGERING CONNECTIONS

Figure 11.12(b) uses on SCR connected as a remote base symmetrical transistor, Q_1, to provide triggering for other SCR's. Q_1 is a low current SCR such as a C5 or a C106 of sufficient voltage rating for the line voltage used. The output current from the GEL300 provides the negative base drive required by Q_1 for both half cycles. Gate current for each SCR flows from either D_2 or D_3, through R_1 and Q_1 to the gate of the required SCR. Diode D_1 is to protect the GEL300 in the event of Q_1 firing as a normal SCR due to a transient.

Since the output of the IC is limited plus the fact that the current gain of the symmetrical transistor is so low, other means must be found to trigger large SCR's.

11.4.2 Mating the IC to the High Current SCR

The circuits shown in Figure 11.13 show various ways of amplifying the IC output to a high enough level to guarantee a positive turn-on of most any high current SCR. Since the GEL300 circuit was designed specifically to trigger triacs, it is desirable to use a triac as a pilot SCR wherever circuit voltage will allow its use, as shown in Figure 11.13(c). Figure 11.13(a) shows a useful technique for firing a pilot SCR from a negative current source as is available from the GEL300. The diodes D_1 and D_2 are needed to prevent excessive voltages from being developed across the IC when initially turning on SCR_1 and SCR_2. Figure 11.13(b) provides positive slave firing of SCR_1 by means of the PUT. R_5 and C_2 may be adjusted to have the charge stored in capacitor C_1 dumped into the gate of SCR_1 anytime before, during or immediately after the cessation of current in SCR_2. This circuit does away with many of the disadvantages associated with slave firing circuits having only passive components.

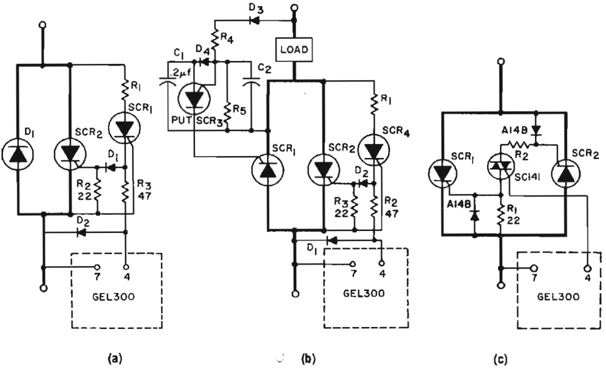


FIGURE 11.13 HIGH CURRENT SCR GATE CIRCUITS TRIGGERED FROM THE GEL300

11.4.3 Connections for the Input Section

The basic connection of the input section as shown in Figure 11.14 is the direct comparison of a resistance bridge, using the internal resistors as one side of the bridge. R_A and R_B should be no lower than 5000 ohms in value to prevent undue loading when using the internally generated supply. The highest value of R_A and R_B may be determined by the inhibit current (5 μA max) and the allowable error in the application. Obviously the next step could be to use both sides of the differential stage in an external bridge or to compare two external DC levels. For temperature control applications, R_A is usually a negative temperature coefficient thermistor.

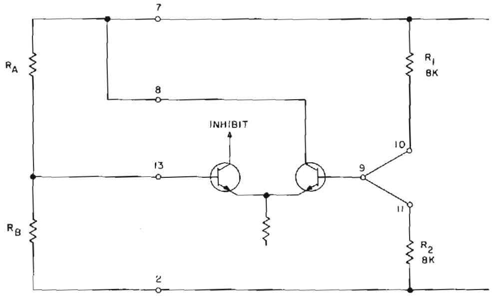


FIGURE 11.14 BASIC BRIDGE CONNECTION FOR THE DIFFERENTIAL INPUT STAGE

The collector of Q_2 (pin 8) can be used to generate a signal which indicates the state of the input stage. If Q_2 is on, and drawing collector current, then Q_1 is off and the circuit is supplying output. This collector current can be sampled by a resistor (from 2 to 10 K ohm) to give a voltage signal.

Chapter 12 includes more design ideas such as proportional control, staging of heaters to minimize light dimming, multiple triac triggering and others.

11.5 ZERO VOLTAGE SWITCHING AT HIGH FREQUENCIES

Many of the disadvantages of zero voltage switching at 50/60 Hz disappear as the power frequency increases. These disadvantages include:

1) Temperature excursions on small load heating systems. Since the smallest increment of energy that can be applied is 1 or ½ of a cycle, the temperature excursion may be excessive for heater loads with small thermal mass. Thermal mass could decrease inversely with frequency because energy absorbed is proportional to time.
2) Lamp dimming. Zero voltage switching control of lamp intensity is not possible because of excessive flicker at low light levels. Assuming that the eye is sensitive to any event that occurs less than 16 times a second, then at a 60 Hz, lamp intensity can only be lowered to ¼ brightness (1 pulse out of every 4). However at 400 Hz, the lamp could easily be dimmed to 1/20 of its full intensity (1 pulse out of every 20). Therefore the solid state high frequency lamp dimmer combines all the advantages of solid state with very low EMI operation, especially critical on airplanes.

3) Motor speed control. Zero voltage switching of motors suffers the same disadvantages of (1) above, namely excessive bursts of speed for low inertia loads. Therefore, one would except the same improvement here at high frequencies as in (1) above.

11.6 THREE PHASE ZERO VOLTAGE SWITCHING POWER CONTROL

Figure 11.15 shows the GEL300 inside the phases of a three phase delta connected load. This circuit is a straightforward extension of the GEL 300 used in single phase circuits of Section 11.4.1. It is applicable to resistive or reactive loads by means of the circuit modifications shown. Control may be accomplished in two distinctly different ways. The first method would involve three separate thermistors as shown, each controlling one-third of the load. A separate type of control could be accomplished by the use of a central control technique shown in Figure 11.17 discussed later, which would synchronize all three load legs with one central sensor.

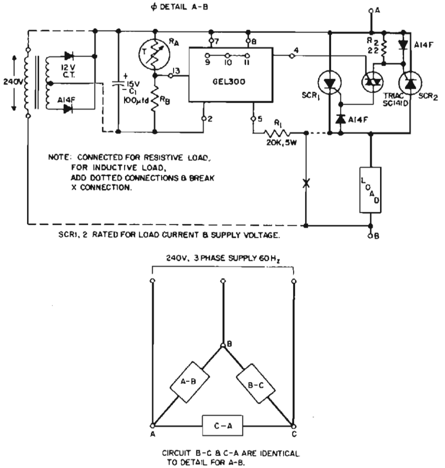


FIGURE 11.15 THREE PHASE ZERO VOLTAGE SWITCHING CIRCUIT CONTROLLING PHASE CURRENTS OF DELTA CONNECTED LOAD

The power control circuit of Figure 11.16 shows the use of the GEL300 controlling line current of a delta or wye connected load. R_5 is used to establish an artificial neutral in conjunction with C_2 which stabilizes the neutral such that it departs from zero voltage by less than 4 volts p.p. on a 240 volt line. C_2 also provides a slight phase lag to the GEL300 which guarantees that its narrow output pulse will properly trigger SCR_1.

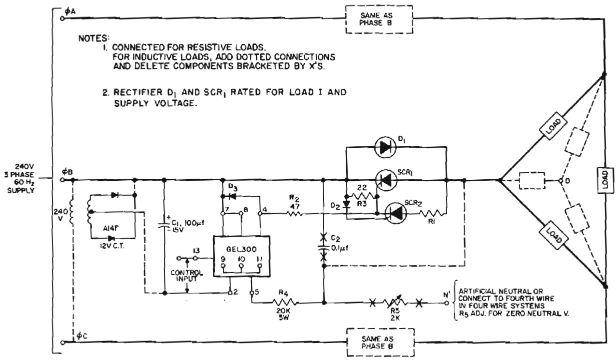


FIGURE 11.16 THREE PHASE ZERO VOLTAGE SWITCHING CIRCUIT CONTROLLING LINE CURRENT

If the load is inductive or is resistive and unbalanced, the changes shown for inductive loads must be made. Point "O" may be connected to a neutral in a four wire system only if D_1 is replaced with an SCR and the gating circuit is appropriately modified as for example in Figure 11.12(b).

A central or master control can be provided for three isolated GEL300's by means of L14 photo darlingtons as shown in Figure 11.17. The GEL230 is used as a high gain differential amplifier to drive the GEL300 fully into or out of their respective inhibit ranges by means of the light source. The circuit can be adapted to provide proportional control in the same manner as that provided for single phase application of the GEL300. This is accomplished by adding a sawtooth voltage to the input of the GEL230 (see Section 12.5.3).

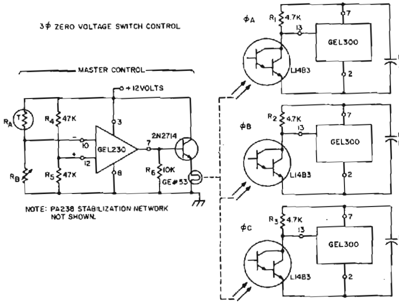


FIGURE 11.17 THREE PHASE ZERO VOLTAGE SWITCH MASTER CONTROL CIRCUIT

REFERENCES

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2. F. W. Gutzwiller and J. H. Galloway, "Power Grab by Linear IC's," Electronics, August 21, 1967, pp. 81-86.
3. E. K. Howell, "Practical Considerations of Solid State Electric Heating Controls," IEEE Conference Record of 1969 Industrial and Commercial Power Systems and Electric Space Heating and Air Conditioning Joint Technical Conference.
4. "Noise Effects in Control Systems," Machine Design, December 19, 1968, pp. 146-156.
5. H. A. Gauper, et al, "The Special Problems of Power Semiconductors Presented to Power Sources," – to be published.
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NOTES

12 SOLID STATE TEMPERATURE & AIR CONDITIONING CONTROL

12.1 INTRODUCTION

Solid state temperature controllers have revolutionized temperature regulation. These controllers feature mechanical ruggedness, high reliability, precise temperature control, multifunction operation, light weight and both silent mechanical and electrical (EMI-less) operation. The circuits described have been designed into electric heating, room conditioning, range oven and burner controls, ovens in general, portable appliances such as hair dryers and light industrial control applications. The temperature sensing elements are either negative temperature coefficient (NTC) thermistors or positive temperature coefficient (PTC) sensors such as thermistors, nickel wire, tungsten, platinum, etc. It is to be expected that new, low cost sensors for humidity and pressure will be incorporated as these transducers become available. Then the controller will become more economical on a function basis than the mechanical relays it replaces.

12.2 HOW TO SELECT THE PROPER CONTROL

There are many different types of temperature controls available, ranging from a very simple bimetallic relay to a very elaborate, proportional control, zero voltage switching electronic system. The design engineer is forced to adopt a systems approach in order to select intelligently the right control. The steps involved are:

1. To obtain a sound understanding of the thermal characteristics of the system to be controlled.

2. To prepare a well-defined specification of control system performance characteristics.

3. To recognize the limitations of the various control vircuits available.

4. Fitting the control to the system.

The basic functions which must be performed in a solid-state electric heat control are shown in Figure 12.1. The comparator decides whether or not to apply power to the chamber after comparing the chamber temperature to the set point temperature. The different elements in this system are considered below and finally different circuits are presented which fulfill the requirements of the system specifications.

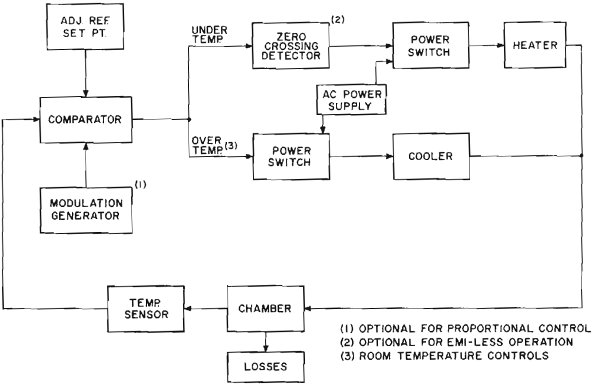
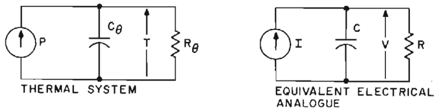


FIGURE 12.1 TEMPERATURE CONTROL BLOCK DIAGRAM WITH THERMAL FEEDBACK

12.2.1 Thermal System Model

The thermal characteristics of the system (chamber, heater and/or cooler, and losses) can be subdivided into two broad categories – steady state and transient. At steady state, the average temperature rise of the controlled environment depends upon its thermal resistance and the power input. The temperature gradient between the controlled space and the temperature sensor can also be important. Heating and cooling follow exponential curves so that if full power is required to maintain a set temperature, the time to reach this temperature is theoretically infinitely long. Therefore, to decrease the response time of the system requires an increase in available power and its pursuant oscillation. This naturally leads to transient analysis.

The model for most heating systems consists of a distributed network of thermal resistances and capacitances with one or more power sources. An exact electrical analogue exists (shown in Figure 12.2) so that if the different thermal resistances and capacitances are known, then the whole system may be easily simulated on an analog or digital computer. One can now predict the amount of overshoot or undershoot of temperature to a step input of heating or cooling power, the setting time, off-set, etc. The last link to close the loop on this network is the power controller.



EQUIVALENT NOMENCLATURE

HEAT	ELECTRICITY
T (TEMPERATURE)-°C	V (VOLTAGE)-VOLTS
P (POWER)-WATTS	I (CURRENT)-AMPERES
C_θ (THERMAL CAPACITANCE)-JOULES/°C	C (CAPACITANCE)-FARADS
R_θ (THERMAL RESISTANCE)-°C/WATT	R (RESISTANCE)-OHMS

MATHEMATICAL RELATIONSHIPS

$T = R_\theta \cdot P$ $\qquad V = I \cdot R$

$dT/dt = P/C_\theta$ $\qquad dv/dt = I/C$

FIGURE 12.2 ELECTRICAL ANALOGUE TO HEAT

12.2.2 Elements of Feedback Control

The control of temperature requires a closed loop feedback control system in which the regulated temperature is sensed, compared with a reference (set point), and a decision made as to whether power input should be changed. In the elementary, ideal thermostat, the switch is closed at any temperature below set-point, and open at any temperature above set-point. The chamber temperature must fluctuate above and below the set-point, shown in Figure 12.3, in order to establish an average input power. These fluctuations can be quite excessive in heating systems because of long thermal time-constants of the chamber, heater, and thermostat, and because of transport delays.

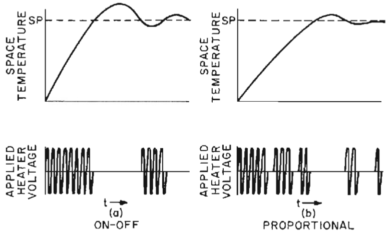


FIGURE 12.3 MODES OF CONTROL

Good temperature control, with small fluctuations, can be achieved by properly controlling average input power in proportion to the error or difference between chamber temperature and set-point, as in Figure 12.3(b). It has been shown[1] that a well designed proportional control can maintain room temperature within small fluctuations of 1°C over the full range of heat loading, without fluctuations so that an order of magnitude better control can be achieved in a smaller, better insulated system.

Since the control of electric heat is a closed-loop feedback control system, the essential elements and characteristics of closed-loop systems need to be examined. The accuracy and stability of a feedback-control system are determined by the factors of system gain and phase-shift or delay.

The open-loop system gain can be defined as the possible change in room temperature per degree change in sensed temperature. For example, in a heating system which, at full power, will just maintain 24°C (75°F) space temperature at −37°C (−35°F) outside temperature and with a proportional thermostat which provides full power when space temperature is five degrees below set-point (and zero power when space temperature is equal to set-point), the system gain is (24 − (−37))/5 or 12.2. In general, higher gain produces more accurate temperature control but also tends to become unstable in the presence of slow thermal responses and transport delays in the system.(2) The temperature fluctuations caused by the elementary ideal thermostat are system oscillations resulting from the virtually infinite gain of such a system. The practical elementary thermostat switches on at one temperature and off at a slightly higher temperature. This differential causes even wider temperature fluctuations to occur, hence should be kept as small as possible. Sensor differential cannot be eliminated completely in mechanical thermostats since it is both inherent and necessary for proper operation and contact life. A small differential would mean many operations and thus rapidly wear out the thermostat.

12.2.3 Phase Shifts

Time is another important factor in system stability. Thermal storage capacity of the heating system, thermal time-constants, and cycling rate are the time-dependent variables which contribute to thermal phase shifts in the system. The response time of the control system should be short compared with the thermal system time-constants. It was found long ago that adding an "anticipation" heater to the thermostat improved system performance. This "anticipation" actually produces proportional control by forced cycling (oscillations) the thermostat itself, providing average room input power in proportion to the difference between space temperature and set-point. This alleviates the problem of excessive temperature fluctuations due to delays in heat reaching the system from the source. In a totally air conditioned system, it should be expected that both anticipation "heaters" and "coolers" would be designed into the system.

12.2.4 Proportional Control

To obtain proportional control, the heaters are switched on and off periodically. The switching repetition rate limits response time, hence must be comparatively fast. The limit on minimum repetition period is determined by characteristics of the switch and effects on the power system. Sensor time-constant must also be relatively short in

order to avoid excessive delay in the system. In other words, system gain must be less than unity at 180 degrees phase-shift. A damping factor of 0.8 is desirable for fastest response with minimum overshoot.

The number of degrees which space temperature must drop below set-point to produce full power input is defined as "droop" by industry terminology, and is also known as the proportional band. In a system which has a 5 degree linear proportional band, similar to Figure 12.4, a demand for 50% input power is met when space temperature is 2.5° below set-point. This drop in room temperature is known as "offset" and is a direct function of the proportional band. It should be noted that system gain, hence accuracy and stability, is not simply a function of the proportional band, but also depends upon maximum input power, heat losses and insulation.

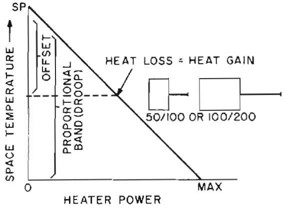


FIGURE 12.4 PROPORTIONAL CONTROL

12.2.5 Controller Specifications

Since the accuracy and stability of a feedback control system are governed by the characteristics of all components within the system, it is not possible to completely specify system performance by defining the control elements alone. However, based upon experience in residential heating tests,(1) results indicate that it may be possible to prescribe control element characteristics which can generally provide acceptable system performance. The four parameters are:

1. Proportional band
2. Switching period
3. Sensor Time Constant
4. Differential

To provide the above characteristics mechanically would be extremely difficult, but they can be easily met with solid-state control. The solid state system includes the temperature sensing, information processing, and power switching functions.

The last remaining control specification which may have to be considered is linearity. Quite commonly it is required that the system temperature vary directly with a potentiometer setting. The problem is two-fold. Linear temperature sensors such as Ni or Pt wire are usually low impedance so that they require additional buffering or a special sensing network. Non-linear temperature sensors must be compensated with series and parallel resistances which result in loss of sensitivity.(3)

12.3 PHASE CONTROL VS ZERO VOLTAGE SWITCHING

One of the obvious advantages to solid-state power switching is the absence of a wear-out mechanism typical of mechanical switches. Since the solid-state power switch is capable of submillisecond operation, average power could be controlled by turning on for a controlled portion of each half-cycle of the ac supply, as shown in Figure 12.5(a). Phase control method of operation has traditionally enjoyed the following two main advantages:

1. The circuit is inherently proportional control and should be able to maintain a tighter differential with smaller temperature fluctuations.
2. The circuits are usually simpler and, therefore, less expensive.

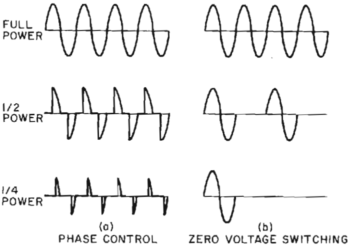


FIGURE 12.5 TYPES OF AC POWER CONTROL

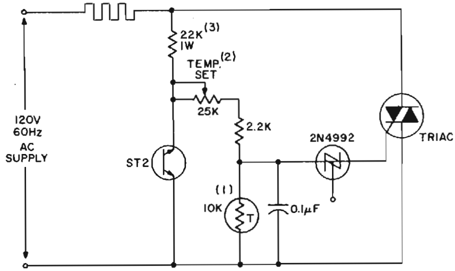
However, phase control produces high frequency components each time the switch closes and will require adequate filtering in order to hold electromagnetic interference (EMI) within acceptable limits (Chapter 17). Because such filters can become rather large and expensive and since it is anticipated that the allowed limits on EMI will decrease, phase control circuits look less and less attractive for large loads and zero voltage switching is recommended (Figure 12.5(b)).

Both phase control and zero voltage switching are covered extensively in the literature and elsewhere in this manual (Chapters 9 and 11 respectively). Therefore the discussion of the circuits will concentrate more on demonstrating what can be done to achieve low cost, adjustable gain or linear control rather than circuit operating details.

12.4 PHASE CONTROL CIRCUITS

Figure 12.6 shows the basic, full wave, phase control circuit. The circuit is economical because of few components but yet it can control up to 6 kw of heating or cooling power with moderate gain using a 400 volt, 25 amp triac (SC60D). In most phase control circuits using thermistors, heating and cooling can be interchanged by interchanging the thermistor and the reference. Another interesting feature is the use of the ST2 diac as a back-to-back zener diode. The diac has a negative resistance region in its E-I characteristic. This allows the circuit in Figure 12.6 to boast of line voltage stabilization. As the input voltage

increases, the diac voltage, and hence the charging voltage to the 0.1 μF capacitor, decreases. This phases back the conduction angle of the triac so that the load voltage is reduced. The control is obviously non-linear over a wide temperature range because of the use of the thermistor.



NOTES:
1. THERMISTOR TYPE 1D101 OF NATIONAL LEAD OR EQUIVALENT
2. REVERSE THERMISTOR AND POTENTIOMETER FOR COOLING LOAD.
3. 47K, 2W FOR 220V OPERATION.

FIGURE 12.6 BASIC, FULL-WAVE, PHASE CONTROL FEATURING VERY LOW COST

Figure 12.7 shows a higher gain version of this circuit, thereby allowing less droop. Cost increases correspondingly. The gating circuit consists of a basic PUT relaxation oscillator circuit (see Chapter 4). The conduction angle is controlled by the thermistor T. As the temperature falls, its resistance increases thereby triggering the 2N6027 earlier in the cycle.

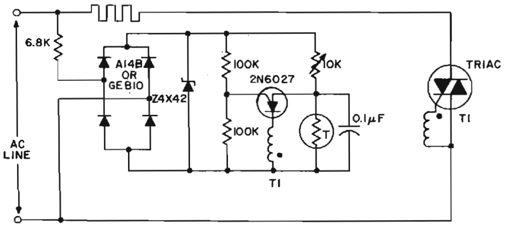
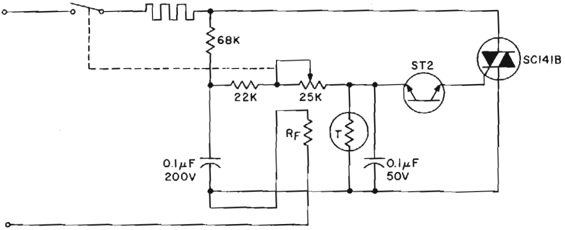


FIGURE 12.7 MODERATE COST, FULL WAVE, HIGH GAIN, PHASE CONTROL CIRCUIT

12.4.1 Remote Sensor

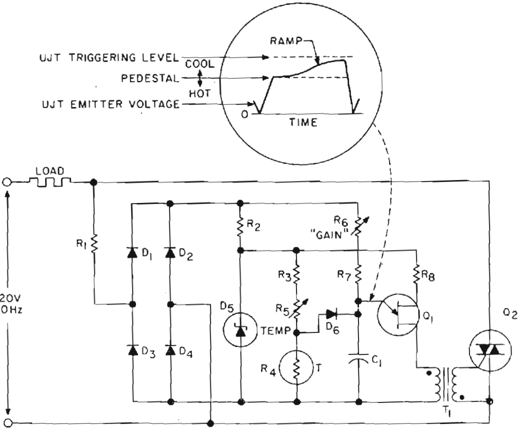
There are situations where it is inconvenient or impossible to mount the temperature sensor right in or adjacent to the temperature environment. Examples are electric blankets, vibrating systems or ones containing corrosive elements, or systems where the controller is separated from sensor which can lead to false triggering in an electrically

noisy environment. In thise case, it is necessary to go to an indirectly heated temperature sensor (see Figure 12.8). The load current flowing through R_F heats up the thermistor to achieve regulation. The selection of R_F is extremely critical and of course its temperature must somehow reflect the controlled space temperature if the system is expected to be sensitive to unexpected thermal transients.



THERMISTOR: 50K N.T.C.
R_F: FEEDBACK RESISTOR AS REQUIRED

FIGURE 12.8 TEMPERATURE CONTROLLER WITH INDIRECTLY HEATED TEMPERATURE SENSOR



R_1, R_2 = 2200 OHMS, 2 WATTS
R_3 = 2200 OHMS, 1/2 WATT
R_4 = THERMISTOR, APPROX 5,000 OHMS AT OPERATING TEMPERATURE
R_5 = 10,000 OHMS W. W. POTENTIOMETER
R_6 = 5 MEGOHM POTENTIOMETER
R_7 = 100 KΩ, 1/2W
R_8 = 1000 OHMS, 1/2W

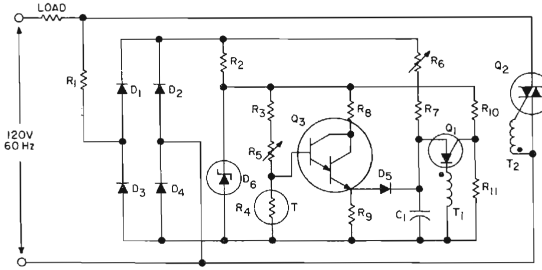
Q_1 = 2N2646
Q_2 = TRIAC AS REQUIRED
T_1 = SPRAGUE 11Z12 OR EQUIVALENT
D_{1-4} = GEA14B OR GEB102
D_5 = Z4XL22
D_6 = GEA14A
C_1 = 0.1μF, 30V

FIGURE 12.9 PRECISION PROPORTIONAL TEMPERATURE CONTROL

12.4.2 Linear Phase Control

The circuits of Figures 12.6, 12.7 and 12.8 have low control "gain" and a non-linear transfer function. In order to achieve both, one can resort to a ramp and pedestal type of control. An example is shown in Figure 12.9. A full explanation of this type of triggering circuit and the many functions that can be performed have been given in Chapter 9. Both the high gain and the linear transfer function are obtained by charging C_1 from the unclamped sinusoidal waveform. This replaces the linear ramp with a cosine ramp to compensate for the sinusoidal supply waveform. System gain can be adjusted over a wide range by changing the magnitude of charging resistor R_6. By selecting a ramp amplitude of 1 volt, for example, and assuming a zener diode of 20 volts, then a 22% change in the thermistor resistance results in the linear, full-range change in output.

To obtain a higher input impedance, an n-p-n transistor may be used as an emitter-follower as shown in Figure 12.10. If the transistor has a current gain of 100, then the values of R_3 and R_4 can be increased by two orders of magnitude, thus greatly reducing power dissipation in the sensing element R_4. In this example the 2N5306 darlington transistor was used. Also note the substitution of the 2N6027 programmable unijunction transistor in place of the 2N2646 conventional unijunction transistor.



R_1, R_2 = 2200Ω, 2W
R_3 = 22K
R_4 = THERMISTOR APPROX 50,000 OHMS AT OPERATING TEMPERATURE
R_5 = 100K W. W. POT
R_6 = 500K POT
R_7 = 100K
R_8, R_9 = 1K
R_{10}, R_{11} = 100K

C_1 = 0.25μF
Q_1 = 2N6027
Q_2 = TRIAC AS REQUIRED
Q_3 = 2N5305
T_1 = SPRAGUE 11Z12 OR EQUIVALENT
D_{1-4} = GE8102
D_5 = A14F
D_6 = Z4XL22

FIGURE 12.10 TRANSISTORIZED MODIFICATION FOR HIGH RESISTANCE THERMISTORS

Figure 12.11 employs a monolithic integrated circuit, the GEL301, phase controlling a heater load in response to a thermistor. This same circuit could be used equally as well with a fan or blower motor.

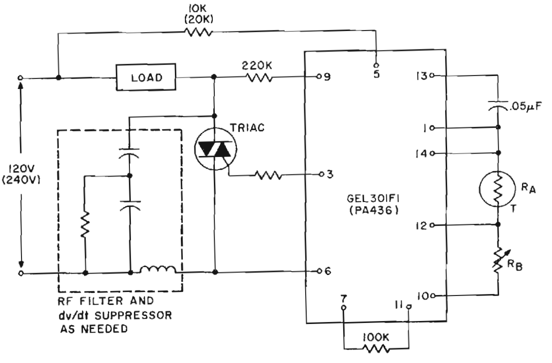


FIGURE 12.11 TEMPERATURE CONTROLLER EMPLOYING GEL301 RF FILTER NEEDED BECAUSE OF PHASE CONTROL

R_A is a thermistor having about 50,000 ohms resistance at the desired operating temperature. R_B can be made variable in order to select the temperature set point. The circuit will control the load voltage range from 0% to 100%.

Zero voltage switching control will always result in greater temperature excursions of the heating element since the minimum on-time of the latter must be full cycle. This excursion may be uncomfortable for some types of heaters, e.g., radiant heaters. In this case, phase control is the only answer.

12.5 ZERO VOLTAGE SWITCHING CIRCUITS

To achieve zero voltage switching temperature control, the control circuit must include a temperature sensor detector, a line voltage crossing detector and a gate drive circuit. For a thermistor sensor, the detector can be a simple differential amplifier which amplifies a bridge imbalance. The zero crossing detector can take several forms, one of which will be described below. The gate drive circuit can be either a pulse or a dc drive, but must appear (or begin in the case of a dc drive) at the proper time in the cycle.

12.5.1 Zero Voltage Switching With the GEL300 Integrated Circuit

To accomplish the zero voltage switching function General Electric introduced the GEL300 integrated zero voltage switching circuit in 1967. This integrated circuit accomplishes all the tasks outlined above in a single dual inline package (DIP). A functional circuit diagram for the GEL300 is shown in Figure 12.12. Also see Chapter 9 for further details.

As the line voltage goes through zero, the current through R_s also goes through zero, and if required, the GEL300 puts out a gating pulse. The pulse will be centered on the zero crossing and will end at a specified time. This time is important when triggering triacs, because it determines, along with the load current level, the latching current requirements of the triac. It is therefore important to use triacs which are tested for the proper gating and latching characteristics. Triacs are now available from General Electric especially selected for use with the GEL300. The user need only add a "12" or "22" suffix to the standard triac part number in order to obtain a triac with the proper gating and latching characteristics. (The type "22" represents an isolated stud device whereas the type "12" is non-isolated.)

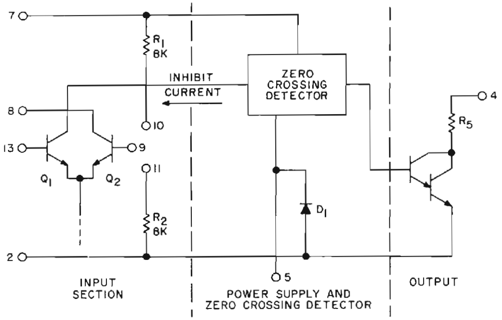
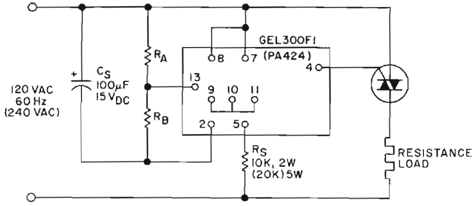


FIGURE 12.12 FUNCTIONAL DIAGRAM OF GEL300

There is a wide variety of input and output connections for the GEL300. The basic ac connection for triggering a triac is shown in Figure 12.13. This figure is also the schematic (less R_a and R_b), of the S200A power control module. This is a standard preassembled unit available in current ranges of 10 and 15 amperes for either 120, 240 or 277 volt ac supply voltages.



R_A = THERMISTOR FOR TEMPERATURE CONTROL APPLICATIONS

FIGURE 12.13 BASIC GEL300 TRIAC HEATER CONTROL

Figure 12.14 shows a connection that will utilize the GEL300 from a dc source. This operation is accomplished by opening pin 5

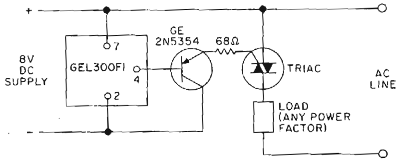


FIGURE 12.14 GEL300 CONNECTION FOR ANY POWER FACTOR LOAD

(disabling the zero crossing detector) and permitting the input section to determine the circuit output.

12.5.2 Zero Voltage Switching With an Inductive Load

In many cases where it is desirable to turn on an ac inductive load, the RF noise associated with a random triggering time is not objectionable. For this application, triggering methods shown in Figure 12.13 would not be suitable because pulses at line voltage zero crossing would not be compatible with the lagging current of an inductive load. The connection of Figure 12.14 shows the use of the GEL300 from an 8 volt dc supply to supply dc trigger current greater than 50 mA to the triac gate. With this type of triggering, the power factor of the ac load is not critical. The p-n-p transistor keeps the power dissipation in the GEL300 down to an acceptable level.

In those instances where a random triggering point for initial turn-on is objectionable, adding a resistor (R_s) as shown in Figure 12.15 will provide line synchronization of the first trigger pulse, followed by dc gate current. Whenever an inductive load is controlled, care should be taken to avoid half wave operation. This can be done by introducing a controlled hysteresis.

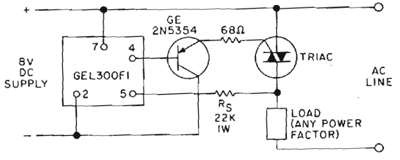


FIGURE 12.15 GEL300 CONNECTION FOR ZERO VOLTAGE SWITCHING FOR ANY POWER FACTOR LOAD

When using the GEL300 in one of the above configurations, fairly good temperature regulation will occur. Control point repeatability will be within ±0.5% of the sensor resistance, with the control point being the set point resistance ±5% (i.e., $R_A = R_B \pm 5\%$ at the control

point but for any given GEL300 this point will not vary more than 0.5% over the usable temperature range of the thermistor).

With the GEL300 most thermistors with resistances between 2.5 K and 50 K at operating temperatures can be used. It should be noted that four to five volts appear across the thermistor, so that for very small thermistors some self heating might occur. Table I lists several General Electric thermistors which have been used successfully with the GEL300.

Operating Temperature	Model Number *	Type
5°C - 25°C	1H203	Hermetic
25°C - 85°C	1H503	Hermetic
40°C - 110°C	1H104	Hermetic
80°C - 150°C	4H504	Hermetic
	81G504	Probe Type
100°C - 175°C	4H105	Hermetic
	81G105	Probe Type
160°C - 255°C	81G90510	Glass Bead

*National Lead Co., P.O. Box 420, Heights Town, N.J.

TABLE I: SOME GE THERMISTORS FOR USE WITH THE GEL300

12.5.3 Proportional Control With Zero Voltage Switching

There are cases where the on/off, zero voltage switching controls do not maintain the temperature within tight enough tolerances and phase control is objectionable. In these cases other methods must be used.

Proportional control systems are essentially the same as on/off type controls except that an anticipatory function is included. This function can take several forms, such as a modulation of the sensor through the use of an electrical or thermal signal generated independently of the feedback from the controlled system. The simplest example of such a system would be to add an auxiliary heater to a system such as the one in Figure 12.8. If this heater was controlled by the GEL300 and placed adjacent to the thermistor sensor, the sensor would heat up more quickly than normally. This in turn would cause the load power to be removed prematurely.

With some care, an auxiliary heater could be designed so that the load would be de-energized at the point in time when the stored heat energy was sufficient to permit the system to come to a stable operating point much sooner due to the lessening of the overshoots.

Because of the non-repeatability of most thermal systems, it is usually easier to implement proportional control circuits on an all solid state basis. Figure 12.16 shows such a system. In this system the modulation generator is a relaxation oscillator, using the 2N6028 Programmable Unijunction Transistor, which produces a sawtooth waveform with a 30 second period. The modulation wave is coupled into the sensor and reference circuit through the 2N3391 transistor buffer amplifier in order to get a modulation amplitude equivalent to a 1°C change in sensor temperature. With the relaxation oscillator time constant and the proportional band as shown in this system, as well as the system shown in Figure 12.17, the system will control normal room heating to within 0.5°F.

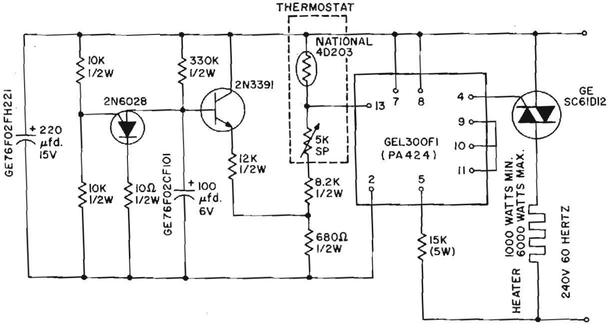


FIGURE 12.16 TYPICAL SOLID STATE SPACE TEMPERATURE CONTROL

The system of Figure 12.17 is very similar in operation to that of Figure 12.16. The primary difference is in the method of obtaining sensor modulation. In the latter the modulating current is introduced across a resistor which represents only 10% of the input bridge impedance whereas Figure 12.17 introduces the modulation directly across the reference arm of the bridge. This allows the modulating current to be decreased to one tenth of its value in Figure 12.16. This in conjunction with the use of the 2N5306 darlington transistor allows the use of a 0.47 µF capacitor to achieve the same time constant as the 100 µF gives in the former circuit. An additional advantage of the circuit of Figure 12.17 is that only two wires are required for a remote thermostat where in Figure 12.16 a three wire system is required.

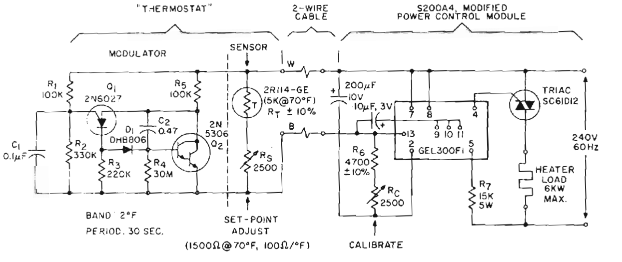


FIGURE 12.17 PROPORTIONAL CONTROL TEMPERATURE REGULATOR

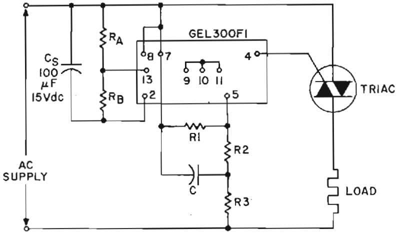
Both of these circuits are compatible with the slaving and staging circuitry, which will be discussed later.

12.5.4 Low Power Zero Voltage Switching Using the GEL300

When the GEL300 is used with a triac as a zero voltage power switch, the triac latching current is the limiting parameter. If the current through the triac does not exceed the latching current at the end of the gate pulse, the triac will return to the non-conducting state and the control will therefore not operate correctly. For this reason, the GEL300 specifications include a listing of special triacs which are tested for latching at a minimum load current of 4.2 amperes.

To allow load less than the 4.2 amperes possible with the specified triacs, the gate pulse must be shifted in time. This allows the conduction current to reach higher levels than would have been possible without the shift. A problem occurs if the pulse is shifted too far and the gate pulse does not occur until after the line voltage zero crossing. When this happens RFI is introduced into the system. To eliminate this RFI the pulse width must be extended.

The diagram and chart show how the gating pulse can be modified and the minimum loads which can be handled with each circuit.



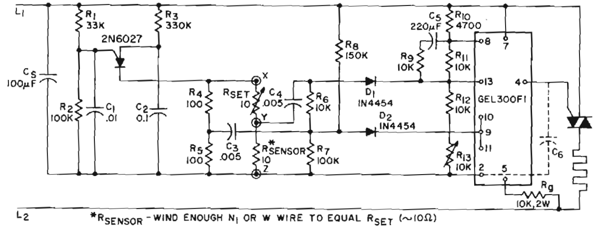
Load (watts)	R_1	R_2	R_3	C	Approx. Min. Pulse	Approx. Pulse ϕ Shift
120 VOLT SUPPLY						
500	∞	10 K	0	0	100 μsec.	0
400	∞	7.5 K	2.2 K	0.01 μfd, 200V	100 μsec.	25 μsec.
250	∞	7.5 K	2.2 K	0.022 μfd, 200 V	100 μsec.	50 μsec.
200	6.8 K	4.7 K	2.2 K	0.047 μfd, 200 V	150 μsec.	75 μsec.
240 VOLT SUPPLY						
1000	∞	20 K	0	0	100 μsec.	0
800	∞	15 K	4.7 K	0.0047 μfd, 400 V	100 μsec.	25 μsec.
500	∞	15 K	4.7 K	0.01 μfd, 400 V	100 μsec.	50 μsec.
400	6.8 K, 1/2 W	6.8 K	3.3 K	0.33 μfd, 400 V	150 μsec.	75 μsec.

FIGURE 12.18 DESIGN CHART FOR LOW POWER LOADS

12.5.5 How to Use Low Resistance Sensors

The above circuits operate extremely well with negative temperature coefficient thermistors in the impedance range of 1 K to 10 K ohms, but are unsuitable for very low impedance sensors. Most low impedance sensors are used at the higher temperatures and are normally of the positive temperature coefficient variety such as Nicrome,* tungsten and platinum. For this sensors the circuit of Figure 12.19 has been developed.

*Trademark of Driver-Harris Company



*R_{SENSOR} - WIND ENOUGH N_I OR W WIRE TO EQUAL R_{SET} (~10Ω)

NOTES:

1. ADJUST R_{13} TO MID POINT BETWEEN ON AND OFF WITH C_2 SHORTED, OSCILLATOR DISABLED.
2. PROPORTIONAL CONTROL BAND (GAIN) DETERMINED BY R_g.
3. WITH VALUES SHOWN, PROPORTIONAL BAND IS 1% R_{SENSOR} AND STROBE RATE IS 21/SECOND.
4. A PULSE TRANSFORMER CONNECTED BETWEEN (Y) AND (Z) GIVES A SENSOR ISOLATED FROM THE LINE.

FIGURE 12.19 USE OF THE GEL300 WITH A LOW RESISTANCE SENSOR

The circuit includes a 2N6027 PUT relaxation oscillator which operates at 20 pulses per second. When the PUT turns on it pulses a resistor bridge consisting of a reference divider (R_4, R_5) and the input divider (R_{set}, R_{sensor}). The dividers are coupled to the GEL300 inputs by means of a capacitor and diode combination, such that with each pulse, some charge on the capacitor is removed. The amount of charge is proportional to the divider ratio. The resistors R_8, R_7 and R_6 serve to reset the coupling capacitors between the pulses. Since each divider is connected to opposite sides of the input differential amplifier of the GEL300, the GEL300 will turn on if the R_{set}, R_{sensor} divider is unbalanced such that point Y is higher than the 50% point of the voltage between X and Z. For positive temperature coefficient sensors this is equivalent to an under temperature condition.

An interesting modification of this circuit involves isolating the sensor from the line. To accomplish isolation of the sensor, one needs only to connect a pulse transformer (such as a Sprague 11Z12 or a Pulse Engineering PE-2229) between points Y and Z. The low resistance sensor is then connected to the pulse transformer secondary to complete the circuit.

12.5.6 Multiple Triac Triggering

If more than one triac is required additional triacs can be added in the manner shown in Figure 12.20. In this circuit, the GEL304 Threshold Detector serves as a buffer amplifier between the GEL300 and the triac gates. With 50 ma I_{gt} triacs, five triacs can be driven from each GEL304. There are other advantages of this approach. The first is that by increasing R and C so that the time constant is about 10 ms, integral cycle control can be obtained. This ensures that inductive loads are switched for full cycles eliminating the possibility of saturation.

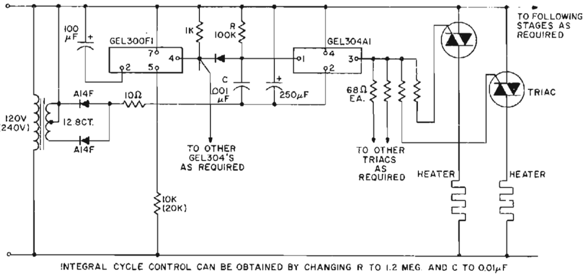


FIGURE 12.20 GEL300/GEL304 TRIGGER CIRCUIT FOR DRIVING MANY TRIACS

The second advantage is that with the widening of the pulse width triacs no longer need be selected for latching and pulse gate trigger current. Pulse widths of 200 μsec will guarantee that all triacs will be latched on by that time and the gate trigger current can be considered dc for such a wide pulse.

12.5.7 Load Staging

Many times when multiple loads are to be controlled, it is desirable to sequentially energize them. Figure 12.21 shows a method of doing this. The circuit is an extension of Figure 12.20, with the RC time constant set greater than the period of the 60 Hz line voltage so that if the GEL300 calls for load power the adjacent GEL304 will be in the on condition for at least the next full cycle.

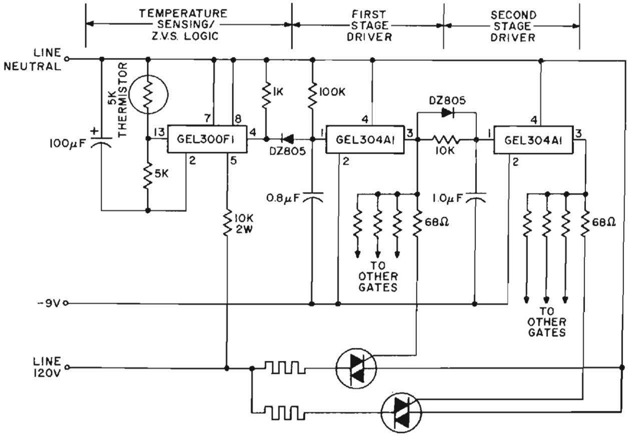


FIGURE 12.21 STAGED TEMPERATURE CONTROL

When this GEL304 is on it begins to discharge the 1.0 μF capacitor coupled to its output through the 10 megohm resistor. After 6 seconds the second GEL304 will turn on and trigger the triacs connected to its output. If the GEL300 output stops pulsing the first GEL304 will turn off resetting the 1.0 μF capacitor quickly through the bypass diode around the 10 megohm resistor. This then restarts the timing delay. By varying the 1 μF capacitor or the 10 megohm resistor delay times from one cycle to several minutes can be obtained. If this staging mechanism is used with a proportional control system, such as the one described below, one could set the delay time greater than the repetition rate of the proportioning circuit. Under this condition the staged loads would only be energized when the system is operating outside the proportional band and full power is being required.

12.5.8 Fail Safe Operation

Positive temperature coefficient sensors have an inherent advantage — *fail safe operation*. If a P.T.C. sensor is broken or opens, it appears as if an over-temperature condition exists and no power is delivered to the load. Negative temperature coefficient sensors lack this advantage; in some applications this aspect should be considered in the design. To avoid this possibility, the circuit of Figure 12.22 may be employed. In this circuit, if the sensor opens, the PUT turns on providing base drive to the transistor. The transistor then shorts the supply capacitor of the GEL300 rendering it inoperative. When the capacitor is discharged the PUT will turn off but will turn back on when the internal supply of the GEL300 attempts to recharge the capacitor. When the sensor is replaced the system will resume normal operation.

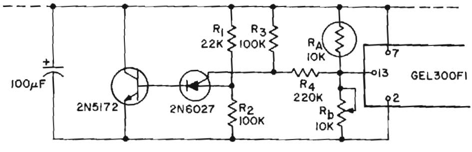


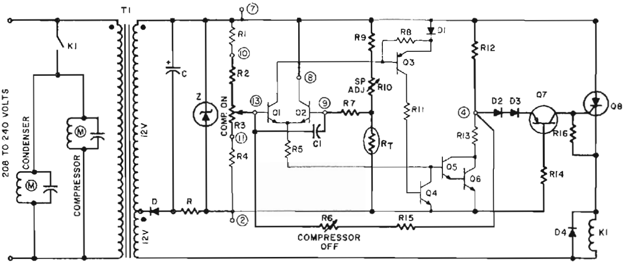
FIGURE 12.22 SENSOR OPEN DETECTOR FOR GEL300F1

12.6 AIR CONDITIONING

Up to this point, the discussion has mostly entailed electric heating with some small mention of phase control to regulate motors. However, heating is but one facet of space conditioning. Other aspects are cooling, ventilating, and heat distribution systems. In all (neglecting thermoelectric cooling), motor control plays a key role. While Chapter 10 is devoted exclusively to this subject, specialized circuits have been developed and tested[1] for these roles and should be mentioned.

12.6.1 Cooling

Most systems, with the exception of hot water, utilize a condenser and compressor to cool room air. A majority of these systems allow these cooling components to have hysteresis, i.e., the temperature at turn-off is lower than that at turn-on, reducing the number of times the cooling components operate and thus increasing their life. The mechanical method is to utilize a mechanical thermostat to turn the units on and off directly or, for the larger units, through an electromechanical relay. In a solid state system, considering the relatively high compressor surge current for the larger units (60 amps or greater), and the desire to isolate the thermostat from the line voltage, it is presently economically advisable to retain the electromechanical relay. To this end, the circuit of Figure 12.23 is a solid state replacement for a mechanical thermostat designed to control a condenser fan and compressor.



$R_1, R_4, R_5, R_8, R_{11}, R_{13}$	- IN GEL300	C	- GE 43F9723AA9 250μF 25V
R_2, R_3, R_{16}	- 1K ohm	C_1	- GE 75F1R5A103 .01μF 50V
R_6	- 5 megohm	D_1	- IN GEL300
R_7	- 12K ohm	D, D_2, D_3, D_4	- GE 414F
R_9	- 3.3K ohm	Q_1 thru Q_6	- IN GEL300
R_{10}	- 5K ohm	Q_7	- 2N5354
R_{12}	- 2.2K ohm	Q_8	- GE C106F
R_{14}	- 82K ohm	Z	- GE 24XL12
R_{15}	- 220K ohm	K_1	- 24V COIL, CONTACTS AS REQ.
R_T	- GE 2R114	T_1	220V PRI; 24V CT. SEC.; 25 WATT
R	- 120 ohm		

NOTE:
ALL RESISTORS 1/2W ±10% UNLESS OTHERWISE NOTED.

FIGURE 12.23 COOLING COMPRESSOR AND CONDENSER CONTROL

The condenser fan and compressor are energized by Q_8 through relay K_1. Q_8 is turned on simultaneously with Q_7. Consequently it remains to turn on Q_7 whenever room cooling is required.

The GEL300, used here as a level detector with hysteresis, is utilized to control Q_7 and consequently the condenser fan and compressor. Note that the GEL300, shown in thin line, is used in the DC mode only and does not utilize the AC synchronization components internally connected to its pin 5. That is, Q_5 and Q_6 will be off and Q_7 on through R_{12}, D_2, D_3, Q_8 and relay K_1, regardless of the AC power signal, if Q_1 is on as dictated by the thermostat components. Therefore, when the room temperature is high, Q_1 is on, Q_5 and Q_6 are off, Q_7 is on, and power is applied to the condenser fan and compressor. At this time

R_6, R_{15} and R_{12} are across R_1, R_2 and part of R_3. As the room temperature decreases, the increasing resistance of R_T will overcome Q_1 and turn on Q_2, Q_5 and Q_6, removing power from the cooling components, allowing room temperature to increase. Note that R_6, R_{15} and R_{13} are now across R_4 and part of R_3. The changing position of R_6 and R_{15} introduces hysteresis and requires the room temperature to increase somewhat before the resistance of R_T reduces sufficiently to allow Q_1 to conduct and ultimately re-energize the cooling components. The hysteresis of this control is adjustable from approximately 0.25°F to 4°F by R_6.

R_7 isolates the thermostat from Q_2 interference and C_1 eliminates erratic relay closure due to noise. The circuit was designed to be operated with mechanical overload protection to prevent rapid, continuous compressor current surges. However, if desirable, this feature could be accomplished electronically.

12.6.2 Ventilating

A proportional motor control which varies the speed of a ventilating fan or blower in response to a heating or cooling requirement, aids in reducing room temperature variations, drafts, noise and variation in noise.[(3)] These advantages have been well known in the room conditioning industry but were not economically feasible until the arrival of solid state. Since a ventilating motor does not usually require the high current capability of inverse parallel SCR's, a triac power switching component is generally used. The triggering circuits may be simple or sophisticated, depending upon the accuracy desired. The thermistor thermostat is similar to that used for heating or cooling, however, it may not be located within the room, e.g., it may be located within a heated or cooled chamber.

In the customary electromechanical furnace central heating system (oil, gas, etc.), the room thermostat controls the action of the burner and a second thermostat, mounted in the bonnet, controls the action of the blower. When the room thermostat calls for heat, the burner is energized and bonnet temperature begins to rise. When bonnet temperature reaches a predetermined high-temperature limit, the blower is energized to circulate the heated air. When the room thermostat is satisfied and de-energizes the burner, the blower continues to run until the bonnet temperature drops below a given low temperature limit, at which point the blower is turned off. This on-off cyclic action results in room temperature variations that are beyond the control capability of the room thermostat.[(4)]

Figure 12.24 shows General Electric's S100E solid state speed control assembly for the furnace blower that replaces the bonnet thermostat with a thermistor. This assembly provides continuous control of blower speed in response to bonnet temperature. It also limits the minimum speed at which the motor can run which protects the bear-

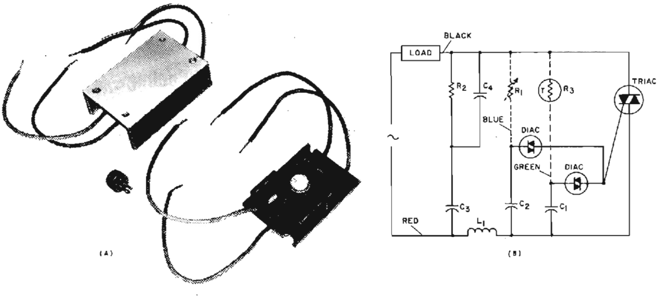


FIGURE 12.24 FURNACE BLOWER MOTOR SPEED CONTROL

ings, and maintains a gentle circulation of air through the heating system. When the room thermostat energizes the burner, the blower speed will increase gradually as bonnet temperature increases. Heat is thereby distributed to the house as soon as it is available from the burner and the thermostat then has the opportunity to turn off the burner long before the full capacity of the system is reached. The effect greatly reduces the temperature excursions that can be experienced in mild weather. Under these mild heating load conditions, the blower may never reach full speed in order to maintain the proper temperature of the house. Conversely, in severe weather, the blower may never reach minimum speed because of the high demand for heat. The control is capable of controlling up to 10 amperes on a 230 volt line. It is contained in approximately a 1″ x 2″ x 3″ metal housing equipped with pigtail leads, as shown in Figure 12.24, to which are connected the user's supply voltage, motor load, thermistor T and potentiometer R_1.

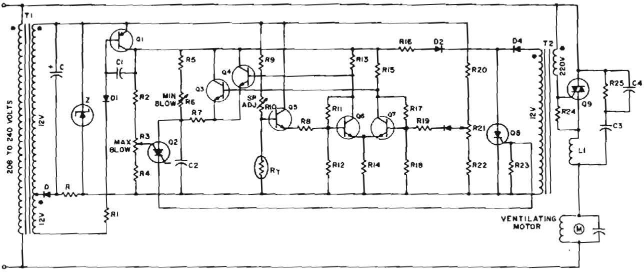
The detailed operation of the control is as follows. When the triac is pulsed on through either diac, it applies power to the motor load until the current reduces to near zero at the end of its half cycle. The triac then turns off, removing power from the motor, allowing the triggering circuits, consisting of C_1, C_2, R_1, R_3 and the two diacs, to start timing again with reference to the voltage across the triac. As mentioned earlier, this type of trigger synchronization may result in an unsymmetrical AC waveform applied to the motor, but for the intended S100E applications it is generally satisfactory. When the bonnet temperature is low, the resistance of R_3 will be high, and the time required for C_1, charging through R_3, to reach the breakover potential of its diac will be long. Therefore, depending upon the setting of R_1, it is possible that C_2 will reach the breakover potential of its diac first, guaranteeing the minimum speed limit. As the temperature of the bonnet increases, with resulting decrease in R_3, C_1 will fire the triac through its diac earlier in the cycle than C_2 and R_2 are capable of, increasing motor speed.

C_3 and R_2 prevent dv/dt triggering and, assisted by L_1 and C_4, smooth the steep voltage wavefront, reducing RFI to a tolerable level.

12.6.3 Ventilating Blower Control for Heating and Cooling

Some room conditioner systems are designed with a ventilating blower (or fan) proportionally controlled during the heating and cooling cycles. This has proven to provide excellent room temperature regulation.

The circuit of Figure 12.25 is such a control. It is designed to be operated from one thermostat located within the room. When neither room heating nor cooling is required, the control operates the blower at minimum speed. As room temperature decreases from SP, blower speed is proportionally increased. When the heating source increases room temperature the control will proportionally reduce the blower speed. Likewise when room temperature increases from SP, blower speed is proportionally increased and then proportionally decreased when the cooling source lowers the room temperature. From the previous discussion it should be noted that the control is capable of proportionally increasing blower speed for either an over or under temperature deviation from SP. In addition it has RFI and dv/dt suppression, line voltage synchronization with a continuous triac gate signal for good motor performance, minimum speed limit, thermostat isolation and is capable of controlling 6 amperes at 240 volts. Higher currents are possible, but probably not needed, by utilizing a larger power triac.



R_1, R_{21}, R_{23}	– 1K ohm	R_{12}, R_{18}	– 33K ohm	C	– GE43F9723AA9 250μF 25V	Q_9	– GESC141D
R_2, R_4	– 4.7K ohm	R_{13}, R_{15}	– 2.2K ohm	C_1	– GE75F1R5A472 .0047μF 50V	Z	– GEZ4XL12
R_3	– 2.5K ohm	R_{14}	– 680 ohm	C_2	– GEAA14A104A .1μF 100V	T_2	THORDARSON 23V123
R_5	– 100K ohm	R_{16}	– 10K ohm	C_3	– GE75F7R4-224 .22μF 400V		220V PRI
R_6	– 50K ohm	R_{17}	– 220K ohm	C_4	– GE75F4R4-473 .047μF 400V	T_1	24V CT SEC
R_7	– 1.5K ohm	R_{20}, R_{22}	– 3.9K ohm	D, D_1 thru D_4	– GEA14F		25 WATT
R_8, R_{19}	– 15K ohm	R_{24}, R_{25}	– 47 ohm	Q_1	– 2N5354	L_1	– 100μh
R_9	– 3.3K ohm	R	– 120 ohm	Q_2	– GE3N86		
R_{10}	– 5K ohm	R_T	– GE2R114	Q_3 thru Q_7	– GE2N3393		
R	– 470K ohm			Q_8	– GEC106Y		

NOTE:
ALL RESISTORS 1/2 WATT ±10% UNLESS OTHERWISE NOTED.

FIGURE 12.25 VENTILATING BLOWER CONTROL (HEATING AND COOLING)

The control is capable of being operated in conjunction with the cooling compressor and condenser control of Figure 12.23, therefore it utilizes their common components of T_1, D, C, R, Z and the thermostat, consisting of R_9, R_{10} and thermistor R_T.

The detailed operation is as follows:

When the triac Q_9 is triggered through T_2 by the triggering circuit, which consists of those components connected to the low voltage side of transformer T_1, it applies power to the ventilating motor.

T_2 performs three functions: (a) provides coupling from the isolated triggering circuit to the triac gate; (b) supplies a continuous gate signal prior to triac turn-on; (c) automatically provides a symmetrical negative half cycle triac gate signal after once being shorted during the positive half cycle by Q_8. Functions (b) and (c) require some explanation. Note that the primary (220 volt side) of T_2 is connected to the gate of the triac. With its secondary open circuited, and the triac off, its impedance is high and, combined with the shunting effect of R_{24}, will not allow the triac to turn on. Shorting the secondary of T_2 some time during the positive half cycle causes a large primary current to flow into the gate of the triac. The current continues until the triac turns on, shorting out the primary of T_2, stopping gate current and not allowing the transformer to change its flux level or direction. Removal of the short at the start of the negative half cycle and ultimately the turning off of the triac, results in the transformer preventing gate current until the supply voltage causes it to saturate during that negative half cycle. The transformer then permits sufficient turn on current until the triac turns on, again shorting out the primary of T_2, stopping gate current and not allowing the transformer to change its flux level or direction. Therefore, at the end of the negative half cycle the transformer core is reset ready to be shorted again during the positive half cycle. After a few cycles, the phase angle of negative cycle saturation will be very close to the phase angle at which shorting took place during the positive half cycle. Consequently T_2 provides a continuous gate signal during the negative half cycle until the triac turns on, symmetrical with that of the positive half cycle. The symmetry is best with a square loop core. However, the transformer used is a standard filament type and results in very good motor performance. It should be noted that Q_8, triggered by Q_2, shorts T_2 during the positive half cycle and at the desired phase angle.

Synchronization to the voltage supply is accomplished by Q_1. During the positive half cycle Q_1 is saturated and the DC supply voltage is applied to the triggering circuit. During the negative half cycle Q_1 is cut off, removing the DC potential, allowing T_2 to provide the predetermined negative half cycle symmetrical trigger.

Q_2 is turned on when its anode potential is approximately 0.6 volt higher than its gate, as determined by the ramp and pedestal charging of capacitor C_2. That is, C_2 charges very rapidly through Q_3 or Q_4 and R_7 and then continues to slowly charge through R_5 and R_6, providing a high gain, well defined trigger for Q_2. R_6 is then used as a reasonably independent minimum speed adjustment.

Q_3 and Q_4 allow the control to increase blower speed for either an over or under temperature deviation from SP. At SP, R_{21} is adjusted so that the potential at the emitters of Q_3 and Q_4 are equal. At this time C_2 is charged at a rate which results in the blower rotating at its minimum speed. When the temperature decreases, Q_7 decreases conduction and the voltage at Q_3 rises, charging C_2 faster, increasing blower speed. When the temperature increases, Q_6 decreases conduction and the voltage at Q_4 rises, again charging C_2 faster and increasing blower speed. The rate at which the blower increases speed with respect to temperature deviation is very dependent upon th gain of the Q_6 Q_7 differential amplifier as dictated by the R_{11}, R_8, R_{17}, R_{19} resistance ratios.

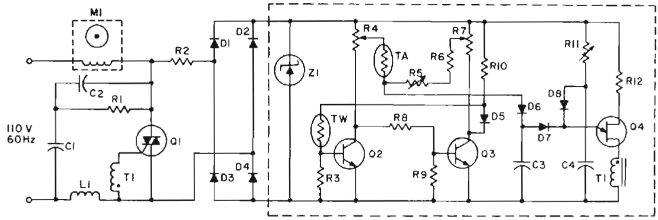
Capacitor C_1 reduces noise interference. Q_5 reduces the interference into the thermostat. R_{25} and C_3 prevent dv/dt triggering and, assisted by L_1 and C_4, smooth the steep voltage wavefront, reducing RFI to a tolerable level.

12.6.4 Fan and Coil Blower Control

Figure 12.26 shows a proportional motor speed control especially designed for fan and coil water systems. A fan and coil water system is a room temperature regulator capable of heating or cooling by means of passing hot or cold water, from a central supply, through heat exchanger coils in each room where a blower helps transfer the heat from or to the room air. The purpose of this solid state control is to improve room temperature regulation by proportionately controlling blower speed in accordance to room temperature demands as indicated by the room thermostat.

Since heating or cooling is accomplished by passing hot or cold water respectively through one coil, the control must again be capable, as in Figure 12.25, of increasing blower speed for either an over or under temperature deviation from SP. In addition it has RFI and dv/dt suppression, a minimum speed limit and is capable of controlling 6 amperes at 110 volts. Higher currents and voltages are possible but probably not necessary. The triggering circuit is shown within the dotted block and is synchronized to the power triac, Q_1. This type of synchronization is acceptable for the majority of the motors used in this application.

Q_1 is triggered on with a pulse supplied by unijunction Q_4, through T_1. R_{11} and C_4 determine the minimum speed. When a unijunction firing signal is supplied through D_7 later in the cycle than that supplied through D_8 as a result of C_4 charging through R_{11}, the blower rotates at the minimum speed dictated by R_{11}. When the central water control determines that cooling is required, and provides water colder than normal room temperature, the water sensing thermistor T_W causes Q_2 to be off and Q_3 on. This requires C_3 to charge through R_4 and the room temperature thermistor T_A. If the relative resistance of T_A with respect to the SP potentiometer R_5 is such so as to request room cooling, C_3 will charge in a ramp and pedestal fashion[2] to the unijunction firing voltage ahead of C_4, increasing blower speed and decreasing room



R_1	- 82 ohm	C_1	-.22μ, 200V	Z_1	- GE [illegible]4XL20
R_2	- 4.7K, 4W	C_2	-.05μ, 200V	T_W	- GE ID103, 5K @ 25°C THERMISTOR
R_3, R_{12}	- 1K	C_3	-.1μ, 50V	T_A	- GE ID103, 5K @ 25°C THERMISTOR
R_4, R_5, R_7	- 5K POT, 1/2W	C_4	-.1μ, 50V	M_1	- 3 AMP SHADED POLE MOTOR
R_6, R_9	- 3.3K	D_1 thru D_4	- GE GEB102	T_1	- SPRAGUE 11Z12 PULSE TRANSFORMER
R_8	- 22K	D_5 thru D_8	- A14F		
R_{10}	- 4.7K	Q_1	- TRIAC AS REQUIRED		
R_{11}	- 100 ohm, 1/2W	Q_2, Q_3	- 2N2712		
		Q_4	- GE 2N2646		

NOTE:
ALL RESISTORS 1/2W ±10% UNLESS OTHERWISE SPECIFIED.

FIGURE 12.26 FAN AND COIL BLOWER SPEED CONTROL, TEMPERATURE REGULATOR

temperature. As more cooling is required the blower speed will be modulated up to its maximum. In the event the central water control determines that heating is required and provides water warmer than nominal room temperature, T_w forces Q_3 off and Q_2 on. Now C_3 charges through R_7, R_6 and R_5. Consequently when the relative resistance of T_A with respect to R_5 is such so as to request room heating, C_3 will again charge to the unijunction firing voltage ahead of C_4, increasing blower speed and room temperature. Thus blower speed is increased for either an over or under temperature deviation from SP.

R_1 and C_1 prevent dv/dt triggering and, assisted by L_1 and C_2, smooth the steep voltage wavefront, reducing RFI to a tolerable level.

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2. Cape, R. C. and Tull, R. H., "Test Room Performance of Line-Voltage Thermostats," IEEE Conference Record of 1967 Industrial and Commercial Power Systems and Electric Space Heating and Air Conditioning Joint Technical Conference, May 22-25, 1967.
3. Application Data 3702, General Electric Company, Edmore, Michigan.
4. Howell, E. Keith, "Switch From Hot to Cool," Electronic Design, February 15, 1967.

NOTES

13 CHOPPERS, INVERTERS AND CYCLOCONVERTERS

This chapter describes choppers, inverters and cycloconverters using SCR's which perform the functions previously performed by electrical machines, mechanical contacts, spark gaps, vacuum tubes, thyratrons and power transistors. These functions include standby power supplies, vibrator power supplies, radio transmitters, sonar transmitters, variable-speed AC motor drives, battery-vehicle drives, ultrasonic generators, ignition systems, pulse-modulator switches, etc.

The advantages of using equipment with solid-state switches to perform these functions are:

Low maintenance
Reliability
Long life
Small size
Light weight
Silent operation
Insensitivity to atmospheric cleanliness or pressure
Tolerance of freezing temperatures
Operable in any attitude
Instantaneous starting
High efficiency
Low cost

13.1 CLASSIFICATION OF INVERTER CIRCUITS

The following definitions are used in this chapter:

Rectifier:	Equipment for transforming AC to DC
Inverter:	Equipment for transforming DC to AC
Converter:	Equipment for transforming AC to AC
DC Converter:	Equipment for transforming DC to DC
Cycloconverter:	Equipment for transforming a higher frequency AC to a lower frequency without a DC link
Cycloinverter:	The combination of an inverter and a cycloconverter
Chopper:	A "single ended" inverter for transforming DC to DC or DC to AC

Note: The term inverter is also used in this chapter as a generic term covering choppers, inverters, and the several forms of converters. Thus "Classification of Inverters" covers classification of Choppers, Inverters, Converters, and DC Converters.

13.1.1 Classes of Inverter Circuits

The basic classification of inverter circuits is by methods of turn-off. These have been described in Chapter 5. There are six classes:

Class A Self commutated by resonating the load
Class B Self commutated by an LC circuit
Class C C or LC switched by a load-carrying SCR
Class D C or LC switched by an auxiliary SCR
Class E External pulse source for commutation
Class F AC line commutated

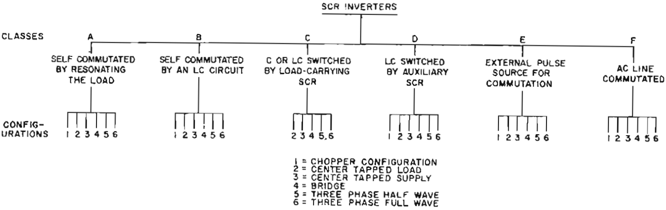


TABLE 13.1

13.1.2 Properties of the Inverter Classes

Class A – Self commutated by resonating the load. These inverters are most suitable for high-frequency operation, i.e., above about 1000 cps, because of the need for an LC resonant circuit which carries the full load current. The current through the SCR is nearly sinusoidal and so the initial di/dt is relatively low. Class A inverters lend themselves to output regulation by varying the frequency of a pulse of fixed width (time ratio control).

Class B – Self commutated by an LC circuit. The great merit of this class is circuit simplicity, the Morgan chopper being an outstanding example. Regulation is by time ratio control. Where saturable reactors are used, some skill is necessary in the design of these components, and manufacturing repeatability must be checked.

Class C – C or LC switched by a load-carrying SCR. An example of this class of inverter is the well known McMurray-Bedford inverter. With the aid of certain accessories this class is very useful at frequencies below about 1000 cps. External means must be used for regulation.

Class D – L or LC switched by an auxiliary SCR. This type of inverter is very versatile as both time-ratio and pulse-width regulation is readily incorporated. The commutation energy may readily be transferred to the load and so high efficiencies are possible.

Class E – External pulse source for commutation. This type of commutation has been neglected. It is capable of very high efficiency as only enough energy is supplied from the external source for commutation. Both time-ratio and pulse-width regulation are easily incorporated.

Class F – AC line commutated. The use of this type of inversion is limited to those applications where a large amount of alternating power is already available. Efficiencies are very high.

13.1.3 Inverter Configurations

Rectifier circuits occur in several configurations such as half-wave, full-wave, bridge, etc. Inverter circuits may be grouped in an analogous manner.

Figure 13.1 shows the different types of configurations. Methods of triggering and commutation have been left out for clarity.

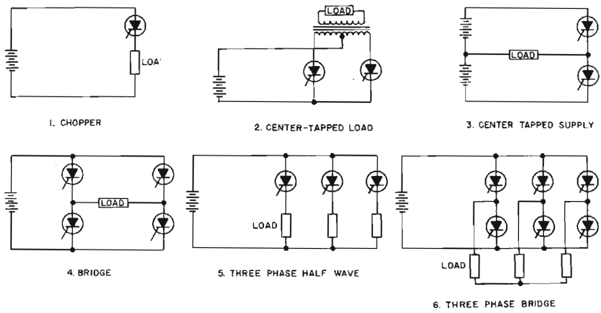


FIGURE 13.1 INVERTER CONFIGURATIONS

13.1.4 Properties of the Different Inverter Configurations

CONFIGURATION	1	2	3	4	5	6
	Chopper	CT Load	CT Supply	Bridge	3φ Half-Wave	3φ Bridge
Blocking Volts(1)	E	2E	E	E	E	E
Peak Load-Volts	E	E(2)	½ E	E	E	E(3)
DC in Load	yes	no	no	no	yes	no(4)
Number of SCR's	1	2	2	4	3	6
Ripple Frequency in Supply	f	2f	f	2f	3f	6f
Ave SCR Current(1) / Supply Current	1	1/2	1	1/2	1/3	1/3
Transformer-less Operation Possible	yes	no	yes	yes	yes	yes

(1) Ignoring overshoot due to commutation.
(2) Using a 1:1:1 transformer.
(3) Line-to-line voltage.
(4) Assuming symmetrical loading.

13.1.5 Discussion of Classification System

This method of classification gives thirty-five (35) different classes and configurations. However there are many circuits which could fall into the same classification and which are yet different. This occurs particularly in Class D where the method of commutating the auxiliary SCR may take many forms. There must therefore be several hundred possible inverter circuits.

In the following pages five examples are given to illustrate the scope of SCR inverters and the design procedure. The examples cover perhaps 1% of the possible circuit variations. It is for the equipment designer to use the classes and configurations together with the accessories to be described as building blocks to form the best combination for this particular application.

13.2 TYPICAL INVERTER CIRCUITS

13.2.1 A Class A Inverter

The design of Class A inverters has been well covered in the literature.[1] The following data, taken from Reference 1.4 of Section 13.6, illustrates the performance of one Class A inverter. Space does not permit the inclusion of the development of design procedures.

13.2.1.1 Circuit Description

The operation of the circuit is as follows. In Figure 13.2 when SCR_1 is triggered, current flows from the supply E_1 charging up capacitor C to a voltage approaching $2E_1$. The current then reverses and flows back to the supply via diode D_1 and C discharges. During the reverse current flow, turn-off time is presented to SCR_1. SCR_2 is triggered next and a similar cycle occurs in the lower half of the circuit with a negative going pulse of voltage appearing across C. SCR_1 is now triggered again and so the cycles repeat.

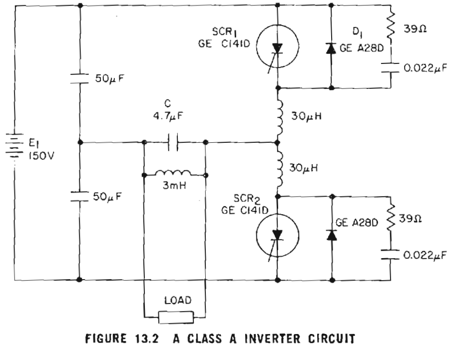


FIGURE 13.2 A CLASS A INVERTER CIRCUIT

Figures 13.3(a) and (b) show the circuit waveforms with no load and full load respectively. A comparison reveals some of the features of this new inverter. The output voltage, the peak SCR voltage, and the output voltage waveform remain virtually unchanged.

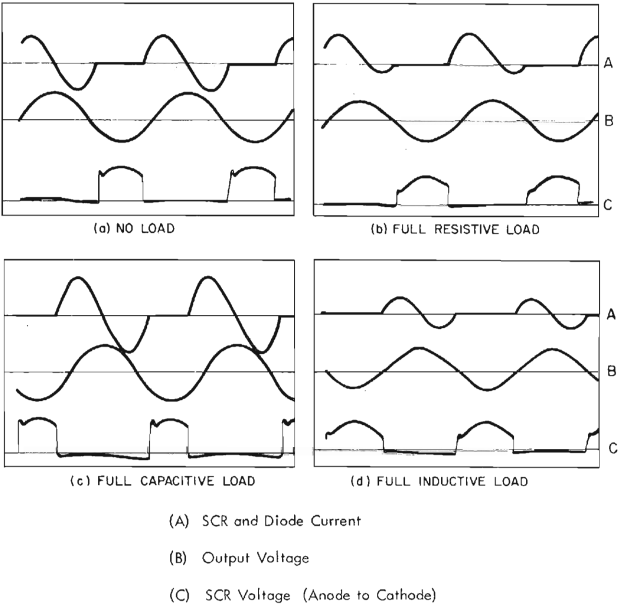


FIGURE 13.3 CLASS A INVERTER WAVEFORMS FOR CIRCUIT OF FIGURE 13.2

Figure 13.3(c) shows the effect of a heavy capacitive load on the circuit waveform. Note the broadening of the current pulses and the increase in output voltage. Figure 13.3(d) shows the effect of a heavy inductive load with an opposite trend. Neither leading nor lagging zero power factor loads have any serious effects on turn-off time or component voltages in tihs inverter circuit.

Figure 13.4 shows the effect of varying the triggering frequency (f_o) on the output voltage waveform while keeping the resonant frequency (f_r) of the LC circuit constant. Lowest distortion is seen to occur at a ratio of $f_r/f_o = 1.35$.

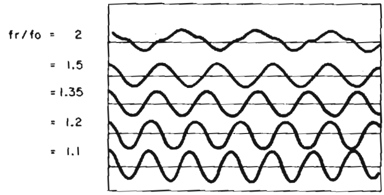


FIGURE 13.4 EFFECT OF VARYING RATIO OF RESONANT FREQUENCY OF LC CIRCUIT f_r TO TRIGGERING FREQUENCY f_o ON OUTPUT WAVEFORM OF CLASS A INVERTER (CIRCUIT OF FIGURE 13.2)

The features of this inverter are:

1. Good output waveform.
2. Excellent load regulation.
3. Ability to operate into an open circuit.
4. Ability to work into a wide range of reactive loads.
5. Relatively low and constant value of SCR voltage.

Figure 13.5 gives the calculated and measured load regulation curves for reactive and resistive loads of the design described in detail in Reference 1.4 of Section 13.6.

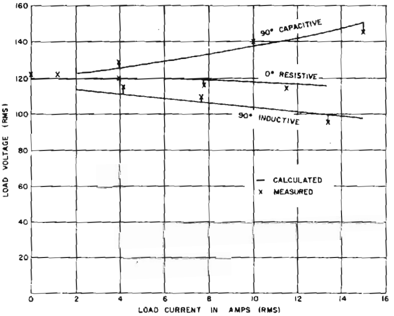


FIGURE 13.5 LOAD REGULATION OF CLASS A INVERTER OF FIGURE 13.2

13.2.1.2 Applications

The following are some of the uses for Class A inverters:

- Ultrasonic cleaning, welding and mixing equipment
- Induction heaters
- Radio transmitters in the VLF band
- Sonar transmitters
- Cycloconverter supplies, the output of the cycloconverter itself being useful for all applications where AC power is used

- DC to DC converters where the advantages of light weight, small size, low cost and fast response time due to the high-frequency link are very apparent

13.2.2 A Class B Inverter

While many examples exist in the literature of Class B choppers, until recently, Class B inverters were not widely discussed. Recent literature has reported on novel developments utilizing the Class B principle in DC to AC conversion. The following data, taken from References 8.12 and 8.22 of Section 13.6 discusses the principle of operation and performance features of one Class B inverter. Space does not permit the inclusion of the development of design procedures. Design equations and notes are included in the cited references.

13.2.2.1 Circuit Description

The Class B regulated sine wave inverter is derived from the basic Class B tuned inverter circuit of Figure 13.6. The basic circuit suffers from three major drawbacks which the circuit of Figure 13.8 overcomes. The circuit performance limitations are: instability and severe transients upon load disruption due to stored reactive power, lack of means for voltage regulation and sensitivity to load power factor. In spite of its sinusoidal output characteristics these disadvantages have severely limited application of the basic circuit.

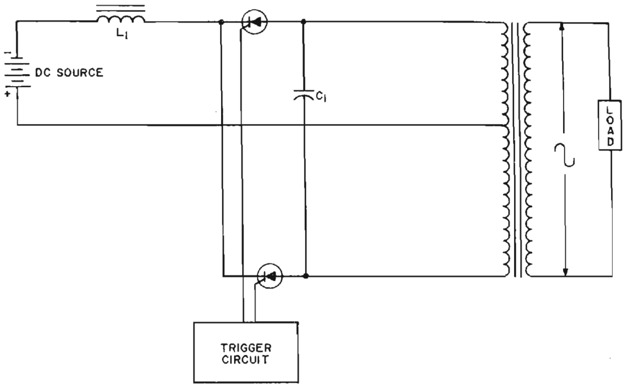


FIGURE 13.6 BASIC CLASS B TUNED INVERTER

Figure 13.7 shows the first of two major modifications introduced to the basic circuit. The purpose of the additional components, L_2, L_3 and D_1 through D_4, is to provide a path for rapid return of excess reactive current. This passive stabilization network eliminates unwieldy voltage transients and stabilizes the output voltage for large abrupt changes in output loading. Its main feature is its ability to accomplish the above goals without substantial clipping or distortion of the output wave shape. This is accomplished by returning the feedback current through a differential choke L_2 such that equal current is distributed between Points A and B of Figure 13.7. Point B contains a considerable amount of pulsating voltage which would normally severely affect the feedback current and consequently cause output voltage distortion. By use of L_2 both the clipping that would be present using solely Point A for a return path, and the distortion of using Point B is eliminated. Diodes D_1 and D_2 serve to isolate L_1 from L_2. L_3 is used to limit extremes of feedback current while being dimensioned small enough to provide a short time constant for good short time feedback performance under transient conditions. Diodes D_3 and D_4 serve to rectify the feedback current for return to the supply. It has recently shown that it is possible to combine L_1 and L_2 by judicious tapping of L_1. See Reference 8.12 of Section 13.6.

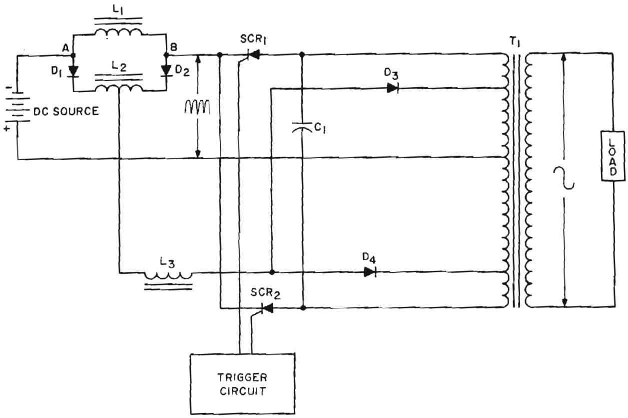


FIGURE 13.7 SINE WAVE INVERTER WITH PASSIVE FEEDBACK STABILIZATION

Figure 13.8 shows the completed circuit with the added second addition of an active feedback system capable of providing voltage regulation for input source and load variations. The active regulating circuit is comprised of C_2, L_4, and SCR_3 and SCR_4. Operation of the active feedback circuit is controlled by SCR's 3 and 4. By varying their phase angle triggering, the voltage on capacitor C_2 can be made to vary, such as to either add or subtract from the source supply voltage.

Since this voltage acts as a bucking or boosting voltage in series with the source, the output voltage can be effectively regulated over a wide range of supply voltage deviation and load conditions. L_4 serves to smooth the active feedback current to limit the pulse current duty required of capacitor C_2. L_5 is added to provide di/dt limiting for SCR's 1 and 2 and is not part of the active stabilization network.

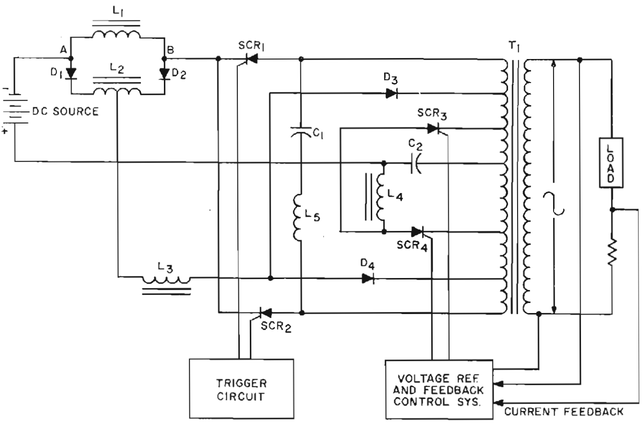


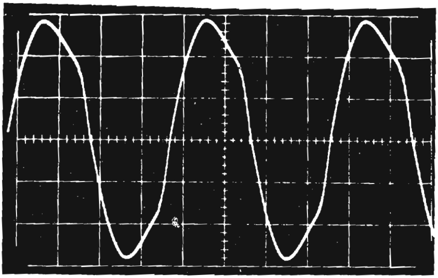
FIGURE 13.8 COMPLETE CLASS B REGULATED SINE WAVE INVERTER

13.2.2.2 Circuit Performance

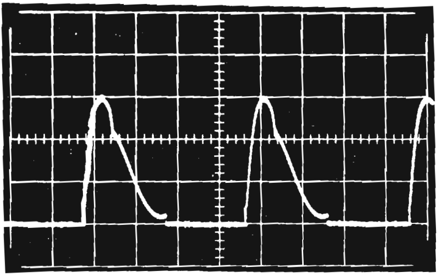
Output voltage wave shapes together with main SCR current and voltage wave shapes are shown in Figure 13.9.

Typical regulation achievable, no load to full load for a ±25% input source variation, is ±2.5% output voltage change. The above is based upon a 50 Hertz, 220 volt output operating from a nominal 28 volt input source. The circuit performance improves with increasing nominal supply voltages. The circuit has been shown to have better than the above performance levels when operated from a 220 volt input source including variations due to a full range of leading and lagging load power factors in addition to the no-load condition.

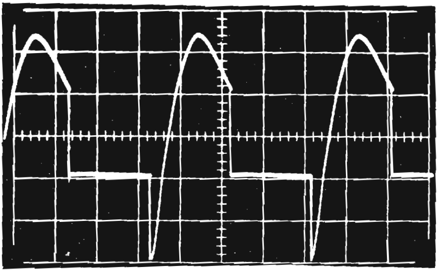
A final feature worthy of mention is the soft commutating duty imposed upon the main SCR as shown by Figures 13.9(b) and (c). Note the reverse voltage and low reapplied dv/dt during the SCR turn-off interval.



(a) Output Voltage



(b) Main SCR Current



(c) Main SCR Voltage

FIGURE 13.9 CIRCUIT OPERATING WAVEFORMS

13.2.3 Class C Inverters

Typical of the Class C inverter is the well-known "McMurray-Bedford Inverter." This inverter circuit is shown in Figure 13.10. It operates as follows. Assume SCR_1 conducting and SCR_2 blocking. Current from the DC supply flows through the left side of the transformer primary. Autotransformer action produces a voltage of $2E_b$ at the anode of SCR_2 charging capacitor C to $2E_b$ volts. When SCR_2 is triggered, point (A) rises to approximately $2E_b$ volts, reverse biases SCR_1, and turns it off. Capacitor C maintains the reverse bias for the required turn-off time. When SCR_1 is again triggered, the inverter returns to the first state. It follows that the DC supply current flows alternately through each side of the transformer primary producing a square-wave AC voltage at the secondary.

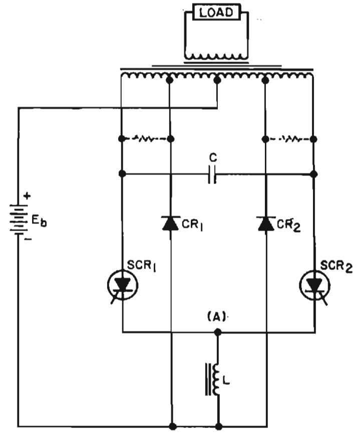


FIGURE 13.10 McMURRAY-BEDFORD INVERTER

Rectifiers CR_1 and CR_2 feed back, to the DC supply, reactive power associated with capacitive and inductive loads. With inductive loads, energy stored in the load at the end of a half cycle of AC voltage is returned to the supply at the beginning of the next half cycle. Conversely with capacitive loads, energy stored in the load at the beginning of a half cycle is returned to the supply later in that half cycle.

The feedback rectifiers are connected between the negative supply terminal and taps on the transformer primary. In applications where losses would not be excessive, the diodes may be returned to the SCR anodes through small resistances as indicated by the dashed lines in Figure 13.10. In the tap connection some energy trapped in L is fed to the load. Use of the tap connection results in some variation of output with load power factor, but far less than with no feedback rectifiers.

Optimum values for the commutating elements of a "McMurray-Bedford Circuit" are:

$$C = \frac{t_c\, I_{com}}{1.7\, E_b}$$

$$L = \frac{t_c\, E_b}{0.425\, I_{com}}$$

where t_c = minimum turn-off time presented to the SCR
I_{com} = maximum value of load current at commutation

Inverter waveshapes for different load power factors are shown in Figure 13.11.

The above relations define C and L such that commutation is insured for maximum lagging load current.

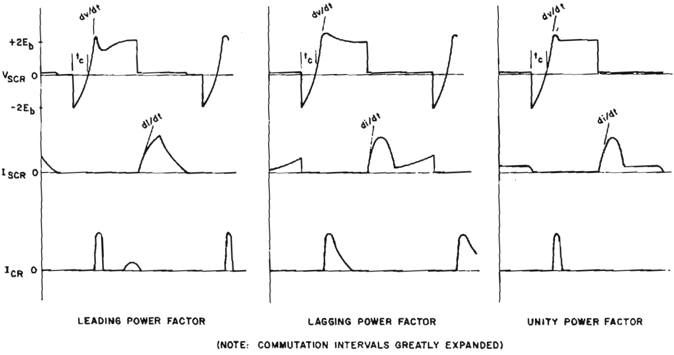
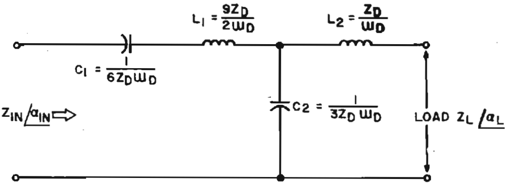


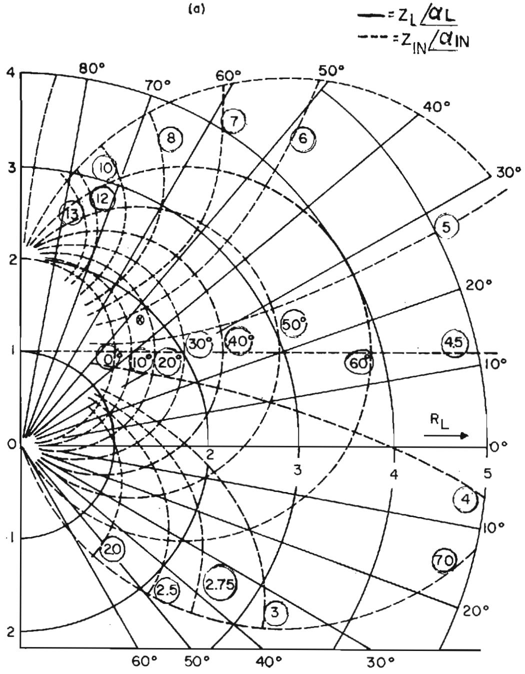
FIGURE 13.11 INVERTER WAVESHAPES FOR VARIOUS LOAD POWER FACTORS

13.2.3.1 Ott Filters For Class C Inverters

The Ott filter shown in Figure 13.12(a) is an extremely useful circuit when used in conjunction with Class C inverters. It performs three important functions. It provides a sine wave output thus essentially eliminating the harmonic content to the load. It provides good load regulation while at the same time maintaining a capacitive load to the inverter over a large load range of load power factor. This capacitive load reflected to the inverter aids SCR commutation as well as inverter output regulation. The Smith chart shown in Figure 13.12(b) provides the designer with a plot of filter input impedance as a function of filter load impedance, normalized to the filter design impedance, Z_D.



(a)



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(b)

FIGURE 13.12 INPUT IMPEDANCE CHART

While an example filter design is worked out in Section 13.2.3.2 a few examples of the use of the chart are given below to aid in its interpretation. The solid lines shown are those of the normalized filter *load impedance*. The radial lines being load phase angle and the circles with center at 0, j0 are load impedance magnitude values. The normalized input impedance is read from the dotted lines where now the circles centering on (−, j1) are capacitive phase angles and the dotted divergent radii are normalized input impedance magnitude values. The values of the dotted lines are identified by being enclosed in circles to separate them from the load set of loci.

From the example below the filter design impedance was chosen as 15 ohms.

The following table of impedances obtained using Figure 13.12(b) should allow one to become proficient in its use.

Given		Read From Smith Chart	
Load Z_L $/a_L$ Ohms	Normalized To Z_D	Normalized Input Z_{IN} $/a_{IN}$	Input Z Ohms
$30\ \angle 0°$	$2\ \angle 0°$	$3.1\ \angle -45°$	$46.5\ \angle -45°$
$20 + j20 = 28.3\ \angle 45°$	$1.88\ \angle 45°$	$5.5\ \angle -16°$	$83\ \angle -16°$
$22.5\ \angle -45°$	$1.5\ \angle -45°$	$2.15\ \angle -65°$	$32.5\ \angle -65°$
$45\ \angle 45°$	$3\ \angle 45°$	$6.1\ \angle -47°$	$91.5\ \angle -47°$
$34.5\ \angle 70°$	$2.3\ \angle 70°$	$12\ \angle -30°$	$180\ \angle -30°$

TABLE 13.2 USE OF SMITH CHART OF FIGURE 13.2(b)

By an examination of the table and the chart several advantages of the Ott filter become apparent. First the input impedance remains capacitive in spite of far-ranging changes in the load power factor and impedance magnitude. Furthermore, one can easily see that as long as the normalized load impedance magnitude exceeds 2 the input impedance is always capacitive. The Ott filter has the further advantage of having a normalized impedance of 4.5 for open, i.e., infinite load impedance, unlike some filters which decrease input impedance with increasing output impedance. Lastly the input impedance of the filter reflects the output impedance when the output becomes short circuited, i.e., the load and the input zeroes are one and the same, thus short circuit input current is theoretically infinite; this being ideal for tripping protective devices under faulted load conditions. The designer should take note that the chart of Figure 13.12(b) is valid for the filter design of the circuit in Figure 13.12(a). Use of other design formula of the same class will result in a different impedance transformation chart. The reader is referred to Reference 3.9 of Section 13.6 for chart construction details.

13.2.3.2 Design Procedure

The following is the design procedure for a Class C square wave inverter used in connection with the Ott filter to produce sinusoidal voltage.

Required specifications

Output voltage (E_o) – Volts (RMS)
Output power (P_o) – watts
Output frequency (f) – Hz
Rated load power factor (pf)
Available DC supply (E_b) – volts

FILTER DESIGN

Load Resistance

$$R_L = \frac{E_o^2 \times pf^2}{P_o} \text{ (ohms)}$$

Load Reactance

$$X_L = \frac{R_L}{pf} \sqrt{1 - pf^2} \text{ (ohms)}$$

Load Impedance

$$|Z_L| = \sqrt{R_L^2 + X_L^2} \text{ (ohms)}$$

$$\angle Z_L = \cos^{-1} pf \text{ (degrees)}$$

Filter Design Impedance

$$Z_D \leqq \frac{|Z_L|}{2} \text{ (ohms)}$$

Design Radian Frequency

$$\omega_D = 2\pi f \text{ (radians/sec)}$$

Filter Element Values

$$C_1 = \frac{1}{6 Z_D \omega_D} \qquad C_2 = \frac{1}{3 Z_D \omega_D} \text{ (farads)}$$

$$L_1 = \frac{9 Z_D}{2 \omega_D} \qquad L_2 = \frac{Z_D}{\omega_D} \text{ (henrys)}$$

Filter Input Impedance

Z_{IN}, R_{IN} and X_{IN} are determined from Figure 13.12(b)

Input Voltage to Filter

$$E_{(SQ)} = \frac{\sqrt{2}}{4} \pi \left| Z_{IN} \right| \left(\frac{P_o}{R_{IN}} \right)^{1/2} \text{(volts)}$$

INVERTER DESIGN

Transformer Turns Ratio

$$n = \frac{E_{(SQ)}}{E_b}$$

Input Power, assuming 85% efficiency

$$P_I = P_o \times \frac{100}{85} \text{ (watts)}$$

Average Current in SCR

$$I_{AV(SCR)} \cong \frac{P_o \, |Z_{IN}|}{2 \, E_b \, R_{IN}}$$

Peak Forward Voltage Across SCR's

$$V_{PK(SCR)} < 2.5 \, E_b$$

From the expressions for $I_{AV(SCR)}$ and $V_{PK(SCR)}$ a preliminary choice of SCR may be made.

Peak Current in SCR's

$$I_{PK(SCR)} = 4 \, E_b \sqrt{\frac{C}{L}}$$

Turn-Off Time

$$t_c = \frac{2\pi}{3} \sqrt{LC}$$

Rate of Reapplication of Forward Blocking Voltage

$$dv/dt = \frac{0.85 \, E_b}{\sqrt{LC}}$$

Turn-on di/dt

$$di/dt \Big|_{t=0} = \frac{2 \, E_b}{L}$$

From the preceding four relationships, L and C may be determined as follows

$$L = \frac{6 \, E_b \, t_c}{\pi \, I_{PK(SCR)}}$$

Choose the desired t_c and $I_{PK(SCR)}$ and determine L. Check dv/dt with the following

$$dv/dt = \frac{3.44 \, E_b^2}{L \, I_{PK(SCR)}}$$

If dv/dt is too high, increase L accordingly and recalculate $I_{PK(SCR)}$. Now:

$$C = \frac{3 \, t_c \, I_{PK(SCR)}}{8\pi \, E_b}$$

The minimum value of L should be such as to keep the turn-on di/dt well below specification.

13.2.3.3 A 400 Hz Inverter With Sine Wave Output

The design procedure for a 400 Hz inverter with sine wave output is given to illustrate the application of a Class C inverter used in conjunction with the Ott filter.

Required Specifications

Output power = 360 watts
Output voltage = 120 volts (RMS)
Output frequency = 400 Hz
Rated load power factor = 0.7 lagging
Available DC supply = 28 VDC

FILTER DESIGN

Load Resistance

$$R_L = \frac{(120)^2 \times (.7)^2}{360} = 20 \text{ ohms}$$

Load Reactance

$$X_L = \frac{20}{.7}\sqrt{1-(.7)^2} = 20 \text{ ohms}$$

Load Impedance

$$|Z_L| = \sqrt{(20)^2 + (20)^2} = 28.3 \text{ ohms}$$

$$\angle Z_L = \cos^{-1}(.7) = \frac{\pi}{4} = 45°$$

Filter Design Impedance

$$Z_D \leq \frac{28.3}{2}$$

Choose $Z_D = 15$ ohms

Design Radian Frequency

$$\omega_D = (2)(3.14)(400) = 2500 \text{ radians/sec}$$

Filter Element Values

$$C_1 = \frac{1}{(6)(15)(2500)} = 4.5 \times 10^{-6} \text{ farads}$$

$$C_2 = \frac{1}{(3)(15)(2500)} = 9 \times 10^{-6} \text{ farads}$$

$$L_1 = \frac{(9)(15)}{2(2500)} = 27 \times 10^{-3} \text{ henrys}$$

$$L_2 = \frac{15}{2500} = 6 \times 10^{-3} \text{ henrys}$$

Filter Input Impedance

From Figure 13.12(b) (point marked X)

$$Z_{IN} = (15)\,5.5 \angle -16°$$
$$= 80 - j\,23$$
$$R_{IN} = 80 \text{ ohms}$$
$$X_{IN} = 23 \text{ ohms}$$
$$|Z_{IN}| = 83 \text{ ohms}$$

Input Voltage to Filter

$$E_{SQ} = \frac{\sqrt{2}}{4} (3.14)(83) \left(\frac{360}{80}\right)^{1/2} = 195 \text{ volts}$$

INVERTER DESIGN

Transformer turns ratio

$$n = \frac{195}{28} = 7$$

Input Power (assuming 85% efficiency)

$$P_I = 360 \times \frac{100}{85} = 424 \text{ watts}$$

Average Current in SCR's

$$I_{AV(SCR)} \cong \frac{(360)(83)}{(2)(28)(80)} = 6.8 \text{ amps}$$

Peak Forward Voltage Across SCR's

$$V_{PK(SCR)} = (2.5)(28) = 70 \text{ volts}$$

From the above a G-E type C141A is chosen.

Commutating Elements

The C141A has a maximum turn-off time of 10μ sec and maximum dv/dt of 200 volts/μsec. Choose $t_c = 12\ \mu$sec and $I_{PK(SCR)} = 14$ amps.

$$L = \frac{6(28)(12)}{(14)(3.14)} = 45 \times 10^{-6} \text{ henrys}$$

Checking dv/dt,

$$dv/dt = \frac{(3.44)(790)}{(45 \times 10^{-6})(14)} = 4.3 \text{ volts}/\mu\text{sec}$$

$$C = \frac{(3)(12 \times 10^{-6})(14)}{(8)(3.14)(28)} = .75 \times 10^{-6} \text{ farads}$$

Turn-On di/dt

$$di/dt \Big|_{t=0} = \frac{2 \times 28}{45} = 1.25 \text{ A}/\mu\text{sec}$$

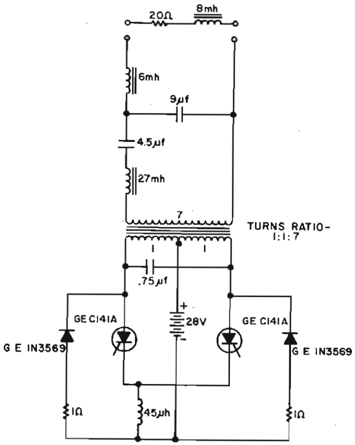


FIGURE 13.13 A 400 Hz INVERTER WITH THE OTT FILTER

NOTES:

1. Feedback rectifiers are chosen to have current and voltage capability similar to the SCR's.
2. One ohm series resistors are used to limit power dissipation in the feedback rectifiers.
3. The composite inverter-filter circuit for the 400 Hz inverter is shown in Figure 13.13.
4. A suitable trigger circuit for the Class C inverter is shown in Figure 4.50.

13.2.4 Designing a Battery Vehicle Motor-Controller Using The Jones SCR Chopper (Class D)

13.2.4.1 Introduction

Three methods are available for controlling the voltage to, and hence the speed of, a battery-driven DC series motor of any appreciable power:

1. A rheostat may be inserted in series with the motor. This method has a smooth action but power is wasted in the rheostat.

2. The battery or the field winding may be switched in series or parallel. This method is virtually lossless but the action is jerky.

3. The third method involves the use of a rapid-acting switch, called a chopper, in series with the motor.

Choppers have several modes of possible control. Figure 13.14 shows the action of the chopper for the pulse width modulation and a combination of pulse width and frequency modulation.

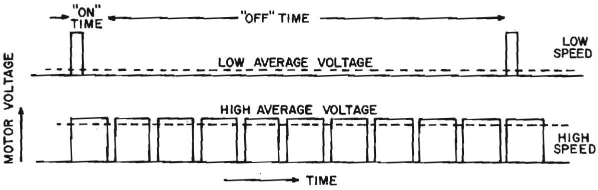


FIGURE 13.14 CHOPPER WAVEFORMS

All three techniques control motor speed by varying the ratio of switch "on" time to "off" time. At low speeds the "on" time is much less than the "off" time. The result is that the average voltage across the motor is low. As the "off" time is decreased so the average voltage increases. The change in the average voltage is as smooth as the "off" time may be readily adjusted by a potentiometer controlled timer. This method combines the advantages of the two previous methods in that both smooth control and high efficiency are achieved simultaneously. The SCR makes an ideal switch for this chopper application.

Figure 13.15 shows a diagram complete except for the method of turning the SCR on and off. This will be discussed later.

S_2, S_3, S_4 and S_5 are field-reversing relays. With S_2 and S_5 closed the direction is forward, whereas with S_3 and S_4 closed the direction is reverse.

This SCR chopper has a practical duty cycle ranging from about 20% to about 80%.

For the standstill state all four switches, S_2, S_3, S_4 and S_5, are open. When S_2 and S_5 are closed, and with the chopper operating at low speed, about 20% of the supply voltage is applied to the motor. This voltage may be increased to 80% of the battery voltage as more torque is required. When 80% is reached relay S_1 is closed applying full voltage to the motor and maximum torque is obtained.

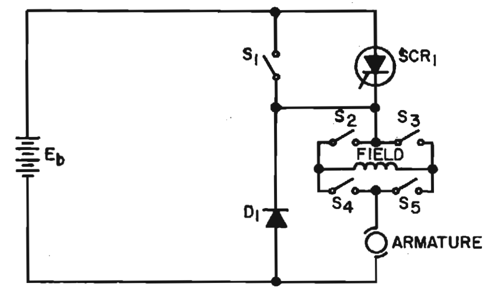


FIGURE 13.15 BASIC VEHICLE CONNECTIONS

The diode D_1 is the well known free-wheeling diode. Its purpose is to carry the inductive current when the SCR is turned off, thus preventing high voltages appearing across the motor.

The controller to be described uses a variable-frequency constant-pulse-width system.

It is capable of pulse width modulation control by changing the trigger circuitry.

13.2.4.2 Operation of the Jones Commutation Circuit

Figure 13.16 shows the basic circuit.

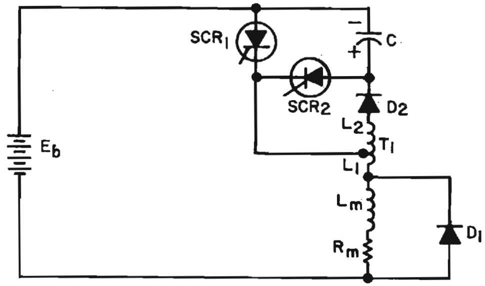


FIGURE 13.16 THE JONES CHOPPER

Figure 13.16 is redrawn in Figure 13.17 to show six working circuits representative of the basic phases of operations of the Jones Chopper.

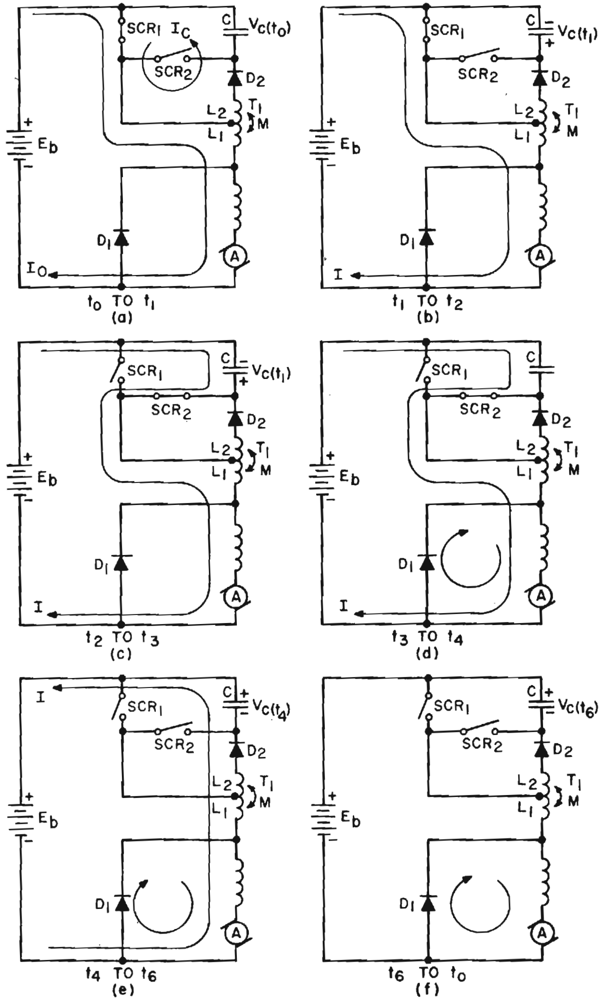


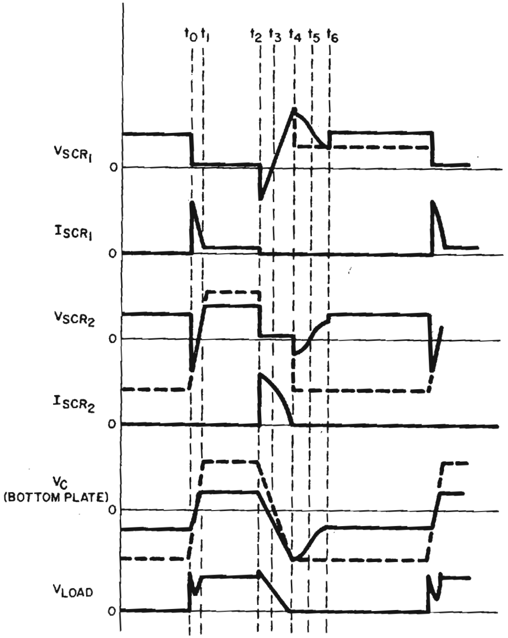
FIGURE 13.17 JONES CHOPPER WORKING CIRCUITS

Switches are shown instead of SCR's to indicate the conducting state. As the switches operate during the cycle, the chopper changes from one working circuit to another. These phases of operation represent consecutive time intervals totaling one full cycle of operation. In the circuit waveforms of Figure 13.18 the times t_0, t_1, t_2 . . . . correspond with the working circuits of Figure 13.17.

The operating cycle is initiated by triggering SCR_1 at time t_0. The bottom plate of capacitor C then starts to charge positively. Note that in Figure 13.17(a) the amount of initial voltage ($V_{c(t_0)}$) on C is not shown in general it will be a different value for starting than it will be for running. The peak voltage to which C charges at t_1, ($V_{c(t_1)}$), depends on ($V_{c(t_0)}$).

At time t_1, the bottom plate of C has resonantly charged, or "rung" via L_2, to its peak positive voltage. Note that the peak positive voltage is always less than, but approximately equal to, the peak negative voltage at t_0. In effect turning on SCR_1 serves to reverse the voltage on the commutating capacitor. The peak positive voltage on C is held by the charging diode D_2. Energy is now available to commutate SCR_1. Meanwhile SCR_1 is delivering power to the load through L_1 as shown in Figure 13.17(b). Note that the use of the autotransformer insures that whenever current is delivered from the DC source to the load, a voltage is induced in L_2 in the correct polarity for charging the commutating capacitor. Thus the autotransformer measurably enhances the reliability of the circuit.

At time t_2, SCR_2 is triggered and the capacitor voltage is placed directly across SCR_1. After cessation of its reverse recovery current, SCR_1 reverts to the blocking state and behaves as an open circuit. The load current transfers to SCR_2, L_1 and the load. This discharge current increases until, at t_3, the voltage across the capacitor is zero and the bottom plate of the capacitor begins to swing negative (Figure 13.17(d)); forward blocking voltage is applied to SCR_1, and the current in SCR_2 begins to decrease. To insure continuity of inductive load current, D_1 begins to conduct at t_3. The time duration t_2 to t_3 is the circuit turn-off time presented to SCR_1.



Notes:

SOLID LINES DEPICT OPERATION WITH DIODE D_2 AS SHOWN IN FIGURE 13.17. DOTTED LINES DEPICT OPERATION OF CIRCUIT SHOWN IN FIGURE 13.17 WITH DIODE D_2 REPLACED BY SCR_3.

FIGURE 13.18 CURRENT AND VOLTAGE WAVEFORMS FOR THE JONES CHOPPER

The bottom plate of C continues to swing negative until it reaches a peak value at time t_4 when the current in SCR_2 attempts to reverse thus commutating SCR_2.

The peak negative voltage reached by C is a function of load current and inductance L_1. It is independent of turns ratio n. The operation taking place during the period t_3-t_4 can be best visualized by examining the elementary circuit of Figure 13.19.

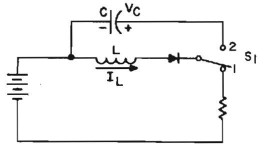


FIGURE 13.19 CAPACITOR VOLTAGE BOOSTING

Prior to throwing switch S_1, I_L current is flowing in the inductor L. The energy stored in L is ½ LI_L^2. After the switch is changed from position 1 to 2 the energy which was in L must be transferred to the capacitor, C. Thus:

$$\tfrac{1}{2} LI_L^2 = \tfrac{1}{2} C V_C^2$$

$$L/C = V_C^2/I_L^2$$

$$\& \qquad V_C = I_L \sqrt{L/C} \qquad (13.1)$$

The current I_L represents the load current flowing in L_1 shown in Figure 13.17(c) prior to t_3.

Since $V_{C(t_4)}$, in general, is greater than E_b, D_2 is again forward biased and current now flows as shown in Figure 13.17(e). The capacitor voltage is now resonantly discharging down to a value less than E_b and the blocking voltages on SCR_1 and SCR_2 change accordingly. Zero voltage across L_2 and SCR_2 occurs when the resonating current reaches a peak at t_5. It can be seen that circuit turn-off time for SCR_2 is the time interval t_4 to t_5. The resonant discharging of C continues and only ceases at time t_6 when current ceases to flow in L_2.

Improved operation can be obtained by replacing D_2 by an SCR. The operation with SCR_3 added is shown by the dotted lines in Figure 13.18. It accomplishes two important functions; namely, it maintains the voltage on C to the $V_{C(t_4)}$ value, thus providing far greater stored energy for turn-off time purposes. Secondly it allows start-up with $V_{C(t_0)}$ charged to t$-E_b$. This is accomplished by switching on SCR_2 prior to SCR_1 to "cock" the commutating circuit. This does away with the need for depending solely on autotransformer action to charge up C during the first pulse.

13.2.4.3 Design Trade-Offs

The following information is required:

The battery voltage E_b;

The rotor current required to provide load breakaway torque, I_{CL}, if current limiting is used, otherwise the locked rotor current of the motor, I_m;

Motor time constant, t_m.

Both maximum motor current and battery voltage are key variables facing the designer who has full control of all design variables, assum-

ing a fixed motor HP requirement. Other important and interrelated variables are commutating capacitor size and SCR current and voltage requirements plus autotransformer specifications. All of the above mentioned parameters and circuit component requirements are interrelated.

The rule of thumb equation generally used for circuit turn-off time in a chopper is:

$$t_c \approx \frac{C\,E_b}{I_{CL}} \tag{13.2a}$$

However this does not take into account the circuit action of the Jones Chopper which has a boost circuit which charges the commutating capacitor voltage, V_C, to values greater than E_b. Thus Equation 13.2a becomes:

$$t_c \approx \frac{C\,V_C}{I_{CL}} \tag{13.2b}$$

where $V_C > E_b$

At current limit the boost voltage is given by Equation 13.1. Substitution of Equation 13.1 in Equation 13.2b yields:

$$t_c \approx \sqrt{L_1 C} \tag{13.3}$$

This is valid for steady state operating conditions but not during initial start-up. Dividing Equation 13.1 by E_b yields:

$$\frac{V_C}{E_b} = \frac{I_{CL}}{E_b}\sqrt{L_1/C}$$

Defining $R_{CL} = E_b/I_{CL}$ (13.4)

and $Q = V_C/E_b$ (13.5)

then $Q = \frac{1}{R_{CL}}\sqrt{L_1/C}$ (13.6)

For Q>>1 peak voltages seen by SCR's 1, 2 and 3 are approximately given by Q E_b. This relationship is given in Figure 13.20. Thus we see that the major design trade-offs revolve around selection of R_{CL}, Q, L_1 and C. Where the L_1 and C determine both circuit turn-off time for SCR_1 and circuit voltages.

Figure 13.21 gives a graphical representation of the major trade-offs. From Figures 13.20 and 13.21 the major parameters for steady state operation can be chosen. The Equations plotted in Figure 13.21 are Equations 13.3 and 13.6.

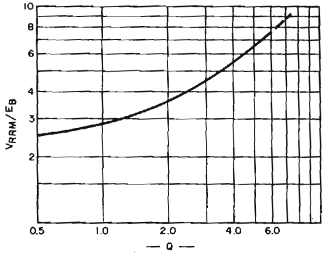


FIGURE 13.20 CIRCUIT DESIGN TRADE-OFFS

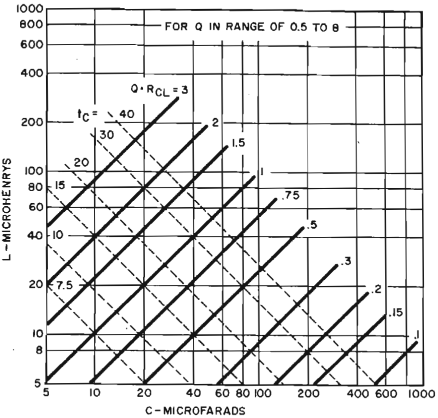


FIGURE 13.21 CIRCUIT PARAMETER RELATIONSHIPS

13.2.4.4 Design Notes

Assuming $L_1 = L_2$.

- Selection of SCR_1

The current rating of the main SCR is determined by the motor locked rotor current or the current limiting value, I_{CL}. This rule of thumb holds in practice with an adequate heat exchanger for SCR_1.

- Capacitor C and L_1, L_2

From Figure 13.20 select a Q value based upon desired maximum SCR and capacitor voltage ratings as well as supply voltage, E_b. Determine R_{CL} from the relationship in Equation 13.4.

From Figure 13.21 select L and C values for a t_c equal to twice the t_q of the main SCR, from the intersection of t_c and Q R_{CL} product. These values guarantee turn-off of the main SCR under steady state conditions with a one hundred per cent safety factor. To check start-up conditions refer to Figure 13.22.

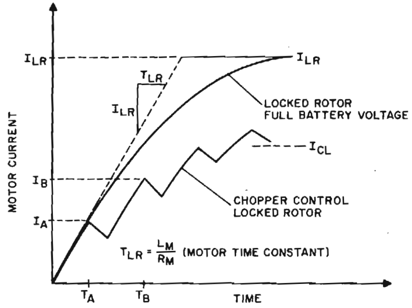


FIGURE 13.22 CHOPPER START-UP

The current I_A, at time T_A, is given by the locked rotor conditions.

$$I_A = \left(\frac{T_A}{T_{LR}}\right)(I_{LR}) \tag{13.7}$$

For 80% voltage control T_A must be 80% of the total minimum cycle time.

$$T_A \approx 4\pi\sqrt{L_1 C} \tag{13.8}$$

Commutation at I_A can be checked from Equation 13.2a.

$$t_c = \frac{C\,E_b}{I_A}$$

By substituting Equations 13.7 and 13.8 in Equations 13.2a

$$t_c = \frac{L_{LR}}{4\pi}\sqrt{C/L_1}\quad\Big|\ \text{1st Commutation}$$

or

$$t_c = \frac{L_{LR}}{4\pi\,Q\,R_{CL}}\quad\Big|\ \text{1st Commutation} \tag{13.9}$$

This equation must be satisfied for $t_c \geqq t_q$ main SCR.

During the second and subsequent commutations the current I_b is always less than twice the magnitude of the previous commutated current level. Since L_1 and C were chosen for twice the main SCR required turn-off time, the boosted voltage due to the previous current peak I_A will guarantee commutation at T_B.

Transformer T_1

Choose a 1:1 turns ratio.

If the transformer core has an air gap made up of the ends of the laminations butting together with no spacer, the number of turns may be found from the following approximate relation.

$$N_1 = N_2 = \sqrt{\frac{L_1}{6A}}$$

The core is assumed to be of the stacked type where A is the core cross sectional area in square inches and L_1 is in μH.

The choice of number of turns and core size must be checked regarding the maximum flux density in the core.

$$\text{Flux density} = \frac{15\, E_b \sqrt{L_1\, C}}{N_1\, A}$$

It is permissible to use a core which saturates provided the volt-second capability is chosen such that saturation does not occur before time t_1. The core is reset when reverse voltage is applied at time t_2.

Free-Wheeling Diode D_1

A rule-of-thumb for the maximum average current in D_1 is a quarter of the maximum motor current, I_{CL} or I_{LR}. (Assume 180° conduction angle.)

A fast recovery diode will reduce di/dt stress on SCR_1 as well as greatly reduce voltage transients that are generated by diode recovery.

Average Current in SCR_2, SCR_3, C and L_2

The same average current flows in all four components.

$$I_{avg} = f\,(C\, E_b + 2\, I_{max} \sqrt{L_1\, C}) \times 10^{-6} \text{ amps average}$$

where $I_{max} = I_{LR}$ or I_{CL}

RMS Current in L_1

A rule-of-thumb for the RMS current in winding L_1: half the motor current I_{max}.

Voltage Rating of SCR_1, SCR_2, D_1, and C

The peak forward and reverse blocking voltage across SCR_1 and SCR_2, the peak reverse voltage across D_1, and the peak voltage across C are found from Figure 13.20.

Voltage Rating of SCR_3

$$C_{PK(SCR3)} = \frac{N_2}{N_1} V_{PK(SCR1)}$$

SCR Dynamic Characteristics

SCR_1:

$$dv/dt = \frac{I_{max}}{C} \text{ volts per } \mu s$$

$$\text{Initial } di/dt \doteq \frac{E_b}{L_1} \text{ amps per } \mu s$$

Circuit Turn-off time t_c obtained from Figure 13.21.

SCR_2:

$$dv/dt = \frac{V_{PK(SCR)1}}{\sqrt{L_2\, C}} \text{ volts per } \mu s$$

$$\text{Initial } di/dt = \frac{V_{PK(SCR)1}}{\text{Stray Inductance in Loop Formed by } SCR_1,\ SCR_2 \text{ and } C}$$

Circuit turn-off time for SCR_2 depends on trigger circuit timing. It may be made several times SCR_1 available circuit turn-off time.

SCR_3:

$$dv/dt = \frac{V_{PK}\,(SCR_1)}{L_1} R_{snubber}$$

$$di/dt = di/dt \text{ of } SCR_1$$

Circuit turn-off time for $SCR_3 \geqq 4 \times t_{c(SCR_1)}$

13.2.4.5 Worked Example

Given: $E_b = 24$ volts

$I_{LR} = 160$ amps

$L_m = 80\ \mu$henrys

Selection of SCR_1

The GE C364 has an RMS rating of 180 amps. The SCR turn-off time t_q, is 10 μs.

Capacitor C and L_1

Assume a Q of 5. Then maximum SCR voltage ratings equal 6.3 × 24 volts or 152 volts, use 200 volt devices.

$$R_{LR} = \frac{24\text{ V}}{160\text{ A}} = 0.15 \text{ ohms and } Q\,R_{LR} = 0.75$$

From Figure 13.21 C and L_1 are respectively 40 μfd and 20 μh, allowing for a two to one turn-off time margin to enable commutation of maximum motor current changes between subsequent cycles.

Checking commutation at first pulse, from Equation 13.9

$$t_c = \frac{80 + 20}{4\pi\,(.75)} \geqq 10.6\ \mu s$$

$$> t_q$$

Had the basic circuit been used with a diode in place of SCR_3, the value of C would be:

$$C = 1.2 \left(\frac{t_{off}\, I_m}{E_b}\right)$$

$$C = 1.2 \left(\frac{10\,(160)}{24}\right) = 80\ \mu fd$$

It is seen that capacitor requirements are greatly reduced by the addition of one SCR and operation at high operating voltages.

Transformer T_1:

$$L_1 = L_2 = 20\ \mu h$$

$$N_1{}^2A = \frac{20}{6} = 3.2$$

If a core of 0.50 square inch cross sectional area is used, then:

$$N_1 = N_2 = \sqrt{\frac{3.2}{.50}} = 3 \text{ turns}$$

$$\text{Flux Density} = \frac{15 \times 24\sqrt{40 \times 20}}{3 \times .50}$$

$$= \frac{15 \times 24 \times 89}{1.5} = 21{,}400 \text{ lines per square inch}$$

With this flux density any of the silicon steel materials will do for the core.

Free-Wheeling Diode D_1

$$\frac{I_{CL}}{4} = \frac{160}{4} = 40 \text{ average amperes}$$

Average Current in SCR_2, SCR_3, C and L_2

$$I_{avg} = 2800\,[40 \times 24 + 160 \times 2\sqrt{40 \times 40}] \times 10^{-6}$$

where $f = 1/T_A$

$$= 28.2 \text{ amperes average}$$

RMS Current in L_1

$$\frac{I_{LR}}{2} = 80 \text{ amps RMS}$$

Voltage Rating of SCR_1, D_1, and C

From Figure 13.20, for $Q = 5$

$$V_{RRM}/E_B = 6.5$$

$$\therefore \quad V_{RRM} = 156 \text{ volts}$$

Voltage Rating of SCR_3

$$V_{pk(SCR_3)} = (1)\,(156 \text{ volts}) = 156 \text{ volts}$$

SCR Dynamic Characteristics

SCR_1:

$$dv/dt = \frac{160}{40} = 4 \text{ volts}/\mu\text{second}$$

Initial $di/dt = 156/20 = 7.8$ amperes/μsecond

Circuit turn-off time, t_c, from Figure 13.

$t_c \approx 20$ μseconds

SCR_2:

$$dv/dt = \frac{156}{\sqrt{40 \times 20}} \text{ volts}/\mu\text{second} = 5.5 \text{ volts}/\mu\text{second}$$

$$\text{Initial } di/dt = \frac{156}{\text{Estimated at } 2\ \mu\text{henry}} = 78 \text{ amperes}/\mu\text{second}$$

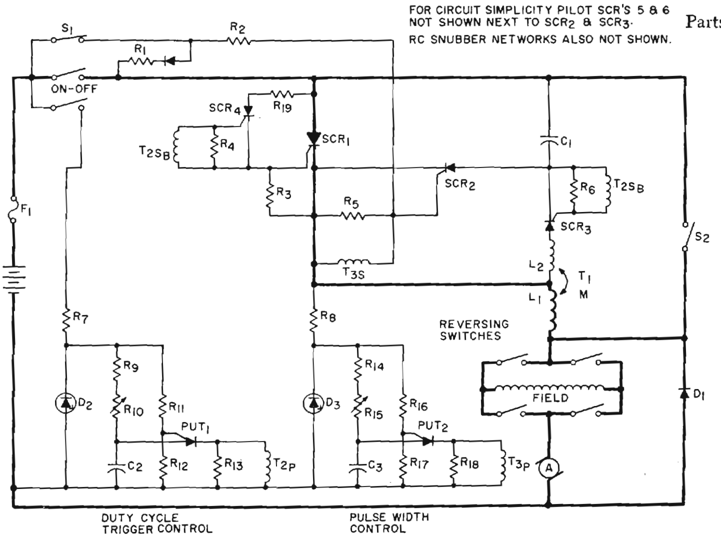
$$\text{Minimum } t_c = \pi/2\sqrt{L_2 C}\ \mu\text{second} = 45\ \mu\text{seconds}$$

SCR_3:

$$dv/dt = (156/20) \cdot 20 = 156 \text{ volts}/\mu\text{second}$$

$$di/dt = di/dt\ SCR_1 = 7.8 \text{ amperes}/\mu\text{second}$$

Circuit turn-off time t_c = minimum of $4 \times t_{c(SCR_1)}$ = 80 μseconds



Parts List:

- SCR_1 – C364C
- SCR_2, SCR_3 – C147
- D_1 – 1N3912
- D_2, D_3 – Z4XL18
- PUT_1, PUT_2 – D13T1
- SCR_4, SCR_5, SCR_6 – C106C
- R_1 – 1K 1W
- R_2 – 100 1W
- R_3, R_5, R_6 – 47 ohms, 1W
- R_4 – 1K, ½W
- R_7, R_8 – 220 ohms, 2W
- R_9, R_{14} – 27K, 1W
- R_{10} – 150K Pot (Speed Control)
- R_{11}, R_{16} – 2.2K 1W
- R_{12}, R_{17} – 3.9K 1W
- R_{15} – 20K Pot (Pulse Width Control)
- R_{13}, R_{18} – 100 ohm, 1W
- R_{19} – 27 ohm, 1W
- C_2, C_3 – 0.01 μfd, 100 Volt
- C_1 – 40 μfd, GE 28F5117
- T_1 – See Text
- T_2, T_3 – Pulse Engineering Type PE 2229
- S_1 – On-Off & Start Control
- S_2 – Bypass Switch
- F_1 – 250 Amp, 200 Volt DC Fuse

FIGURE 13.23 COMPLETE CHOPPER CIRCUIT

13.2.5 Pulse Width Modulated (PWM) Inverter

Pulse width modulation is a technique used to eliminate or reduce unwanted harmonic frequencies when inverting DC voltage to sinewave AC. One version of the PWM technique is illustrated in Figure 13.24 where the dashed wave represents the fundamental component which is obtained by inverting the DC supply voltage at a high frequency while modulating the width of each pulse. The result is an output voltage that is easily filtered to produce a sinewave. The high chopping frequency results in small lightweight magnetic components since iron size is inversely proportional to frequency.

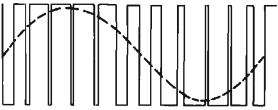


FIGURE 13.24 PWM VOLTAGE

The PWM inverter finds use in the following applications:

- UPS, uninterruptible power supplies for stand-by power source for computers, medical equipment, etc.
- AC motor speed control where the variable voltage/variable frequency capability is utilized.
- Lightweight sinewave inverter such that the high chopping frequency results in small lightweight magnetic components.

The SCR must conduct a current waveshape comprised of pulses which are modulating in both height and width. A computer program is used to determine SCR current capability for any PWM waveshape and circuit operating conditions.

13.2.5.1 The Auxiliary Commutated Inverter (Class D)

The auxiliary commutated inverter, discussed by McMurray[1.1] is one of the circuit techniques used to generate a PWM voltage. A discussion of the advantages of the auxiliary commutated PWM inverter can be found in Reference 1.2 of Section 13.6. These include:

- High operating frequency capability resulting in small, lightweight filter components.
- Variable frequency capability.
- Excellent voltage regulation capability.
- Low no-load losses.
- Low commutation energy loss.

The basic inverter circuit of Figure 13.25 can be used in either the half bridge or full bridge configurations of Figure 13.1. The half bridge single phase configuration requires a center-tapped DC supply as traded-off against the full bridge with twice as many power semiconductors. Peak to peak output voltage of the full bridge configuration is twice that of the half bridge, eliminating the need for voltage trans-

formation in some applications. The basic inverter circuit can be used as a building block for the three-phase circuit of Figure 13.1.

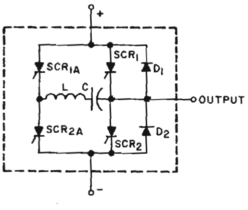


FIGURE 13.25 BASIC CIRCUIT AUXILIARY COMMUTATED INVERTER

A detailed discussion of the theory of operation is contained in Reference 1.1 of Section 13.6. Briefly, SCR_1 is the main SCR whose task it is to deliver current from the DC supply to the load. SCR_{1A} is the commutation SCR which forces the current in the main SCR to zero by an impulse current discharge of the L-C components. By controlling the ratio of ON to OFF time of the main SCR, SCR_1, the desired PWM voltage will appear at the output.

Waveshapes of current and voltage for the main and auxiliary SCR's are shown in Figure 13.26.

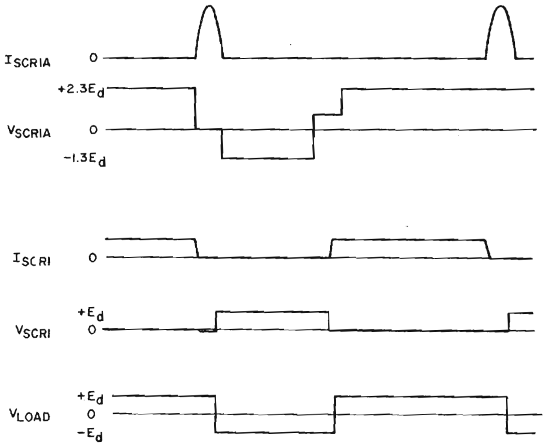


FIGURE 13.26 WAVESHAPES FOR FULL BRIDGE CIRCUIT

13.2.5.2 Design Notes

The auxiliary SCR, SCR_{1A}, must be capable of conducting a high peak, narrow pulse current wave. This indicates the need for a field-initiated gate structure. The reader is referred to Chapter 1 for a discussion of the FI gate and its derivatives.

To achieve adequate commutation of the main SCR, the L-C discharge current must exceed the load current, I_L, for an interval t_c which is longer than the turn-off time of the main SCR, t_q. The optimum impulse current waveshape, that requiring the least amount of energy, occurs for $I_p = 1.5\ I_L$, as in Figure 13.27. The width of the commutating current pulse, t_{pw}, is determined by the resonant components.

$$\omega = 2\pi f = \frac{2\pi}{2\ t_{pw}} = \frac{\pi}{t_{pw}}$$

$$t_{pw} = \pi \sqrt{LC}$$

The commutation components can then be expressed in terms of turn-off time of the main SCR.

$$\sqrt{LC} = .6\ t_q$$

Therefore an SCR with low t_q will be chosen in order to minimize the commutation components, L and C.

The ratio of peak commutation capacitor voltage, E_C, and I_p can be approximated as

$$\sqrt{\frac{L}{C}} = \frac{E_C}{I_p}$$

The commutation capacitor and inductor are then determined as

$$C = \frac{.6\ t_q\ I_p}{E_C}$$

$$L = \left(\frac{E_C}{I_p}\right)^2 C = \frac{.6\ t_q\ E_C}{I_p}$$

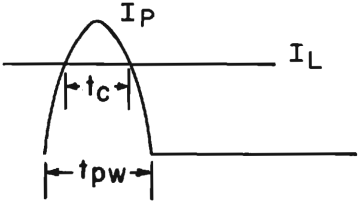


FIGURE 13.27 COMMUTATION CURRENT PULSE

The blocking voltage requirement of the commutation thyristor, SCR_{1A}, is dependent on the capacitor voltage, E_C.

$$E_C = E_d + \left[X I_L \sin \omega t_2 - (Ed - E_1) \cos \omega t_2 \right] \exp\left[-\frac{\omega t_2}{2Q} \right]$$

where
E_d = DC supply voltage
$X = \sqrt{L} / \sqrt{C}$
I_L = Load current
ω = Approximately $(LC)^{-\frac{1}{2}}$
t_2 = Portion of commutation interval
E_1 = Initial capacitor voltage at start of time t_2
$Q = X/R$

The above equation for E_C is derived and plotted in Reference 1.1 of Section 13.6. As an approximation the peak capacitor voltage can be expressed as

$$E_C = 2.5\ E_d$$

Actual performance can then be experimentally determined.

13.2.5.3 Design Example

Required output: 110 volts RMS
400 Hertz sinewave
400 A peak load current

The main SCR is chosen for fast turn-off time in order to minimize commutation component size. The C395 is capable of conducting the load current with a maximum turn-off time of 20 microseconds, under severe test conditions.

Choose chopping frequency of 2 kHertz

$$\frac{2000\text{ Hz}}{400\text{ Hz}} = 5{:}1$$

Commutation components are determined by the impulse current required.

$$I_p = 1.5\ I_L$$
$$= 600 \text{ amperes peak}$$

For turn-off time of the main SCR of 20 microseconds

$$t_{pw} = 2\ (20\ \mu\text{seconds})$$
$$= 40\ \mu\text{seconds}$$

The C358 SCR is chosen to meet the current requirements of a 600 amp peak half sinewave of 40 microsecond pulse width operating at 2 kiloHertz.

$$\text{initial } di/dt = \frac{\pi I_p}{t_{pw}}$$
$$= 50 \text{ amperes per microsecond, repetitive}$$

The DC supply voltage is estimated to be

$$E_d = \frac{110\ \pi}{2\sqrt{2}}$$
$$= 125 \text{ volts DC}$$

The commutation SCR blocking voltage is chosen to be three times the supply voltage. Peak capacitor voltage, E_C

$$E_C = 2.5\ E_d$$
$$= 300 \text{ volts}$$

The commutation capacitor can then be determined.

$$C = \frac{.6\ t_o\ I_p}{E_C}$$
$$= \frac{.6\ (20\ \mu s)\ (600\ A)}{300\ V}$$
$$= 24\ \mu\text{Farad}$$

From the capacitor selection chart in Chapter 5 select 28F5116, a 30 μFarad capacitor. The commutation inductance size is calculated

$$L = \frac{E_C^2}{I_p}(C)$$
$$= \frac{(300\ V)^2}{(600\ A)^2}(30\ \mu F)$$
$$L = 7.5\ \mu H$$

RC snubber network values depend on stray inductance and source impedance, thus may be determined experimentally.

Fast recovery A396 diodes are used in order to minimize reverse recovery currents, power dissipation, and voltage transients.

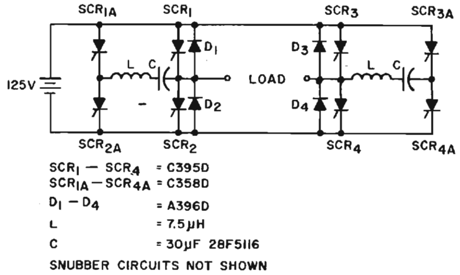


FIGURE 13.28 SINGLE PHASE CIRCUIT

13.3 INVERTER ACCESSORIES

In practical applications of inverters it is often necessary to modify the design to accommodate one or more of the following requirements:

1. The ability to operate into inductive loads
2. Over-current protection
3. Open-circuit operation
4. Sine wave output
5. Regulated output

13.3.1 The Ability to Operate Into Inductive Loads

When an inverter sees a reactive load as opposed to a purely resistive load several changes occur in the operation of the inverter. Without attention, a reactive load can cause high voltage transients to exist in the inverter resulting in loss of efficiency and power and jeopardizing the components.

Consider Figure 13.29. Assume that SCR_1 is conducting. Current is flowing in the primary of the transformer as shown by arrow "a" and in the load by "b". When SCR_1 is turned off, current "b" still needs to flow. If no path were provided in the primary, the voltage would rise excessively.

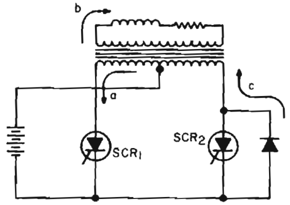


FIGURE 13.29 FLOW OF REACTIVE CURRENT

A convenient means of providing a current path is to place a diode across SCR_2. Now current "c" can flow and this is magnetically the same path as current "a". The dv/dt that the circuit applies to the SCR is greatly increased. Figure 13.30 shows the effect of a diode across the SCR on the voltage waveform. In Figure 13.30(b) it is seen that the voltage across the SCR is held at a low negative value while current is flowing through the diode. When the diode ceases to carry current, the voltage across the SCR suddenly snaps up to a high value. As the rise time is commonly less than 1 μs, the value of dv/dt can be very high. Where possible, it is preferable to avoid placing the diode directly across the SCR. The circuit of Figure 13.10 for example shows how an inductor can be used between the SCR and the diode. By this means both the high values of dv/dt and the low amount of reverse voltage can be avoided.

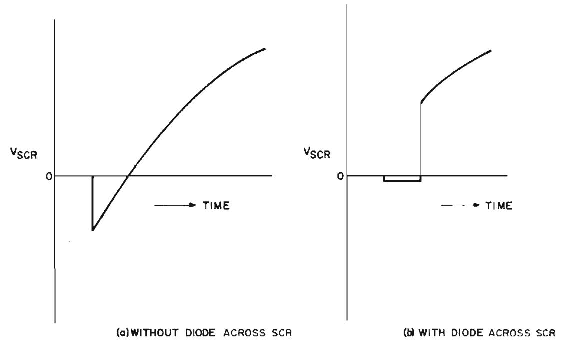


FIGURE 13.30 VOLTAGE WAVEFORM ACROSS THE SCR

13.3.2 Overcurrent Protection

If the load current in an inverter is increased beyond the rated output, some means must be provided for the protection of the components. The following methods may be considered.

13.3.2.1 Fuses and Circuit Breakers in the DC Supply

This, the most obvious of steps, has the advantage of simplicity. It is however necessary to match the overload capabilities of the SCR with the current-time rating of the fuses or circuit breakers. Thus the I^2t rating of the SCR must be greater than that of the fuse. This is complicated by the fact that the I^2t rating of the SCR drops substantially during the SCR turn-on time, and fuses or circuit breakers do not afford very good protection in this short time.

Another snag is the location of the fuse in the DC supply. Invariably a ripple current due to the load current flows in the DC supply. Thus the fuse will see a relatively high RMS current and may, in the case of high frequency inverters, have to be derated because of skin effect. If on the other hand a large filter capacitor is placed between the fuse and the inverter to carry the ripple current then the fuse does not isolate the SCR from the energy in the capacitor.

13.3.2.2 Current Limiting by Pulse-Width Control

The inverter components may be protected by sensing the output current and using this information to narrow down the pulse width when the output current exceeds the rated value. With a very heavy

load the current pulses then become narrow and have a high amplitude. The circuit is then liable to present short values of turn-off time and high values of di/dt to the SCR. If the load is distributed to more than one piece of apparatus, there may not be enough current in the case of a current limited supply to blow the local fuse where a short circuit occurs.

13.3.2.3 Current Limiting by LC Resonance

The bridge circuit in the output lead of the inverter in Figure 13.31 is in series resonance at the output frequency. If the Q of the capacitors and inductors is high, the overall efficiency of the inverter will not be appreciably changed.

In the event of a current overload a fast acting switch is connected between points A and B. The bridge circuit then becomes a parallel resonant circuit at the operating frequency and the impedance to the load current becomes very high.

The fast-acting switch may be either a saturating reactor or one of the forms of SCR AC switches described in Chapter 8.

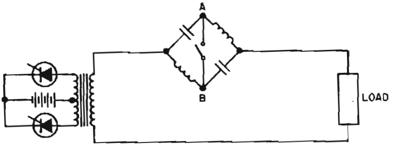


FIGURE 13.31 CURRENT LIMITING BY RESONANCE

13.3.2.4 Current Limiting in Class A Circuits by Means of Series Capacitors

Class A circuits such as Figure 13.32 can be made current limiting by connecting a capacitor C_1 in series with the load R. See Figure 13.32. The value of capacitor is chosen so that, when the load is shorted, the resonant frequency of the LC circuit is still appreciably greater than the triggering frequency. Figure 13.33 shows a typical curve of load current versus load voltage.

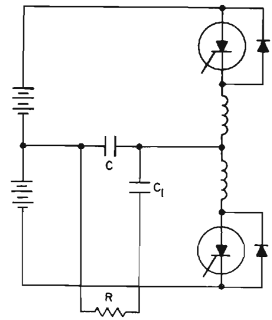


FIGURE 13.32 CURRENT LIMITING IN A CLASS A INVERTER CIRCUIT

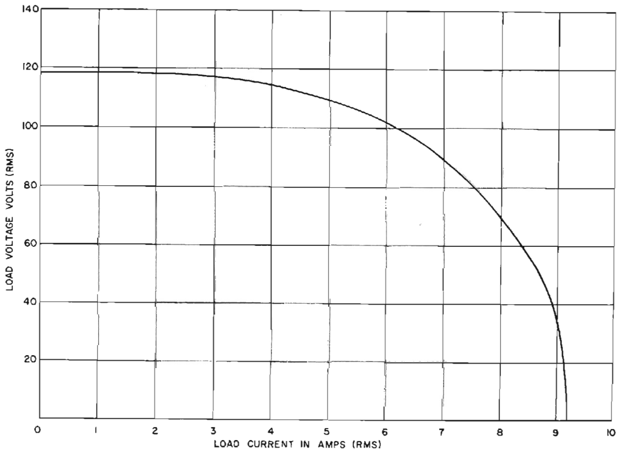


FIGURE 13.33 LOAD REGULATION CURVE OF A CURRENT LIMITING CLASS A INVERTER

13.3.3 Sine-Wave Output

Most applications of DC to AC inverters prefer a sine-wave rather than a square wave output. In conflict with this we are faced with the fact that the SCR is essentially a switch and switching a battery gives square waves. In fact the great efficiency with which SCR inverters

operate is mainly due to the fact that the SCR switches at high speed from the fully-off to the fully-on mode.

Sine-wave output-waveforms may be obtained from SCR inverters by the following approaches:

1. Resonating the load
2. Harmonic attenuation by means of an LC filter
3. An LC filter plus optimum pulse-width selection
4. Synthesis by means of output voltage switching
5. Synthesis by control of the relative phase of multiple inverters
6. Multiple pulse width control
7. Selected harmonic reduction
8. Cycloinversion

13.3.3.1 Resonating the Load

The waveform in the load may be made sinusoidal by inserting the load in a resonant circuit of a Q high enough to achieve the desired harmonic content. A typical circuit using this approach is found in Class A inverters. Owing to the large size of the LC components this circuit only becomes attractive above about 400 Hz.

13.3.3.2 Harmonic Attenuation by Means of an LC Filter

This filter can take many forms. The most attractive is that by Ott described in Reference 3.9 of Section 13.6. The circuit is shown in Figure 13.12(a). The Ott filter has the following very desirable characteristics:

1. Good voltage transfer characteristics.
2. Attenuation independent of the load.
3. The input impedance can be designed to be capacitive over the working load range.

For details see the Class C inverter example in Sections 13.2.3.1 and 13.2.3.2.

13.3.3.3 An LC Filter Plus Optimum Pulse Width Selection

The requirements of the LC filter can be appreciably reduced by using a narrower pulse width than 180°. Thus a 120° pulse has zero third harmonic distortion. See Figure 13.34.

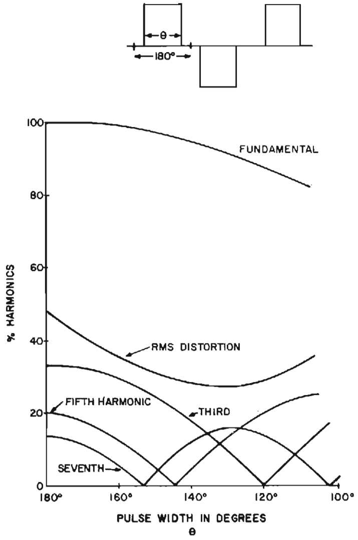


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FIGURE 13.34 HARMONIC CONTENT VERSUS PULSE WIDTH WITH RECTANGULAR WAVEFORMS

13.3.3.4 Synthesis by Means of Output-Voltage Switching

The output from an inverter is coupled through a transformer (Figure 13.35) to the load via SCR "tap switches". The appropriate SCR is triggered to give the output waveform shown in Figure 13.36. The inverter operates, in this case, at five times the output frequency. This waveform is easily filtered to give a good sine wave output.

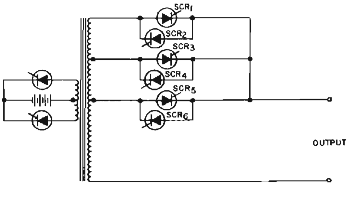


FIGURE 13.35 OUTPUT VOLTAGE SWITCHING CIRCUIT

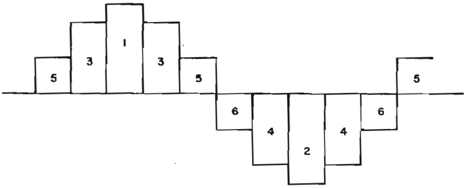


FIGURE 13.36 WAVEFORM WITH OUTPUT VOLTAGE SWITCHING

13.3.3.5 Synthesis by Controlling the Phase Relationship of Multiple Inverters

The basis of this method of harmonic reduction is to add the outputs of a multiplicity of inverters to form a quasi sine wave which has no low-order harmonic component. The remaining high-order harmonics are easily filtered.

Figure 13.37 shows an outline of a three phase bridge inverter circuit. The voltages across outputs a, b and c are shown in Figure 13.38(a) and the line-to-line voltage across the output transformer is shown in Figure 13.38(b). If more phases are used the steps in the waveform become smaller giving an even lower harmonic content.

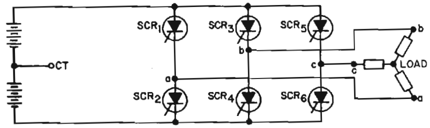
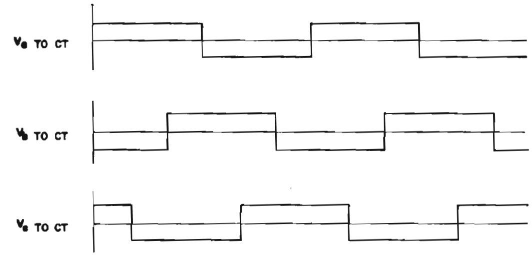
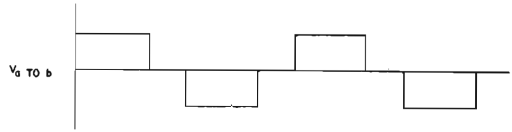


FIGURE 13.37 THREE PHASE BRIDGE INVERTER CIRCUIT



(a)

FIGURE 13.38 THREE PHASE BRIDGE WAVESHAPES



(b)

FIGURE 13.38 THREE PHASE BRIDGE WAVESHAPES

13.3.3.6 Multiple Pulse Width Control

This method of achieving a sine wave output is obvious from Figure 13.39. This waveform may be obtained from a bridge circuit (Figure 13.37). One pair of SCR's is triggered and turned off with various pulse widths to form the positive half cycle and then the other pair is operated similarly for the negative half cycle.

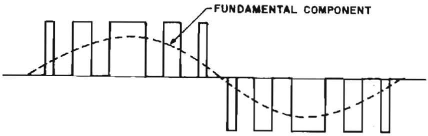


FIGURE 13.39 OUTPUT WAVEFORM USING MULTIPLE PULSE WIDTH CONTROL

13.3.3.7 Selected Harmonic Reduction

The circuit in Figure 13.14 is triggered so as to give a load waveform as shown in Figure 13.40. With precise control of the pulse widths the output wave-shape can be made low in 3rd and 5th harmonic content.

The advantages of this method over other methods of synthesis are:

1. The fundamental output may be varied from zero to maximum amplitude without re-introducing the harmonic voltages.
2. A three-phase circuit using only twelve SCR's can eliminate all the harmonics below the eleventh while still being able to control the fundamental frequency from zero to maximum.
3. The triggering circuitry is considerably simplified.

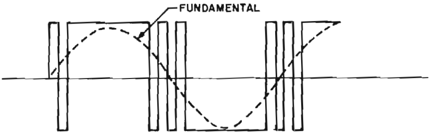


FIGURE 13.40 OUTPUT WAVEFORM WITH SELECTED HARMONIC REDUCTION

13.3.3.8 The Cycloinverter

A cycloinverter consists of an inverter, operating at about ten times the desired output frequency, to which is coupled a cycloconverter (see Section 13.5) producing the desired output frequency waveform and amplitude.

13.3.4 Regulated Output

Most inverter customers specify that the inverter output be regulated both for input voltage and load current variations.

The inverter designer has three choices:

1. To regulate the supply voltage to the inverter
2. To regulate within the inverter
3. To regulate the output of the inverter

13.3.4.1 Supply-Voltage Regulation

If the supply is a battery, fuel cells or some other DC supply, then the pre-regulation takes the form of a regulated DC to DC converter, the logic for the DC to DC converter coming from the output of the inverter, Figure 13.41.

The DC to DC regulated supply can take many forms. If the inverter supply is from a rectified AC line, then pre-regulation can be achieved by substituting phase controlled SCR's for the rectifier diodes. The logic for the triggering circuits is again supplied from the output of the inverter, Figure 13.42. Phase controlled rectifiers are discussed in Chapter 9.

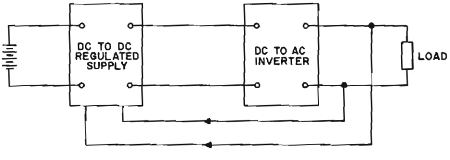


FIGURE 13.41 DC SUPPLY VOLTAGE REGULATION

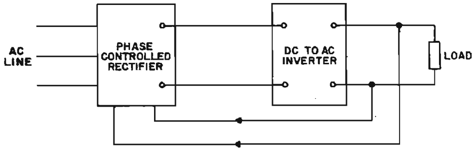


FIGURE 13.42 AC SUPPLY VOLTAGE REGULATION

13.4 PULSE MODULATOR SWITCHES

The semiconductor switch in a pulse modulator circuit is required to discharge a capacitor extremely fast, through a noninductive path. A specially characterized pulser SCR is needed to conduct the resulting high amplitude, fast-rising current pulse. Pulse widths vary from .1 μsecond to 10 μseconds in applications such as radar modulators and laser pulsers, as in the circuit of Figure 13.43.

If turn-off time is not a critical characteristic of the SCR because of the low repetition rate, advantage can be taken of the SCR design trade-off existing between turn-off and turn-on capabilities. See Chapter 1 for discussion of gold doping. Pulser SCR's designed specifically for superior turn-on characteristics are capable of fast turn-on, low turn-on power dissipation, and extremely high di/dt capability.

Airborne radar, with its higher frequency requirements, necessitates an SCR with both fast turn-on and fast turn-off capabilities. High frequency SCR's such as the C141 and C144 make ideal pulse modulator switches for high frequency applications.

In order to achieve high di/dt capability the gate of the SCR should be driven as hard as the ratings permit. The rise time of the gate pulse should be less than .1 μsecond.

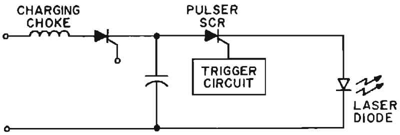


FIGURE 13.43 LASER PULSER CIRCUIT

13.5 CYCLOCONVERTERS

A cycloconverter is a means of changing the frequency of alternating power using controlled rectifiers which are AC line (Class F) commutated. The cycloconverter is thus an alternative to the frequency changing system using a rectifier followed by an inverter.

13.5.1 Basic Circuit

The method of operation is readily understood from Figure 13.44. A single-phase full-wave rectifier circuit is equipped with two sets of SCR's, which would give opposite output polarities. Thus if SCR_1 and

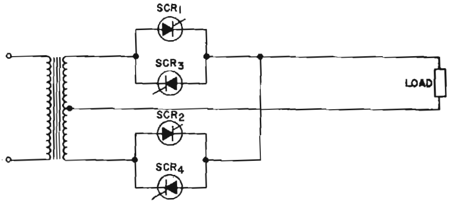


FIGURE 13.44 SINGLE PHASE CYCLOCONVERTER

SCR_2 are triggered the DC output would be in the polarity shown on the left side of Figure 13.45. If SCR_3 and SCR_4 were triggered instead, the output polarity would be reversed as shown. Thus, by alternately triggering the SCR pairs at a frequency lower than the supply frequency a square wave of current would flow in the load resistor. A filter would be needed to eliminate the ripple.

In order to produce a sine wave output, the triggering of the individual SCR's would have to be delayed by varying degrees so as to produce the waveform shown in Figure

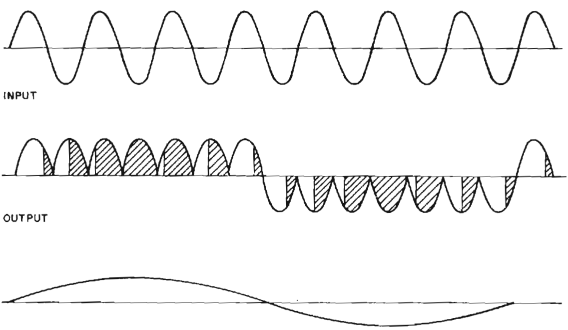


FIGURE 13.45 SINGLE PHASE CYCLOCONVERTER WAVEFORMS

13.5.2 Polyphase Application

The SCR cycloconverter is important in two applications. In the variable-speed, constant-frequency system an alternator is driven by a variable-speed motor such as an aircraft engine, yet the required output must be at a fixed and precise frequency such as 400 Hz.

A second application is where the required output must be variable in both frequency and amplitude for driving an induction or synchronous motor. This makes possible variable speed brushless motors which could for example be used to drive the wheels of vehicles operating in difficult environments.

Due to the advantages in AC motor design, most of the cycloconverter systems are polyphase. Figure 13.46 shows a typical schematic (excluding the trigger circuit).

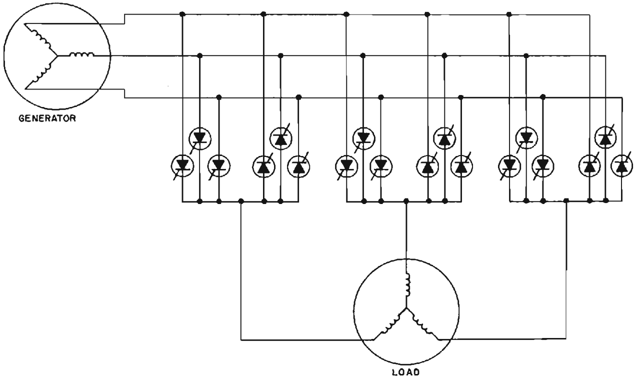


FIGURE 13.46 THREE PHASE CYCLOCONVERTER CIRCUIT

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14 LIGHT ACTIVATED THYRISTOR APPLICATIONS

Light, or more precisely, electromagnetic radiation, with wave length between 0.2 and 1.4 microns, is increasingly being used in conjunction with solid state devices. The use of light offers a convenient method for sensing the absence or presence of an opaque object and for achieving electrical isolation. These features are useful in the control of power devices and will be discussed in this chapter. Opto-electronic devices also find usage in communications, and other applications beyond the scope of the Manual.

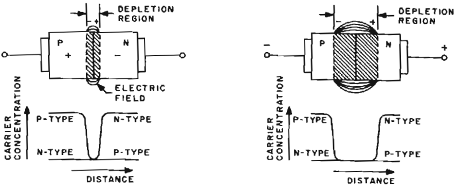
14.1 LIGHT ACTIVATED SEMICONDUCTORS

There are many types of devices available for converting radiant energy into electrical information. These devices may convert the radiant information into a variable resistance, such as occurs in photo resistive elements such as cadmium sulfhide, cadmium selenide and lead sulfhide, or into a generated voltage and current as in photo voltaic cells of selenium, silicon and germanium. The newer types of light sensitive devices are semiconductor junction devices. Included in this group are light activated diodes, transistors, and thyristors. It is to this last group of devices which we will direct our attention.

Radiant energy incident on a semiconductor (such as silicon, germanium, cadmium, sulfhide or selenium) causes the generation of hole-electron pairs. These free charges create a change in the electrical characteristics of the semiconductor. In a photo cell they cause a decrease in resistance, in the photo-voltaic cell they create a voltage and in a junction device, under bias, cause currents to flow across the exposed junctions. In a photo thyristor this current is equivalent to gate current, whereas in a photo transistor the light causes an equivalent base current.

14.1.1 Photo Diode (Light Sensitive Diode)

In a conventional p-n junction without external bias, a very thin depletion region is formed where electrons from the n-type material move across the junction and combine with holes in the p-type material. The positive ions so created in the n-type material and the negative ions in the p-type material build up an electric field.

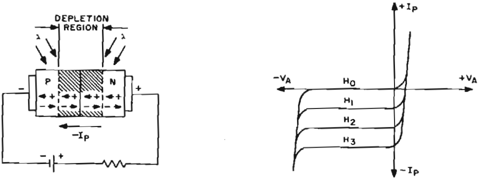


(a) Without Bias (b) Reverse Biased

FIGURE 14.1 PN JUNCTION AND CARRIER CONCENTRATION

In a reverse biased p-n junction, the width of this depletion region will increase proportionally with applied voltage (capacitance will decrease with higher voltage). Electrons which attempt to enter the p-type material are too low in energy to cross the potential barrier and the current will be almost zero. Some electrons will be excited by thermal energy to an extent that hole electron pairs are created which will be swept across the junction as leakage current by the existing field of the depletion region.

If light (electromagnetic radiation) with the proper wave length is directed toward the reverse biased p-n junction, absorbed photon energy will also create hole electron pairs and enable the electrons to move across the depletion region. Additional current proportional to the light intensity will flow across the reverse biased junction.



(a) Hole Electron Pairs in Reverse Biased Light Sensitive PN Junction (b) VI Characteristic of Light Sensitive Reverse Biased PN Junction

FIGURE 14.2

$$-I_p = \eta \cdot q \cdot \Phi \cdot A \cdot \frac{\tau}{t_r} = \text{current through junction}$$

η = Quantum Efficiency
q = Electron Charge = 1.602×10^{-19} Coul.
Φ = Photon Flux Density in Photons/sec-cm^2
A = Area in cm^2
τ = Lifetime of Free Carrier
t_r = Transit Time of These Carriers

Since for a photo diode with sufficient reverse bias, the carriers are swept across the depletion region before they have a chance to recombine, $\tau = t_r$ and the above equation will become

$$-I_p = \eta \cdot q \cdot \Phi \cdot A$$

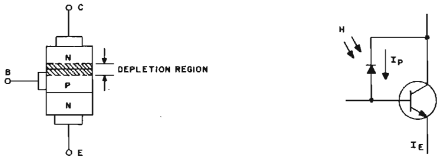
Frequency response will be influenced by capacitance of the depletion region, drift time in the depletion region and the diffusion of carriers. Carriers generated outside the depletion region must diffuse toward the depletion region and considerable time delay will be introduced. To overcome this delay, the depletion region should be close to the surface of the device.

Higher efficiency will result by increasing the width of the depletion region (low capacitance) and higher reverse bias. The depletion region must not be too wide, however, or transmit-time effect will limit the frequency response; neither should it be too thin or the capacitance will increase.

Most parameters of a photo diode can be influenced by selecting different materials or changing diffusion concentration, mobility and lifetime of the carriers.

14.1.2 Photo Transistors

The equivalent circuit of a photo transistor is shown in Figure 14.3. A photo diode as described earlier is used as a constant current generator to supply the transistor with base current, which will be amplified by h_{FE} of the transistor.



(a) Simplified Physical Layout of Photo Transistor

(b) Photo Transistor Illustrating the Effect of Photon Current Generation

FIGURE 14.3

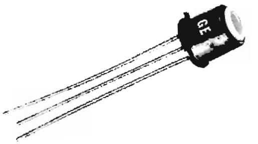
$$I_E = I_p \cdot (h_{FE} + 1)$$

I_p = current through n-p junction

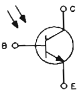
h_{FE} = transistor dc current gain

The collector-base junction of the transistor and the photo diode are one and the same but for simplicity the light sensitive junction in Figure 14.3(b) has been separated from the normal transistor.

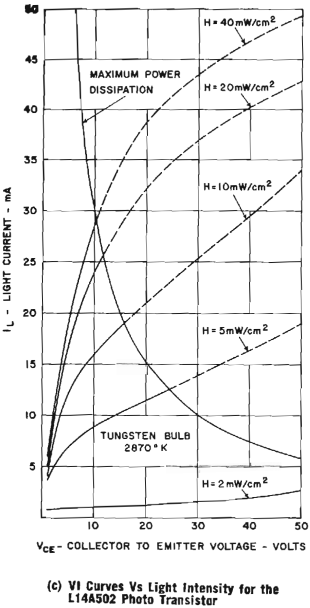
A photo transistor, like the L14A shown in Figure 14.4(a) will control a collector current of 0-50 ma at V_{CE} = 0-50 V with a total irradiance between 0-40 mW/cm^2.



(a) View of Photo Transistor



(b) Symbol



(c) VI Curves Vs Light Intensity for the L14A502 Photo Transistor

FIGURE 14.4

Switching speed is an important characteristic of this device and should be considered. For the L14A502 the delay time is about 2 μsec and rise time about 5 μsec.

Note: Response time is heavily dependent on external base-to-emitter impedance since collector-base capacitance is multiplied by Miller effect. Most significant in darlington!

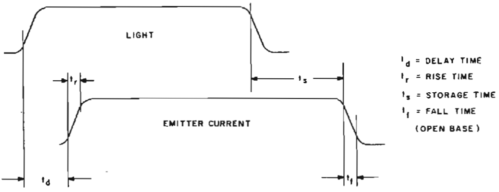
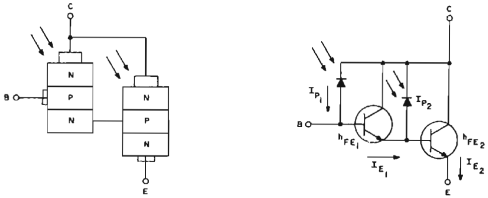


FIGURE 14.5 RELATIONSHIP BETWEEN INPUT & OUTPUT OF LIGHT SENSITIVE DEVICE

14.1.3 Photo Darlington Amplifier

Like the photo transistor, the current between collector and emitter of the photo darlington amplifier is a function of the light incident on the device. The dominant term on the output current is the product of the two betas, which accounts for the high sensitivity of the device.



(a) Simplified Physical Layout of Photo Darlington Amplifier

(b) Photo Darlington Amplifier Illustrating the Effects of Photon Current Generation

FIGURE 14.6

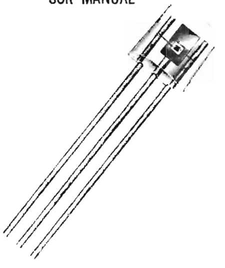
$$I_{E1} = I_{P1}\,(h_{FE1} + 1)$$
$$I_{E2} = (I_{P2} + I_{E1})\,(h_{FE2} + 1)$$
$$I_{E2} = [I_{P2} + I_{P1}\,(h_{FE1} + I_{P1})]\,[h_{FE2} + 1]$$

Because I_{P2} is small compared to I_{E1}:

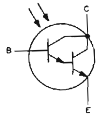
$$I_{E2} \approx I_{P1} \cdot h_{FE1} \cdot h_{FE2}$$

I_E = Emitter Current
I_p = Photon Produced Current
h_{FE} = DC Current Gain of Transistors 1 and 2

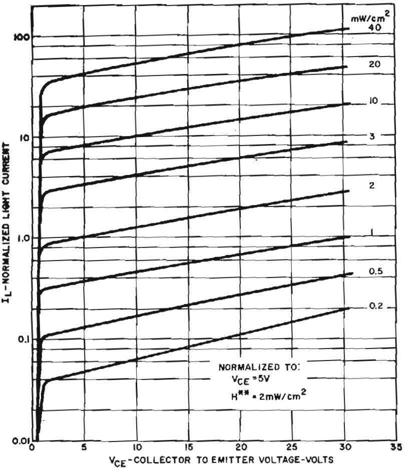
The 2N5777-2N5780 family is one example of a light sensitive darlington. Its spectral response is centered near 0.85 microns, maximum collector current is 250 mA, power dissipation 200 mW at 25°C and rise time is typically 75 μseconds. These devices can be used with or without base lead. Base bias can increase or decrease sensitivity depending on the bias polarity.



(a) View of Darlington Amplifier



(b) Symbol



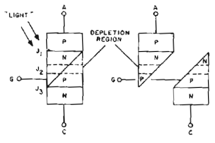
**H = RADIATION FLUX DENSITY, RADIATION SOURCE IS AN UNFILTERED TUNGSTEN FILAMENT BULB AT 2870° K COLOR TEMPERATURE.

(c) Normalized Light Current Vs Collector to Emitter Voltage

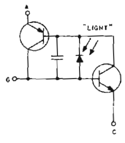
FIGURE 14.7 LIGHT SENSITIVE DARLINGTON AMPLIFIER

14.1.4 Light Activated SCR (LASCR)

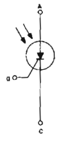
The basic operation of a light activated SCR is shown in Figure 14.8. With applied forward voltage junctions J_1 and J_3 are forward biased and they can conduct if sufficient free charge is present. Junction J_2 is reverse biased, however, and blocks current flow. Light entering the silicon creates free hole-electron pairs in the vicinity of the J_2 depletion region which are then swept across J_2 (Note: The theory developed for the photo diode and extended to the transistor can be applied here also). As light is increased the current in the reverse biased diode, Figure 14.8(c), will increase. The current gains of the n-p-n and p-n-p transistor equivalents in the structure also increase



(a) & (b) Simplified Physical Layout of LASCR



(c) LASCR Transistor Equivalent Illustrating the Effects of Photon Current Generation & Junction Capacitance



(d) Symbol of LASCR

FIGURE 14.8 LIGHT ACTIVATED SCR

with current. At some point the net current gain ($\alpha_1 + \alpha_2$) exceeds unity and the SCR will turn on. The criterion for turn-on is the same as explained in Chapter 1 but with an additional term due to the light generated current.

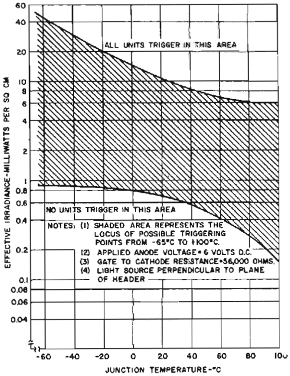
$$I_A = \frac{\alpha_2 (I_P \pm I_G) + I_{CBO(1)} + I_{CBO(2)}}{1 - \alpha_2 - \alpha_1}$$

I_P = Photon Current (Current Generated by Incident Light)
I_G = Gate Current
$I_{CBO(1)} + I_{CBO(2)}$ = Leakage Current
α = Current Gain

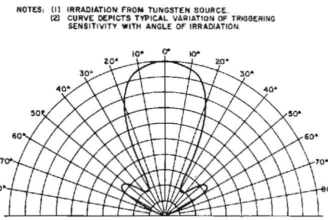
α_1 varies with $I_A + (I_p)$
α_2 varies with $I_A + (I_p \pm I_G)$
when $\alpha_1 + \alpha_2 \rightarrow 1$ than $I_A \rightarrow \infty$

In order to obtain reasonable sensitivity to light the SCR must be constructed so that it can be triggered with a very low current density. This requires the use of a fairly thin silicon pellet of small dimensions hence high current devices are not considered practical for light triggering at this time. The high sensitivity of the LASCR also causes it to respond to other effects which produce internal currents. As a result the LASCR has a higher sensitivity to temperature, applied voltage, rate of change of applied voltage, and has a longer turn-off time than a normal SCR.

Some important characteristics of the L8-L9 series light activated SCR's are shown in Figure 14.9(a)-(e).

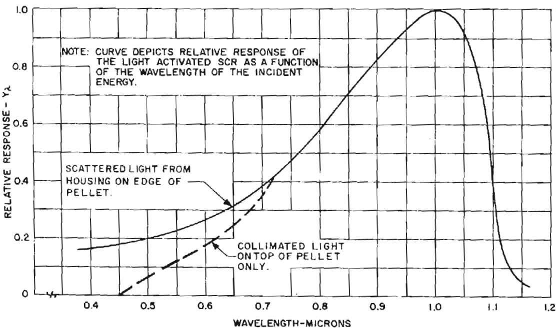


(a) Light Triggering Characteristics

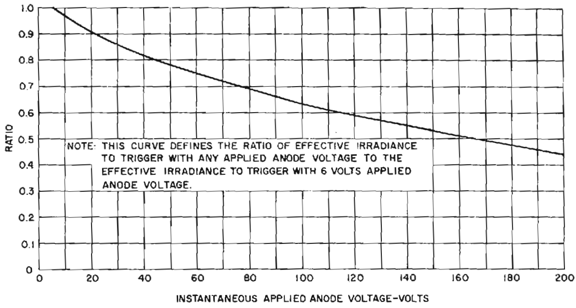


(b) Typical Angular Response

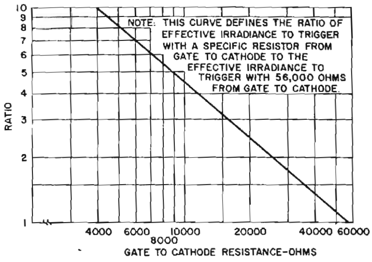
FIGURE 14.9 CHARACTERISTICS OF THE L8-L9 LASCR



(c) Typical Spectral Response



(d) Typical Variation of Light Sensitivity With Anode Voltage



(e) Typical Variation of Light Sensitivity With Gate to Cathode Resistance

FIGURE 14.9 CHARACTERISTICS OF THE L8-L9 LASCR

Figure 14.9(a) shows the relationship between effective irradiance to trigger and junction temperature. Since the triggering level is highest at the lowest junction temperature, the amount of light provided in a given system must take into account the lowest junction temperature at which operation is expected. Conversely the maximum sensitivity is obtained at maximum junction temperature. Therefore, the maximum irradiance provided by the system under conditions where the LASCR should not trigger must be less than the value given for the highest operation junction temperature.

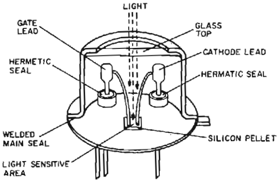
Figure 14.9(b) shows the spatial response typical of the L8 and L9 devices. Primary response is confined to an angle of $\pm 25°$ from perpendicular. Secondary responses are found at about 55° from the perpendicular. Secondary responses are produced by high reflection from the inside walls of the case. The specified effective irradiance to trigger is given for a point source of light oriented perpendicular to the plane of the silicon pellet.

Figure 14.9(c) shows the relative response of the LASCR as a function of wave length of the incident irradiation. This curve also indicates the difference in spectral response of the LASCR to direct light and scattered light. Direct radiation must penetrate a significant thickness of silicon to reach the region of J_2. Since the absorption of silicon is rather high in the visible spectrum (0.4-0.7 micron) the spectral response is rather low in this band. Scattered light from the housing reaches the vicinity of J_2 near the edge of the pellet, hence less of the shorter wave length is absorbed before reaching the junction. The result of edge radiation is higher response to the shorter wave lengths.

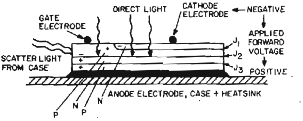
Figure 14.9(d) shows the typical variation of light sensitivity with anode voltage. At high voltages, the required irradiance to trigger becomes significantly less as a result of the effect of voltage on the gain of the equivalent transistor circuit. Since H_{ET} is normally specified with an anode voltage of 6 volts, operation at higher or lower voltages will modify this value. If the applied voltage is sinusoidal and the irradiance is increased slowly from low level, triggering will occur initially at the peak of the applied wave form. Further increase in irradiance will then advance the point of triggering to the beginning of the applied wave.

Figure 14.9(e) shows that typical light sensitivity is inversely proportional to gate to cathode resistance. The purpose of the gate cathode resistor is to bypass current around J_1, thus reducing the gain of the n-p-n transistor region to desensitize the device. The use of temperature sensitive resistors (thermistors) between gate and cathode or a forward biased silicon diode plus resistor network can provide some degree of temperature compensation against changes in sensitivity. It should be noted in Figure 14.9(a) however that the effect of temperature upon sensitivity is far from consistent from one device to the next. Therefore, it is not practical as a general rule to provide temperature compensation which will maintain light sensitivity constant over the operating temperature range.

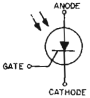
The General Electric LASCR is similar to the C5 type planar SCR except that there is a glass window on top of the package. The device is capable of handling up to 1.6 amperes RMS anode current and of blocking up to 200 volts peak.



(a) LASCR Construction



(b) LASCR Planar Pellet

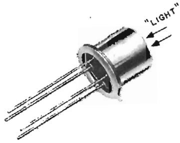


(c) LASCR Symbol

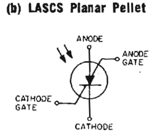
FIGURE 14.10 CONSTRUCTION OF HOUSING, PELLET & SYMBOL OF LASCR

14.1.5 Light Activated Silicon Controlled Switch (LASCS)

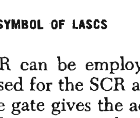
The light activated silicon controlled switch (LASCS) is another planar thyristor structure with all four semiconductor regions accessible, rather than only three as is customary with silicon controlled rectifiers. Accessibility of the fourth region greatly expands circuit possibilities beyond those of conventional transistors or SCR's. In addition, making it sensitive to light adds an entirely new dimension to the circuit design possibilities. It is probably the most versatile p-n-p-n device on the market today.



(a) View of LASCS



(b) LASCS Planar Pellet



(c) LASCS Symbol

FIGURE 14.11 HOUSING, PELLET & SYMBOL OF LASCS

The theory developed for the LASCR can be employed for the LASCS. Turn-on and turn-off techniques used for the SCR and LASCR are applicable to the LASCS, but the anode gate gives the added possibility of turn-on with negative pulses with respect to the anode and turn-off with positive pulses.

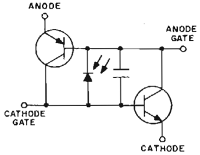


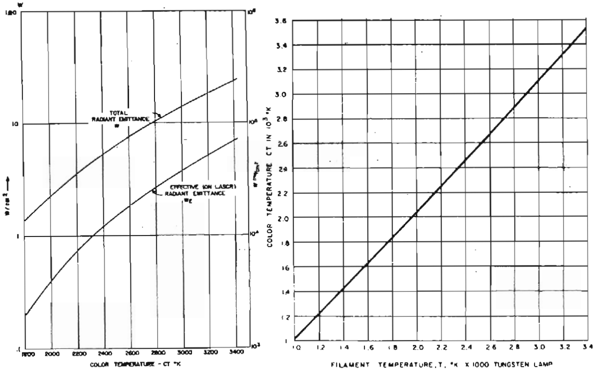
FIGURE 14.12 LASCS TRANSISTOR EQUIVALENT

The General Electric light activated silicon controlled switch is electrically similar to the 3N80 series silicon controlled switch, but is provided with a lens capped package for triggering by light (see Figure 14.11(a)). The curves shown for the LASCR are similar for the LASCS.

14.2 LIGHT EMITTING DEVICES

14.2.1 Tungsten Lamps

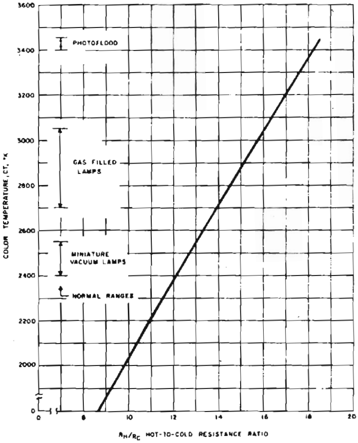
Tungsten filament incandescent lamps are probably the best known light emitting devices. Their wide range of spectral emission, their good efficiency and low cost make them ideal devices to use with General Electric light sensing devices.



(a) Emittance of Tungsten

(b) Relationship Between Color Temperature and True Filament Temperature for Tungsten Lamps

FIGURE 14.13 MOST IMPORTANT CHARACTERISTICS OF TUNGSTEN LAMPS



(c) Color Temperature Vs Hot-to-Cold Resistance Ratio for Tungsten

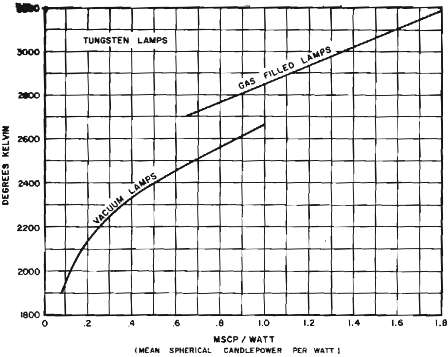
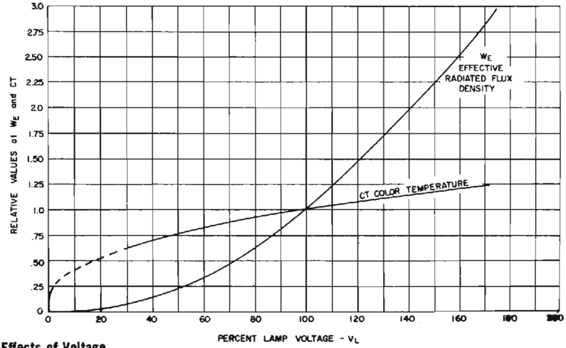


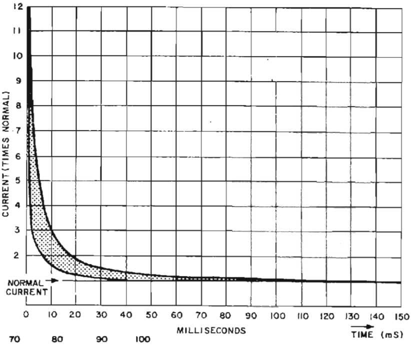
FIGURE 3.9 APPROX. COLOR TEMPERATURE VS EFFICIENCY

(d) Color Temperature Vs Efficiency

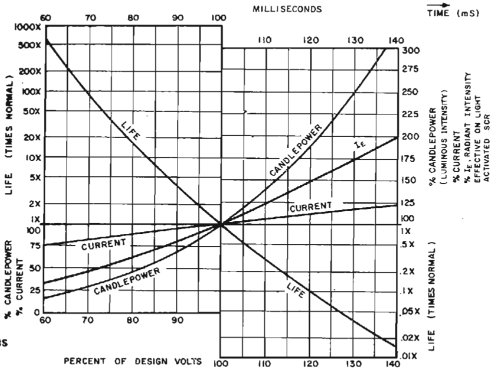
FIGURE 14.13 MOST IMPORTANT CHARACTERISTICS OF TUNGSTEN LAMPS



(e) Effects of Voltage on Tungsten Lamps



(f) Inrush Current Vs Time With Rated Voltage Applied



(g) Character Curves of Tungsten Lamps

FIGURE 14.13 MOST IMPORTANT CHARACTERISTICS OF TUNGSTEN LAMPS

Figure 14.13(a) shows the high radiant emittance of tungsten as a function of color temperature and also its high effective radiant emittance on the LASCR. Effective irradiance to trigger a LASCR typically is between 0.15 mW/cm^2 at 100°C to 20 mW/cm^2 at −65°C. This indicates that any tungsten lamp will trigger an LASCR providing the distance is not excessive. The same can be said for all other GE light sensing devices mentioned in this chapter.

Color temperature (CT) is a very popular measurement for tungsten lamps because color temperature defines the majority of the lamp's characteristics. Several of these characteristics are shown in Figure 14.13(a)-(b).

One very useful method of establishing filament temperature is based upon the fact that resistance of the filament increases with increasing temperature. Figure 14.13(c) shows the theoretical relationship between color temperature and the ratio of hot resistance to cold resistance, measured at 25°C. The measurement of this cold resistance must be made with the lowest voltage and current possible in order to prevent heating during the measurement. This can be done with a bridge by applying the voltage momentarily and noting the initial direction of the galvanometer deflection, then balancing accordingly. The observed resistance should be decreased by about 10% (multiply by 0.9) to account for resistance of lead wires, socket, and the connecting ends of the filament which are cooled by the lead wires. Measurement of hot resistance is made by using operating voltage and current values. Small lamps having low-mass filaments will have considerable cyclic temperature variations when operated at 50 or 60 Hz, hence hot resistance should be measured with an oscilloscope.

Figure 14.13(d) shows an easy method of approximating color temperature by the luminous efficiency of the lamp. If the input power and either the mean spherical candlepower (MSCP), or candlepower (CP) or total output lumens ($I = F/4\pi$) (Source intensity $= I$ in lumens/steradian = candle; Total flux output of source $= F$ in lumens) are known, then the color temperature may be established. The difference between evacuated and gas-filled lamps is the result of heat being conducted away from the filament by the gas. In general, lamps designed for operation at 5 volts or less, and less than 10 watts, are evacuated. It should also be noted that the geometric configuration of the filament will produce variations from the data of Figure 14.13(d).

Once a point has been established for a lamp, it may be desirable to know the effect of variations in supply voltage on the effective radiant output. Figure 14.13(e) shows this effect upon output and upon color temperature.

Similar information is given in Figure 14.13(f) which also relates life, current, and candlepower to lamp voltage. Note that the life curve is on a logarithmic scale. At 65% voltage, life is extended 200 times, input power is 50%, and effective radiation on an LASCR is reduced to 40% of the initial value.

Of particular importance is the effect of "normal" supply voltage variations of ±10%.

When incandescent lamps are connected in series with semiconductors the initial lamp inrush current flows through the semiconductor.

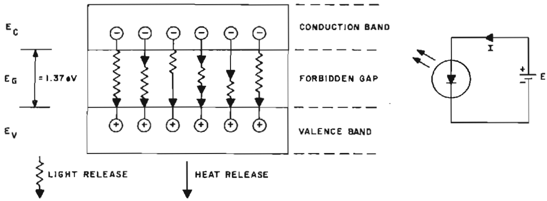
Peak inrush current can be up to 20 times the normal RMS operating current. It will not always reach the maximum values shown in Figure 14.13(g) because circuit impedance will have a limiting effect. Applying a preheat voltage is often used to limit inrush current to safe values. See Section 9.2.2 for further discussion on this subject.

14.2.2 Light Emitting Diodes (LED) or Solid State Lamps (SSL)

The light emitting diode is a p-n junction which when forward biased will emit light. There are several inherent advantages of an SSL light source over conventional sources.

1. Very fast response time. Fall and rise time can be in the order of a few nanoseconds to a few microseconds (depending on type).
2. Long life and mechanical ruggedness, leading to much improved reliability.
3. Low impedance of SSL, similar to a conventional forward biased diode.
4. The predominant light output is monochromatic.

Light emission from a p-n junction occurs when electrons from the bottom of the conduction band recombine with holes at the top of the valence band. The energy released from the electron corresponds to the width of the forbidden energy gap.



(a) Energy Bands in SSL **(b) Biasing of SSL**

FIGURE 14.14 ENERGY BANDS AND BIASING OF SSL

A gallium arsenide lamp has an energy band gap of $E_G = 1.37$ eV. The wave length which will be emitted (λ) is:

$$\lambda = \frac{h \cdot C}{E_q} \text{ in microns}$$

where: $h = 6.63 \times 10^{-34}$ joule seconds (Planck's constant)
$C = 3 \times 10^{14}$ micron/second (velocity of light)
E_q = Energy in Joules (lev $= 1.6 \times 10^{-19}$ joule)

For GaAs: $E_q = (1.39)(1.6 \times 10^{-19}) = 2.19 \times 10^{-19}$ joule

$$\lambda = \frac{(6.63 \times 10^{-34})(3 \times 10^{14})}{2.19 \times 10^{-19}} = 9.05 \cdot 10^{-1} \text{ microns}$$

$$= .905 \text{ microns}$$

This calculated wave length belongs to the infrared region of the radiant energy spectrum. GaAs SSL therefore are classified as infrared sources since they have a peak emission near 0.9 micron.

The energy released by the electrons, which may occur as light or heat, has to be replaced by an external power source as shown in

Figure 14.14(b). The quantum efficiency (QE) of a SSL determines how much electrical energy is converted to light energy. In an indirect material, some of the electrons when traveling from the conduction band to the valence band are detained in trapping levels, causing phonon (heat) as well as photon (light) releases.

$$QE = \frac{\text{No. of Photons Out}}{\text{No. of Electrons In}}$$

FIGURE 14.15 VIEW OF SSL AND SYMBOL OF SSL

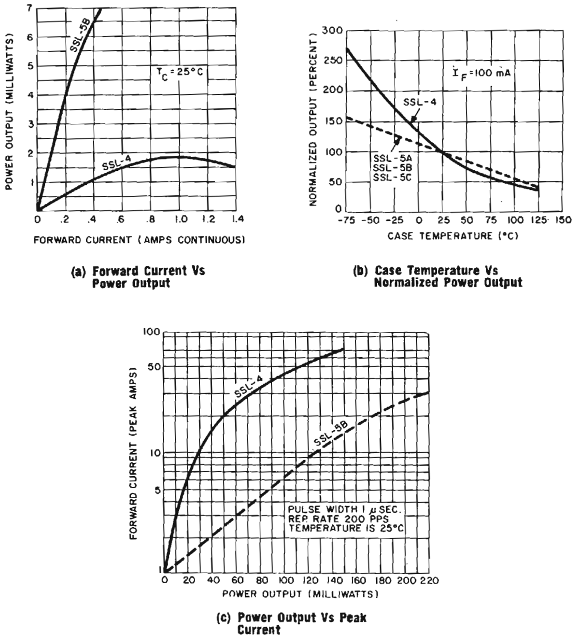


FIGURE 14.16

The most useful information in an SSL specification sheet is its power output (irradiance) H_{out} in mW versus current input. Figure 14.16(a) shows the power output H in mW increasing until a peak point is reached. The efficiency of GaAs SSL decreases with increasing temperature because more trapping levels occur in the energy gap (see Figure 14.16(b)).

To increase output power H_{out}, SSL's are often used in a pulsed condition. SSL's can withstand much higher peak currents under these conditions. The average current depends on the duty cycle which is determined by: Duty Cycle $= \frac{t_{on}}{t_{on} + t_{off}}$. Maximum peak current I_p is dependent on maximum average current and the duty cycle: Duty Cycle $= \frac{I_{avg}}{I_{peak}}$.

14.3 PHOTON COUPLER

Light emitting devices and light sensing devices have major applications in areas where electrical isolation between the input signal and the output is important.

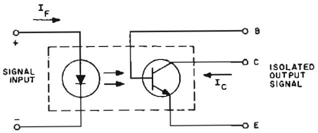


FIGURE 14.17 CIRCUIT COMPONENTS IN A PHOTO COUPLER

The General Electric PC15-26 and PC4-73 photon couplers consists of an SSL and a photo transistor. When an input signal is applied to the GaAs SSL, the light emitted is detected by the photo transistor and converted back to an electrical signal. Input and output signal have complete electrical isolation and there is no feedback from the output to the input.

The main advantages are:

1. Simple interface between different voltage levels.
2. Noise isolation and ground loop elimination.
3. High speed switching.
4. Modification of output signal through access to base terminal.
5. High shock and vibration immunity.
6. Bounceless switching.
7. Small size.

Figure 14.18 shows input current versus output current for the PC4-73. Note that this is a linear relationship. Output current and dark current are influenced by temperature and should be considered when designing with photon couplers.

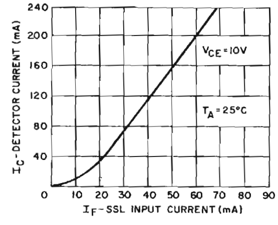


FIGURE 14.18 INPUT CURRENT (mA) VS OUTPUT CURRENT (mA) FOR THE PC4-73 PHOTON COUPLER

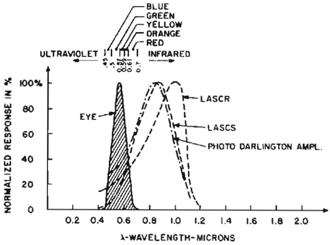
14.3.1 Specifications of Light Intensity*

In order to apply these devices, it is necessary to know if a given source at a known distance will cause the desired response in a sensor. This is a function of the characteristics and intensity of the light, the response of sensor to that type of light, and the physical relationship and optical coupling between the source and sensor. The output of most sources is specified in terms of visible light. There is no general relationship between visible light and the effect of the radiation on a sensor.

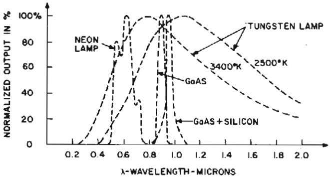
*See application Note 200.34 for more detailed discussion of this subject and applications of the LASCR.

14.4 CHARACTERISTICS OF SOURCES AND SENSORS

Most people learn in high school physics that light is a form of electromagnetic radiation. Electromagnetic radiation is characterized by its frequency (or more commonly in the case of light, wave length), magnitude and direction. Sources vary greatly in the components of frequency in their output. Figure 14.9(a) shows the spectral distribution of some of the more common types of light sources. The characteristics of the light from a tungsten lamp are a function of the color temperature of that lamp. The color temperature depends upon the type of lamp and upon the applied voltage.



(a) Light Sensitive Devices



(b) Light Emitting Devices

FIGURE 14.19 SPECTRAL DISTRIBUTIONS OF GENERAL ELECTRIC LIGHT SENSITIVE AND LIGHT EMITTING DEVICES

The effect of electromagnetic radiation on a sensor depends upon the wave length of the radiation. The relative effect of radiation of different wave lengths upon the eye and upon several types of silicon semiconductor sensors is shown in Figure 14.9(b). The eye responds to shorter wave lengths than do silicon devices. By comparing Figure 14.9(a) and 14.9(b) it can be seen that most of the radiation emitted by a tungsten lamp is not visible. Hence, it is important to note that the amount of visible light produced by a source does not reveal how effective this source will be upon a silicon sensor.

14.4.1 Definition of Light Intensity

The intensity of electromagnetic radiation incident on a surface is called irradiance (H). Its dimensions are watts/square centimeter. Since any type of electromagnetic radiation has a spectral distribution, it is also reasonable to define the irradiance per unit of wave length (Hλ). Hλ is a function of the wave length. By definition then,

$$H = \int H\lambda \, d\lambda$$

Yλ is the relative response of a sensor to electromagnetic radiation at any given wave length. The effect of a particular wave length from a light source on a given sensor is the product Hλ Yλ. The effect of radiation on a sensor is additive so that to determine the total effect

of a particular source on a particular sensor, it is necessary to add the Hλ Yλ products for all wave lengths of interest. Or,

$$H_E = \int H\lambda\ Y\lambda\ d\lambda$$

H_E is called effective irradiance.

The definition of light is the effective irradiance on the human eye. The amount of light incident on a surface, or the illuminance (E), is given by the following equation:

$$E = K\int H\lambda\ Y\lambda\ d\lambda$$

Yλ in this case is the relative spectral response of the human eye as shown in Figure 14.19(b). K is a proportionality constant depending on the desired units. To get E in the units of foot candles, where H is given in terms of watts per square centimeter, K is equal to 6.35×10^5.

Effective irradiance is used in specifying the GE light sensing devices. The response of these devices versus wave length is provided on the specification sheet so that effective irradiance can be calculated if the characteristics of the light source is known. The effective irradiance to trigger (H_{ET}) is the minimum amount of effective irradiance that will trigger these devices into conduction.

The curve of Figure 20.20 shows this efficiency for a tungsten lamp as a function of color temperature of the lamp. The ratio of effective irradiance to total irradiance can be used with total irradiance as calculated, or as measured with a thermopile, to determine operation of the light sensitive device.

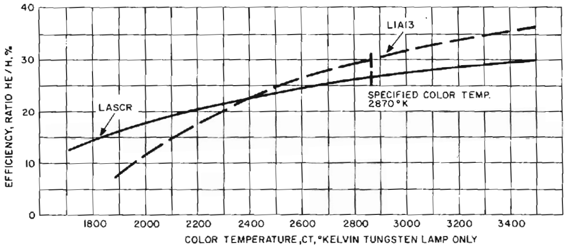


FIGURE 14.20 LASCR AND L14B EFFICIENCY OF TUNGSTEN LAMP VS COLOR TEMPERATURE

14.4.2 Design Procedures

For a source with a given spectral distribution, there is a definite relationship between the illuminance (light) and the effective irradiance on a sensor. This ratio has been determined for the combination of a tungsten lamp and an LASCR and is given in Figure 14.21 as a function of the color temperature of the lamp.

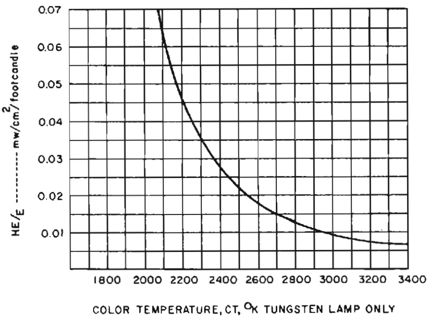


FIGURE 14.21 LASCR EFFECTIVE IRRADIANCE PER FOOTCANDLE FOR A TUNGSTEN LAMP VS COLOR TEMPERATURE

The irradiance on a device varies inversely with the square of the distance between a point source and the device. The devices are most sensitive if the lens in the cap is pointed directly at the source. The relative response for other angles is given on the specification sheets of the devices. As an example, let us calculate the effective irradiance on an LASCR 6 inches from a point source emitting 100 candela at a 2500°k color temperature. Assume the LASCR is perfectly aligned with the source. At .5 feet the light intensity is

$$E = \frac{100 \text{ candela}}{(.5 \text{ ft})^2} = 400 \text{ ft candles}$$

The conversion factor from E to H_E at 2500°k from Figure 14.21 is .023 mW/centimeter squared foot candles. This means that

$$H_E = E \times .023 = 400 \times .023 = 9.2 \text{ mW/cm}^2$$

This amount of light would be adequate to trigger all L9 LASCR's which are specified at a minimum H_{ET} of 4.2 mW/centimeter squared.

14.4.3 Effective Irradiance to Trigger

H_{ET} varies depending on how the device is applied in a circuit. Parameters that affect gate trigger current or base current affect H_{ET} in a similar manner. Increases in voltage, temperature or R_{GK} will reduce H_{ET} and also the required irradiance to produce a given current in a light sensitive device.

Resistor R_{GK} is almost always used with the LASCR and LASCS. Its purpose is to prevent the devices from being triggered by leakage current and to hold the sensitivity to "rate effect" triggering to a reasonable level. This resistor is particularly important in elevated temperature applications.

Replacing R_{GK} with an inductor (approximately 1 henry) makes the LASCR and LASCS sensitive to rate of rise of light intensity rather than absolute value. After triggering, the holding current of the device

will increase as the current in the inductor increases. If the holding current becomes greater than the anode load current, the device turns off. The ringing caused by capacitance in parallel with the inductor will sometimes cause the device to turn back on at a later time. An inductor with a high L/R ratio can reduce turn-off time of the thyristor by maintaining negative gate current during the commutating interval.

14.4.4 Approximate Irradiance Calculation

The conversion efficiency of tungsten lamps from input power to radiant power is approximately 80% for gas filled lamps and 90% for evacuated lamps. At rated voltage this leads to a method for deriving a rough approximation of total irradiance on a receiver by assuming spherical distribution.

$$H = \frac{P_{out}}{4 \cdot \pi \cdot d^2} \text{ (mW/cm}^2\text{)}$$

$$P_{out} = P_{in} \times (0.8 \text{ or } 0.9) \text{ (mW)}$$

$$d = \text{distance from source to receiver (cm)}$$

$$H_{effective} \approx \frac{1}{4} \cdot H \text{ (mW/cm}^2\text{)}$$

Accuracy depends on color temperature and departure from spherical distribution of the particular case.

14.4.5 Refined Irradiance Calculations

Lamp: GE #1400

$$\left.\begin{aligned} V_L &= 3.2 \text{ volts} \\ i_L &= 0.16 \text{ amps} \\ CP &= 0.20 \text{ candela} = I_L \\ \text{Life} &= 3000 \text{ hours} \end{aligned}\right\} \text{From lamp specifications}$$

Required life = 30,000 hours

$$P = V_L \cdot i_L = 0.512 \text{ W}$$

$$\text{Luminous efficiency} = \frac{CP}{P} = \frac{0.20}{0.512} = 0.39$$

From Figure 14.13(d) for vacuum lamp CT = 2320°K

To get a ten times increase in life Figure 14.13(b) shows that V_L has to be reduced to 83% of 3.2 V or 2.65 volts. This reduced I_L (CP) to 50%, or 0.1 candela. Color temperature (see Figure 14.13(e)) is reduced 2320 × 0.93 = 2150°K. From Figure 14.20 H_E/E is 0.055 mW/cm²/footcandle. For a device like the L9 LASCR at 25°C H_{ET} = 4.2 mW/cm² is required.

$$\frac{4.2}{0.055} = 76.5 \text{ footcandles}$$

Assuming a point source then

$$E = \frac{I_L}{d^2} \left[\frac{\text{Lumen}}{\text{Foot}^2}\right]$$

$$d = \sqrt{\frac{I_L}{E}} \qquad I_L = 0.1 \text{ candle}$$

$$d = \sqrt{\frac{0.1}{76.5}} = .036 \text{ feet} = 1.1 \text{ cm}$$

1.1 cm is the maximum working distance from the filament to the LASCR pellet which will trigger the least sensitive of the L9 type LASCR's at 25°C with a 6 volt anode supply.

14.4.6 Comparison of Sources

Typical values of emitted flux density for various types of light sources are shown in Figure 14.22. Radiant emittance, W, and luminous emittance, L, are both given for comparison. Of specific interest for use with the LASCR is the effective radiant emittance, W_E, which is obtained from the relationship between spectral distribution of energy from the source and spectral response of the LASCR. The ratio W_E/W is also the ratio H_E/H shown in the Table. The conversion factor from photometric to radiometric effective value is given by the ratio H_E/E.

SOURCE	Emitted Flux Density*			Color Temp.	Effectiveness*	
	W (mw/cm²)	L (Footlamberts)	W_E (effective) (mw/cm²)	CT(°K)	H_E/E	H_E/E (mw/cm²/fc)
Candle Flame	10^4	3×10^3	700	2000	.07	.065
Sun	4.5×10^6	4.5×10^8	2.8×10^6	5800	.5	.003
Tungsten Lamps Miniature (evacuated)	6×10^4	6×10^5	1.3×10^4	2500	.22	.022
Standard (gas filled)	1.3×10^5	2.5×10^6	3.8×10^4	2900	.29	.013
Standard (frosted 100W)	2.6×10^3	5×10^4	7.5×10^2	2900	.29	.013
Photo	2.5×10^5	9×10^6	9×10^4	3400	.35	.009
Neon (NE-2 at 1 ma)	8×10^{-2}		6×10^{-2}		.75	
Fluorescent (Daylight 40W)	30	2×10^3	12		.4	.006
Xenon Flash (450 V, 10 ws)	1.2×10^7	1×10^9	6×10^6		.5	.006
Solid State Lamp Continuous Operation	0.5-570	0	0.5-570		1	
Solid State Lamp Pulsed Operation	$20\text{-}55 \times 10^3$	0	$20\text{-}55 \times 10^3$		1	

*Approximate Values

FIGURE 14.22 TYPICAL CHARACTERISTICS OF SOURCES

It is interesting to note that although H_E/H is high for the neon lamp, the extremely low emittance in normal operation of this lamp means that the lamp must be heavily over-driven to obtain enough energy to trigger the LASCR. Another interesting point is the similarity in W_E between a candle flame and a 100 watt frosted incandescent lamp, when compared with the large difference in luminous emittances. The highest effective radiant emittance is found in the

xenon flash lamp because of its high power density and concentration of energy around the response band of silicon.

14.5 APPLICATIONS

14.5.1 Light Activated DC and AC Relays

The combination of an LASCR or a LASCS with a lamp is close to being the semiconductor analog of an electromechanical relay. This combination offers complete electrical isolation between input and output and an excellent current carrying capability. These are two characteristics that make a relay so useful. In addition, this combination offers the other solid state virtues of long life, microsecond response, freedom from contact bounce and small size. Figures 14.23-14.25 depict some basic LASCR relay configurations. Figure 14.23 shows the LASCR used with a DC power supply. If the LASCR is off and the lamp is not energized, the load will see what appears to be an open circuit. When the input lamp is energized, the LASCR will switch into conduction so that there is approximately 1 volt drop across it. When the lamp is shut off, the LASCR will remain latched on and must be reset externally by S_1. The tungsten lamp (TL) can be replaced by a solid state lamp which is able to apply light to the sensing device a few nanoseconds after it is forward biased. See Section 14.6, Circuits for Light Emitting Devices.

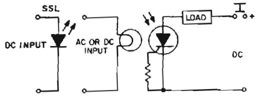


FIGURE 14.23 DC LATCHING RELAY

Figure 14.24 shows the same circuit with an AC power supply. Since the LASCR will not conduct when its anode is negative with respect to the cathode, the current through the load will be halfwave rectified. The current through the load will flow only when the lamp is energized. The LASCR will reset during the negative half of the AC cycle. The free-wheeling diode shown in this circuit is used with inductive loads, such as relays or solenoids, to provide a smoother load current and reduce chattering.

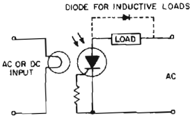
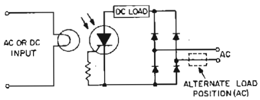
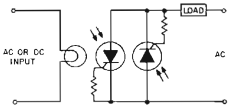


FIGURE 14.24 AC NON LATCHING RELAY

A nonlatching circuit for driving DC loads is shown in Figure 14.25. In this circuit fullwave rectified AC is applied to the LASCR and the load. The LASCR will reset when the voltage applied to the load goes to zero. This circuit is therefore nonlatching. Care should be taken when using this circuit since difficulty in LASCR commutation may be encountered. By placing the load in the alternate position shown, full wave AC power will be applied to it when the lamp is energized. An alternate method of driving an AC load is shown in Figure 14.25. The electrical isolation of the optical coupling allows the two LASCR's to be used in the inverse-parallel connection. A possible difficulty with this circuit is that a light level between the sensitivity of the two devices may cause one device to turn on and not the other thereby causing a DC component of current to flow through the load. This difficulty could be solved by using sufficiently high light levels to guarantee triggering of both devices.



(a) AC or DC Contact

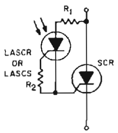


(b) Alternate AC Contact

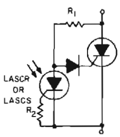
FIGURE 14.25 LASCR RELAY CONFIGURATIONS

14.5.2 Triggering Higher Power SCR's by Light

The power handling ability of any of the preceding circuits may be increased by using the LASCR or LASCS as a gate amplifier to trigger a larger SCR (Figure 14.26(a)). Repositioning the light sensitive device with respect to the driven SCR (Figure 14.26(b)) converts the circuit into the equivalent of a normally closed relay contact. This is a useful configuration in many monitoring and alarm circuits requiring the load to be energized in the absence of light.



(a) Normally off SCR



(b) Normally on SCR

FIGURE 14.26 TRIGGERING HIGH CURRENT SCR'S

If the voltage applied to the load and the LASCR is greater than the voltage rating of the LASCR, an LASCS or an LASCR or a light sensitive transistor can be used to trigger a higher voltage SCR. The

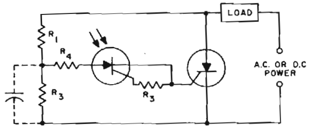
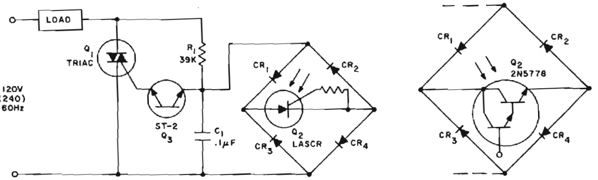


FIGURE 14.27 USE OF LASCR TO TRIGGER HIGHER POWER SCR'S

circuit for doing this is shown in Figure 14.27. If DC power is used (or if AC power and a pulsed light), the capacitor indicated will allow larger resistance values to be used for resistors R1 and R2 by furnishing the necessary trigger current pulse for the SCR. If AC power is used, when a steady light is applied to the light sensitive device, a charge cannot build up on the capacitor so that it does not aid triggering. In this case R1 must be small enough to provide adequate trigger current for the SCR and large enough so that the gate current rating of the SCR is not exceeded. R2 determines the required breakdown voltage of light sensitive devices.

14.5.3 Light Activated Triac Applications

The combination of light sensitive devices with power semiconductors opens a wide new area of very useful circuits. Figure 14.28 shows a normally closed relay. When AC is applied to the input terminal and no light is directed toward the light sensitive device (high impedance), the voltage on capacitor C_1 will rise until breakover of ST-2 (32 V) is reached and triac Q_1 will trigger applying AC to the load. This will be repeated on each half cycle.

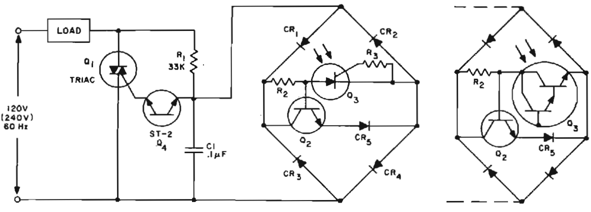


(a) With LASCR **(b) With Light Activated Darlington Amplifie**

FIGURE 14.28 NORMALLY CLOSED AC RELAY

Directing light toward the light sensing device will switch it into the on-state, shorting both polarities of voltage across C_1, allowing Q_1 to turn off.

Figure 14.29 shows a normally open relay. This circuit is basically the same as Figure 14.28 except that an additional transistor, Q_2, is used as an inverting stage.

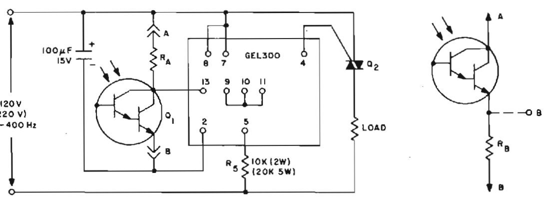


(a) With LASCR (b) With Light Activated Darlington Amplifier

FIGURE 14.29 NORMALLY OPEN AC RELAY

14.5.4 Light Activated Integrated Zero Voltage Switch

GE light sensitive devices in conjunction with the GE GEL300 zero voltage switch and the GEL301 phase control provide some very practical circuits for resistive loads.



(a) Normally Open (b) Normally Closed

FIGURE 14.30 LIGHT ACTIVATED ZERO VOLTAGE SWITCH

Figure 14.30(a) shows a normally open solid state relay. When light is directed toward Q_1 (L14B or L14A) the triac will be actuated at the next zero crossing of the line voltage. The inverted logic is shown in Figure 14.30(b), normally closed relay. For more information see Chapter 11 on zero voltage switches.

Using the above configurations (Figure 14.30(a)), Figure 14.31(a) could be a normally open control, but as soon as light is directed towards Q_1, Q_2 is turned on leaving the decision of turn-on or turn-off entirely to the resistance ratio of R_A to R_B. For example, a room temperature control works only when the light in the room is on. Figure 14.31(b) shows the same principle but for a normally closed configuration.

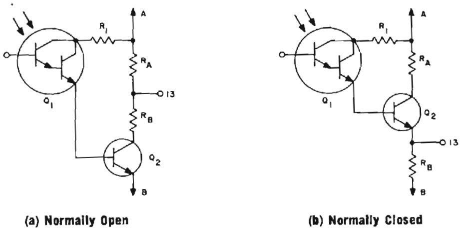


FIGURE 14.31 LIGHT ACTIVATED ZERO VOLTAGE SWITCHING CONTROL

14.5.5 Light Activated Integrated Circuit Phase Control

Figure 14.32 shows a typical circuit where a GEL301 integrated circuit controls the phase angle at which Q_1 triggers, thereby varying power to the load. The ratio of R_A to R_B determines the triggering angle of the triac, Q_1. (See also Chapter 9.)

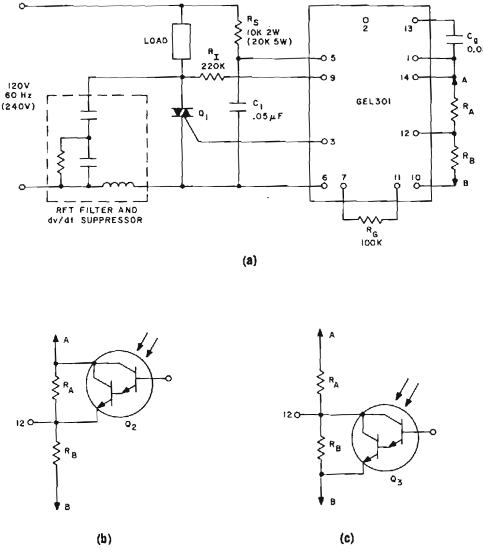


FIGURE 14.32 LIGHT ACTIVATED INTEGRATED CIRCUIT PHASE CONTROL

In Figure 14.32(a) as soon as light is directed at Q_2 (R_A parallel $Q_2 < R_B$) a phase angle retard would result, reducing the power applied to the load. In Figure 14.32(c) as soon as light is directed at Q_3 (R_B parallel $Q_3 < R_A$), an advance in phase angle would result and cause an increase in power. Many variations are possible. Changing the light intensity on Q_2 and Q_3 would give phase control with isolated input.

14.5.6 Series Connection of SCR's Triggered by Light (Light Activated High Voltage Switch)

For triggering very high voltage loads, series connections of SCR's are used. The circuit shown in Figure 14.33 illustrates how the electrical isolation of the LASCS or the LASCR can be used to good advantage. This circuit is capable of blocking voltages equal to the sum of the voltage ratings of the five SCR's. See Chapter 6 and Reference 10.

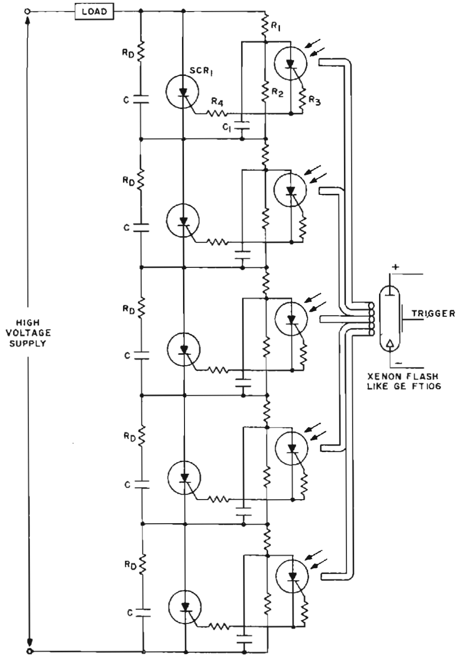
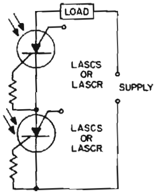


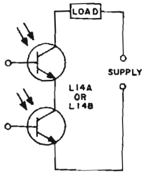
FIGURE 14.33 USE OF LASCR'S TO TRIGGER SERIES CONNECTED SCR'S

14.5.7 Light Activated Logic Circuits

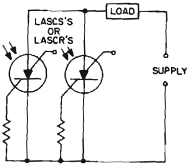
The binary nature of the LASCS and the LASCR makes them ideal elements for use in opto-electronic logic circuitry. Figure 14.34 illustrates some of the common logic functions that can be implemented with these devices.



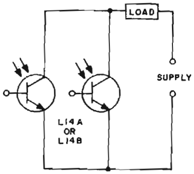
(a) "And" Circuit



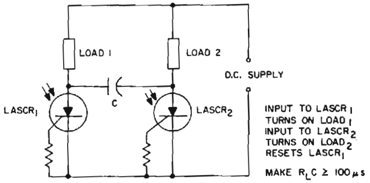
(b) "And" Circuit



(c) "Or" Circuit



(d) "Or" Circuit



(e) Flip-Flop

FIGURE 14.34 OPTOELECTRONIC LOGIC CIRCUITS

14.5.8 Light Activated Astable Circuits

The circuits in Figure 14.35 and 14.36 are light triggered single shots. In Figure 14.35, the unijunction transistor triggers approximately .6 sec after a pulse of light turns on the LASCR. If the pulse of light has ended, the LASCR will turn off. If the light is still on the unijunction will operate as a relaxation oscillator. It will turn the LASCR off the first time it fires after the light is removed. When the LASCR is off, the high resistance in series with the capacitor prevents the unijunction from oscillating.

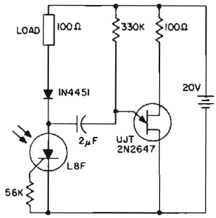


FIGURE 14.35 SELF CLEARING SINGLE SHOT

In the circuit shown in Figure 14.36, with no light applied to the LASCR, the 3N81 silicon controlled switch is in the conducting state. When a short pulse of light is applied to the LASCR, it is turned on and the SCS is commutated off through the one microfarad capacitor. At the same time, the voltage at the junction of the four microfarad capacitor and the 220k resistor is pulled negative. This voltage gradually goes positive due to the charging action of the 220k resistor. After approximately .6 of a second the SCS is turned on. This in turn commutates off the LASCR.

This circuit is useful for detecting the presence of pulses of light that last longer than some minimum time. If the pulses last longer than 0.6 sec, the LASCR will remain in the conducting state.

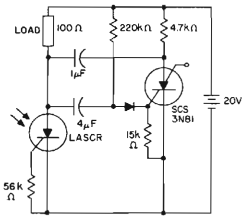


FIGURE 14.36 SINGLE SHOT AND PULSE WIDTH SENSOR

14.5.9 Light Interruption Detector

When the light incident on the LASCS in Figure 14.37 is interrupted, this allows the voltage at the anode to the 2N4990 unilateral switch to go positive on the next positive cycle of the power and trigger the switch and the C5 SCR when the switching voltage of the unilateral switch is reached. This will cause the load to be energized for as long as light is not incident on the LASCS.

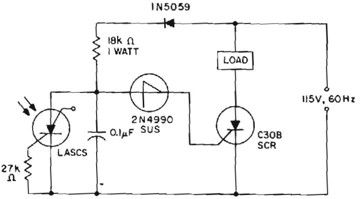
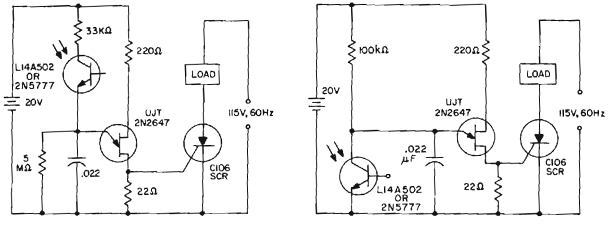


FIGURE 14.37 LIGHT INTERRUPTION DETECTOR

The unilateral switch allows higher power SCR's with their higher gate triggering currents to be used while holding the power in the 18kΩ resistor to a reasonable value. The charge in the capacitor provides a pulse of current adequate to trigger high current SCR's.

14.5.10 Higher Sensitivity Light Detectors

The L14A502 phototransistor and a unijunction transistor in combination allow much lower levels of light to be detected. Figure 14.38 shows how this can be done. In Figure 14.38(a) when the phototransistor has light incident upon it, the unijunction will oscillate as a relaxation oscillator. Since its frequency is considerably higher than 60 Hz, the C106 SCR is turned on early in the positive half of every cycle. The circuit in Figure 14.38(b) energizes the load when light is



(a) Light Presence Detector **(b) Light Absence Detector**

FIGURE 14.38 HIGHER SENSITIVITY CIRCUITS

removed from the phototransistor. In this circuit when the phototransistor is dark, the unijunction operates as a relaxation oscillator and energizes the load on positive half cycles.

14.5.11 "Slave" Electronic Flash

There is a need, in the photographic industry, for a fast photosensitive switch capable of triggering the "slave" flash units used extensively in multiple-light-source high speed photography. Figure 14.39 shows how an industry-standard flashgun circuit can be modified with an LASCR to serve as a fast acting slave unit. With switch S_1 closed, capacitor C_1 charges to 300 volts through R_1, and capacitor C_2, charges to approximately 200 volts through R_2 and R_3. When the master flashgun fires (triggered by the flash contacts on the camera) its light output triggers $LASCR_1$, which then discharges capacitor C_2 into the primary winding of transformer T_1. Its secondary puts out a high voltage pulse to trigger the flashtube. The flashtube discharges capacitor C_1, while the resonant action between C_2 and T_1 reverse biases $LASCR_1$ for positive turn-off. With the intense instantaneous light energy available from present-day electronic flash units, the speed of response of the LASCR is easily in the low microsecond region, leading to perfect synchronization between master and slave.

High levels of ambient light can also trigger the LASCR when a resistor is used between gate and cathode. Although this resistance could be made adjustable to compensate for ambient light, the best solution is to use an inductance (at least one henry) which will appear as a low impedance to ambient light and as a very high impedance to a flash.

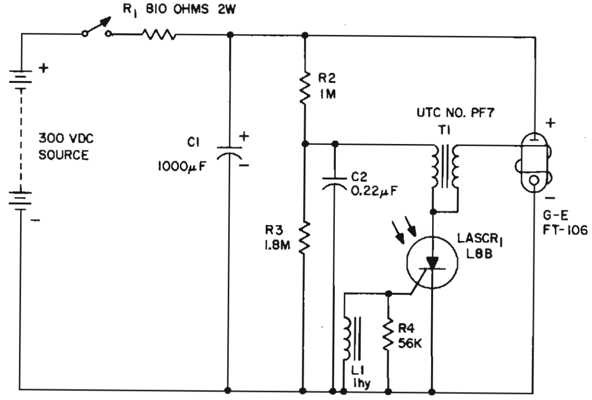
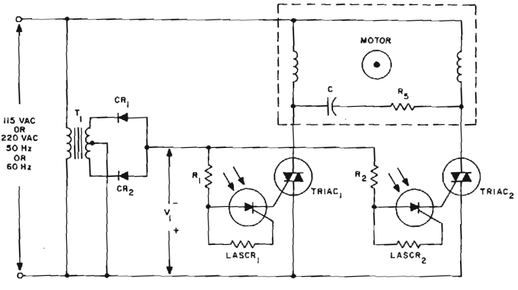


FIGURE 14.39 SLAVE FLASH

14.5.12 Light Activated Motor Control

Light sensing devices can be used to perform the switching function in a reversible motor control circuit. In this case S_1 has to be used to reset the circuit.

Figure 14.40 shows such a light activated control where the light is used to control the direction of rotation of a balanced winding permanent split capacitor motor through two triacs.



LASCR = GE L9U

CR_1, CR_2 - GE A14F

FIGURE 14.40 REVERSING INDUCTION-MOTOR DRIVE

The transformer T_1 is selected to have a dc secondary voltage V_1 between 6 to 24 volts.

$$R_1 = R_2 = \frac{V_1}{I_{Gate\ 1}} = \frac{V_1}{I_{Gate\ 2}} = \frac{V_1}{100\ \text{ma}} \qquad R_5 \approx 10\ \text{ohms}$$

Whenever light is directed toward $LASCR_1$, triac 1 would be triggered, turning the motor into one direction. Removing the light from $LASCR_1$ and directing it toward $LASCR_2$ would turn off triac 1 and turn on triac 2 which will reverse the direction of the motor.

$LASCR_1$ and $LASCR_2$ could be replaced by LASCS or by light sensitive transistors but maximum current rating for the transistor should be considered. The triacs must have voltage ratings at least equal to the capacitor voltage rating (usually 1.5 to 2.5 times peak line voltage).

14.6 CIRCUITS FOR LIGHT EMITTING DEVICES

Designing power supplies for light emitting devices requires the understanding of how the wave shapes of the supply influence the irradiance, H, of light emitting devices.

*Measurement was made with the A14 diode in series.

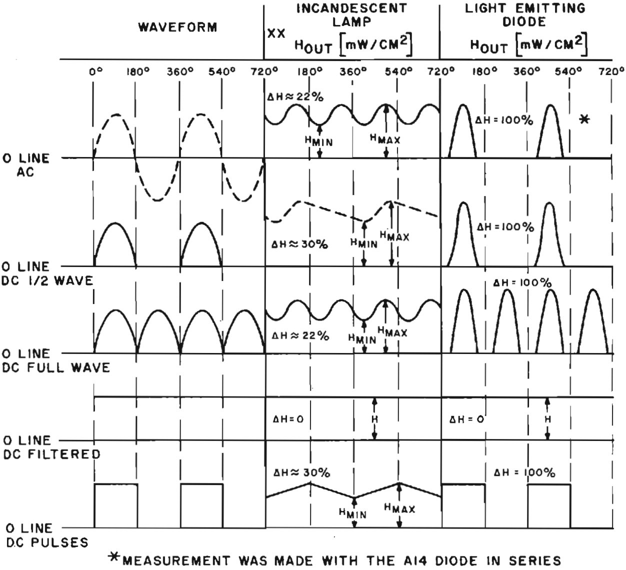


FIGURE 14.41 DEPENDENCE OF IRRADIANCE OF LIGHT EMITTING DEVICES FROM INPUT WAVEFORMS

The irradiance H in the above table was measured on a GE #1813 light bulb (14.4 volts; 0.1 amp; ≈ 0.86 CP). ΔH maximum will be larger for smaller, lower mass filament bulbs and will be smaller for larger bulbs. If ΔH, the irradiance change as shown in the table, cannot be tolerated, filtered dc supplies should be used.

14.6.1 Low Loss Brightness Control

A circuit which changes average value of the DC supply voltage on the light emitting device is shown in Figure 14.42. Because of the high switching frequency the tungsten lamp will have an almost continuous adjustable light output between 0 and 100%. If a light emitting diode is used as the emitting device, the irradiance will be in phase with the applied current pulses and will decrease to zero when the supply current is zero.

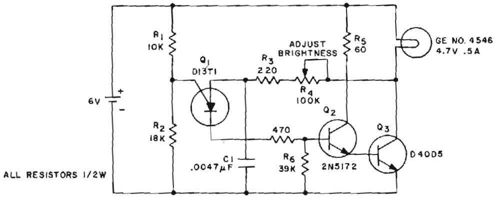


FIGURE 14.42 LOW LOSS BRIGHTNESS CONTROL

In this circuit the PUT is used as an oscillator; the time constant and resultant frequency are determined by $(R_3 + R_4) \times C_1$. Every time Q_1 fires, Q_2 will be forward biased, driving Q_3 into saturation and applying the battery voltage to the light bulb.

14.6.2 Current Limiting Circuits

To protect light emitting devices from damaging current levels, different types of limiting circuits are used.

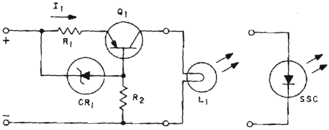


FIGURE 14.43 SIMPLE CURRENT LIMITER

A simple form of current limiter is shown in Figure 14.43. At low currents Q_1 is forward biased applying the full power supply voltage to the load. When $I_1 \cdot R_1 \approx V_{CR1}$, Q_1 will come out of saturation and limit lamp current to this value.

A more effective current limiter is shown in Figure 14.44. When the voltage drop across R_1 is greater than the base threshold voltage of Q_2, Q_2 will begin to conduct, divert base drive from Q_1 and Q_1 will limit the output current.

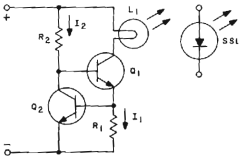
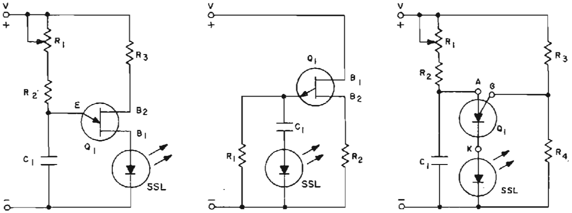


FIGURE 14.44 HIGHER PERFORMANCE CURRENT LIMITER

14.6.3 Impulse Circuits for Light Emitters

Because solid state light emitters have very low emission levels when continuously forward biased, a very popular method is to use them in a pulsed mode. Current levels can be many times higher than the continuous current without exceeding the average power.

A low current pulser can be very easily built with unijunction transistors of the same type used for SCR triggering circuits. More information on these circuits can be found in Chapter 4.



(a) Pulser With Unijunction Transistor (b) Pulser With Complementary Unijunction Transistor (c) Pulser With Programmable Unijunction Transistor

FIGURE 14.45 UNIJUNCTION TRANSISTOR PULSE GENERATORS

Pulse circuits for higher current levels can be designed by using SCR's which are ideal devices for such applications.

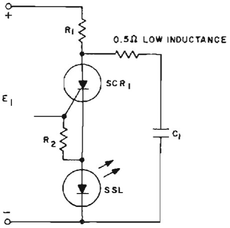


FIGURE 14.46 HIGH CURRENT PULSE GENERATOR

In Figure 14.46 capacitor C_1 is charged through R_1 and discharged through SCR_1 when the SCR is triggered. The limiting factor of this circuit is the holding current of SCR_1 which determines the smallest value for R_1,

$$R_{1_{min}} = \frac{E_{1_{max}}}{I_{H_{min}}}$$

Because the recharge cycle is long (five times $R_1 \cdot C_1$) this circuit is limited to low frequencies if large capacitors are used. Much higher frequencies can be obtained when a fast charging path for C_1 is added to the above circuit as in Figure 14.47. R_1 supplies Q_1 with base drive,

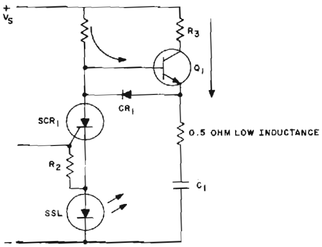


FIGURE 14.47 HIGH CURRENT HIGH FREQUENCY PULSE GENERATOR

turning Q_1 on. Current into the capacitor is limited by R_3. After C_1 is charged and SCR_1 is fired, CR_1 is forward biased and as long as CR_1 is conducting, the base of Q_1 is at a lower potential than the emitter. Assuming $V_S/R_1 <$ holding current of SCR_1, SCR_1 will turn off and the cycle will repeat.

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10. Flashtube Data Manual, Photo Lamp Department #281, General Electric Company, Nela Park, Cleveland, Ohio.

*Refer to Chapter 23 for availability and ordering information.

15 PROTECTING THE THYRISTOR AGAINST OVERLOADS AND FAULTS

Satisfactory operation of thyristor circuits and the equipment in which they operate often depends heavily on the ability of the system to survive unusual overcurrent conditions. One obvious answer to this requirement, not usually an economical one, although one that is becoming more reasonable with the decreasing costs of semiconductors, is to design the system to withstand the worst fault currents on a steady-state basis. This requires semiconductors and associated components that are rated many times the normal load requirements. Where this approach is not possible because of economics or other factors, an adequate overcurrent protective system is usually used.

15.1 WHY PROTECTION?

The functions of an overcurrent protective system are any or all of the following:

1. To limit the duration of overloads and the frequency of application of overloads.
2. To limit the duration and magnitude of short circuits.
3. To limit the duration and magnitude of fault current due to shorted semiconductor cells.[1]

The objective of these functions is to safeguard not only semiconductor components but also the associated electrical devices and buswork in the equipment from excessive heating and magnetic stresses. The trend toward high capacity systems feeding electronic converter equipment often results in extremely high available fault currents. Since both heating and magnetic stresses in linear circuit elements respond to the square of the current, the importance of adequate protection in "stiff" systems is self-evident.

Elaborating on function No. 3 above, thyristors as well as diode rectifiers may fail by shorting rather than by opening. In many circuits such a device fault results in a direct short from line to line through the low forward resistance of the good devices in adjacent legs during

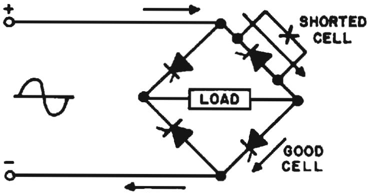


FIGURE 15.1 ARROWS INDICATE FLOW OF FAULT CURRENT THROUGH GOOD DEVICE AFTER ADJACENT LEG HAS SHORTED. LOAD RESISTANCE DOES NOT LIMIT CURRENT

at least part of the cycle, as illustrated in Figure 15.1. Under these circumstances, a protective system functions either to shut the entire supply down or to isolate the shorted device in order to permit continuity of operation. This will be discussed at greater length later.

It is difficult to make broad recommendations for overcurrent protection since the concept of satisfactory operation means different levels of reliability in different applications. The selection of a protective system should be based on such individual factors as:

1. The degree of system reliability expected.
2. The need or lack of need for continuity of operation if a semiconductor fails.
3. Whether or not good semiconductor cells are expendable in the event of a fault.
4. The possibility of load faults.
5. The magnitude and rate of rise of available fault current.

Depending upon the application, these various factors will carry more or less weight. As the investment in semiconductors increases for a specific piece of equipment, or as an increasing number of components in a circuit increases the possibility of a single failure, or as continuity of operation becomes more essential, more elaborate protective systems are justified. On the other hand, in a low-cost circuit where continuity of operation is not absolutely essential, economy type semiconductors may be considered expendable and a branch circuit fuse in the AC line may be all that is needed, or justified, for isolation of the circuit on faults, allowing semiconductor components to fail during the interval until the protection functions. In other designs, the most practical and economical solution may lie in overdesigning the current carrying capability of the semiconductors so that conventional fuses or circuit breakers will protect the semiconductors against such faults.

It is therefore reasonable that each circuit designer rather than the semiconductor component manufacturer decide precisely what level of protection is required for a specified circuit. Once the specific requirements are determined the component manufacturer can recommend means of attaining these specific objectives. This chapter is prepared to assist the circuit designer in determining his protection requirements, and then to select satisfactory means of meeting these requirements.

15.2 OVERCURRENT PROTECTIVE ELEMENTS

The main protective elements can be divided into two general classes. One class consists of those devices which protect by interrupting or preventing current flow, and the other class consists of those elements which limit the magnitude or rate of rise of current flow by virtue of their impedance.

Among the elements in the first class are:

1. The AC circuit breaker or fuse which disconnects the entire circuit from the supply.
2. The cell fuse or breaker which isolates faulted semiconductor cells.
3. Load breakers or fuses which isolate load faults from the equipment or a faulted cell from DC feedback from the load or parallel converter equipments.

4. Current limiting fuses and SCR circuit breakers.
5. Gate blocking of SCR's to interrupt overcurrent.

Internal leads of stud mounted devices may burn open under severe fault currents before regular protective elements function. Prior to leads burning open, the associated junction will have been permanently damaged to a shorted condition. (The internal fusing characteristics of commercial semiconductors are generally not predictable nor reliable enough to be used as protective elements in practical circuits.) Press Pak packages most generally fail short.

Among the elements of the second class which limit magnitude or rate-of-rise of current are:

1. Source impedance.
2. Transformer impedance.
3. Inductance and resistance of the load circuit.

15.3 CO-ORDINATION OF PROTECTIVE ELEMENTS

Depending upon their complexity and the degree of protection desired, converter circuits include one or more of the various interrupting devices listed above. Functioning of these devices must be coordinated with the semiconductor and with each other so that the overall protection objectives are met. Fuses or breakers must interrupt fault currents before semiconductor cells are destroyed. In isolating defective semiconductors from the rest of the equipment, only the fuse or breaker in series with a defective semiconductor cell should open. Other fuses and breakers in the circuit should remain unaffected. On the other hand, when a load fault occurs, main breakers or fuses should function before any of the semiconductor cell-isolating fuses or breakers function. This fault discriminating action is often referred to as selectivity. In addition, the voltage surges developed across semiconductors during operation of protective devices should not exceed the transient reverse voltage rating of these devices. More complex protective systems require meeting additional coordinating criteria. The example of a protection system and its associated coordination chart described later in this discussion illustrates some of the basic principles of coordination for both overloads and stiff short circuits.

The magnitude and waveshape of fault and overload currents vary with the circuit configuration, the type of fault, and the size and location of circuit impedances. Fault currents under various conditions can generally be estimated by analytical means. References 1, 2, and 3 show analytical methods for calculating fault currents for generally encountered rectifier circuits.

For overloads on rectifier or inverter circuits where the current is limited to a value which the semiconductors can withstand for roughly 50 milliseconds, conventional circuit interrupting devices like circuit breakers and fuses can usually be used satisfactorily for protection. This type of overload can be expected where a sizeable filter choke in the load or a "weak" line limits the magnitude or rate of rise of current significantly or where semiconductor components are substantially oversized. By placing the circuit breaker or fuse in the line ahead of the semiconductors, the protective device can be designed to isolate

the entire circuit from the supply source whenever the line current exceeds a predetermined level which approaches the maximum rating of the semiconductors for that duration of fault.

For time intervals greater than approximately 0.001 second after application of a repetitive overload, the thyristor rating for coordination purposes is determined by the methods discussed in Section 3.6. If the overload being considered is of a type that is expected only rarely (no more than 100 times in the life of the equipment), additional semiconductor rating for overload intervals of one second and less can be secured by use of the surge curve and I^2t rating for the specific device being considered.

The surge characteristic is expressed as the peak value of a half-sine wave of current versus the number of cycles that the semiconductor can handle this surge concurrent with its maximum voltage, current, and junction temperature ratings. In circuits that do not impose a half-sine wave of fault current on the semiconductors, the surge curve can be converted into current values that represent the particular waveshape being encountered.[4] The surge curve for the semiconductor can be converted to different waveshapes or different frequencies in an approximate, yet conservative, manner for this time range by maintaining equipment RMS values of current for a specific time interval. For example, the peak half-sine wave surge current rating of the C35 SCR for 10 cycles on a 60 Hz base is shown on the spec sheet to be 88 amperes. For a half-sine waveshape, the RMS value of current over the complete cycle is one-half the peak value, or 44 amperes. To convert this to average cell current in a three-phase bridge feeding an inductive load (120-degree conduction angle), divide this RMS value by $\sqrt{3}$. ($44 \div \sqrt{3} = 25.4$ amps). To determine the total load current rating for a bridge using this cell, multiply the average cell current by 3. ($25.4 \times 3 = 76.2$ amps).

15.4 PROTECTING CIRCUITS OPERATING ON STIFF POWER SYSTEMS

Conventional circuit breakers and fuses can be designed to provide adequate protection when fault currents are limited by circuit impedance to values within the semiconductor ratings up to the time when these protective devices can function. However, circuits requiring good voltage regulation or high efficiency will usually not tolerate high enough values of series impedance to limit fault currents to such low values unless substantially oversized semiconductors are used. When a fault occurs in a circuit without current limiting impedance, current will develop in a shape similar to the dashed line in Figure 15.2. Its rate of rise is limited by the inductance inherent in even the stiffest practical systems. If the peak available current substantially exceeds the semiconductor ratings, and if it is permitted to flow in the circuit, the semiconductor would be destroyed before the current reaches this first peak. Conventional circuit breakers and fuses will not function quickly enough. Instead, "current limiting" fuses which melt extremely fast at high levels of current are used. Alternately, "electronic circuit breakers" of the type discussed in Section 8.8 can be designed for this purpose.

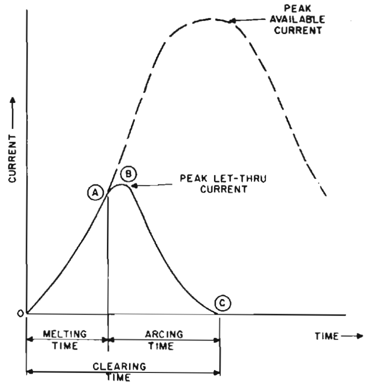


FIGURE 15.2 LIMITING ACTION OF CURRENT LIMITING FUSE

15.4.1 The Current Limiting Fuse

The terms "current-limiting" fuse applies to a fuse which, when used within its current-limiting ratings, limits the peak let-through current to a value lower than that which would overwise flow in the circuit. The action of a typical current limiting fuse is indicated in Figure 15.2. Melting of the fuse occurs at point A. Depending on the fuse design and the circuit, the current may continue to rise somewhat further to point B, the peak let-through current. Beyond this point the impedance of the arcing fuse forces the fault current down to zero at some point C.

The interruption ratings become very important when applying fuses to power systems having high fault current capability. A fuse with an interruptive rating less than the fault capability of the system at the location of the fuse may not be able to interrupt a short circuit within its clearing I^2t and peak let-through rating, resulting in damage to the power semiconductor it is protecting.

It becomes obvious that time and current are the controlling factors in the function of fuses, and the time-current let-through characteristics of the fuse must conform to the time-current rating of the SCR the fuse is protecting. References 4, 5, 6 and 7 discuss in detail the behavior and characteristics of current limiting fuses based on specified conditions of physical surroundings, circuit parameters and fuse design. A practical method of coordinating fuse characteristics to that of SCR's under specified conditions[7,8] is discussed in the following section.

15.4.2 Fuse-SCR Coordination in AC Circuit

Before setting down a set of logical design steps let's look at a typical fuse-SCR circuit (Figure 15.3) in order to define terms and become acquainted with typical waveshapes. Assume a fault across

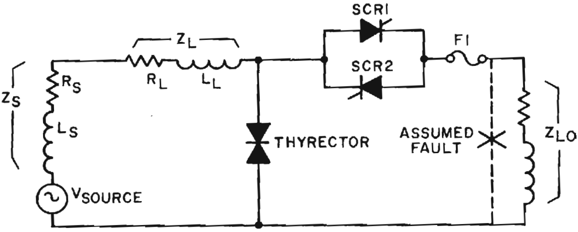


FIGURE 15.3 TYPICAL FUSE-SCR CIRCUIT

the load impedance Z_{LO}. In Figure 15.4 this fault is shown taking place close to the instant of peak source voltage. This is the most stringent condition for the fuse to interrupt under large prospective fault current conditions and high circuit X/R ratios.

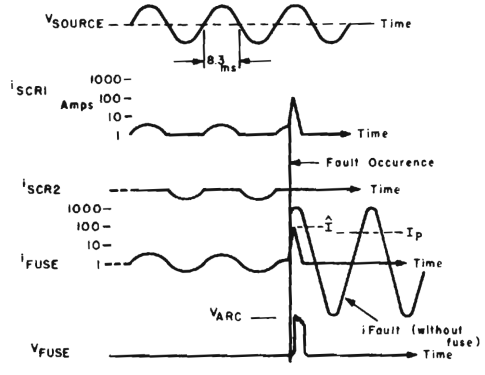


FIGURE 15.4 CIRCUIT WAVEFORM OF FIGURE 15.3 UNDER STEADY STATE & TYPICAL TRANSIENT FAULT CONDITIONS

X/R ratio as used here refers to the ratio of the series reactive to resistive elements of the circuit when shorted. Since the series reactive component in power circuits is nearly always inductive, the ratio of X/R is a relative measure of the energy a circuit can store.

Since this energy must be absorbed by the fuse in its arcing phase it serves as an indication of the severity of the current quenching duty placed upon the fuse. Figure 15.5 shows a close-up of the fuse action shown in Figure 15.4.

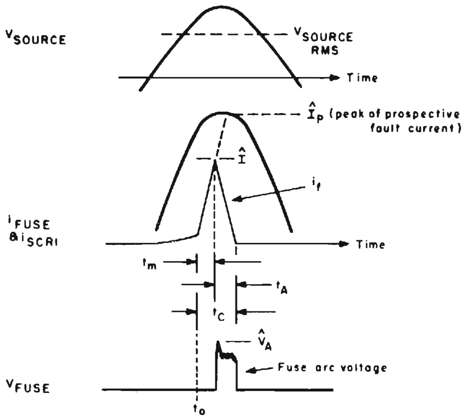


FIGURE 15.5 CIRCUIT WAVEFORMS DURING FUSE CLEARING INTERVAL

The fuse current waveform is typically triangular in shape with an effective pulse width of t_c seconds and a peak of $\hat{I}$ amperes. It is important to note that t_c can vary from less than ½ ms to greater than 8 ms in 60 Hz circuits, while the variation in $\hat{I}$ is typically from 10 to 100 times fuse RMS rating. $\hat{I}$ and t_c are the parameters that determine the destructive effects of the short circuit current, both on the semiconductor and on other circuit components.

15.4.2.1 Fuse Ratings

Fuse manufacturers generally give only the following data:

- Values of I^2t at different RMS circuit voltages and prospective fault currents
- Peak let-through current curves vs RMS prospective current
- Melting time vs RMS current curves

The latter curve's time values shouldn't be confused with t_c since the values given for melting time rarely extend below 10 ms and the time values are for melting time only — not complete fuse clearing time. Thus, these curves are not very useful for short circuit current evaluation of fuse behavior. They are valuable only for long term fuse overload conditions.

Figures 15.6 and 15.7 show typical fuse performance in a 480 V circuit. These two curves when taken together characterize the fuse as a function of the circuit parameters, V_{SOURCE} and I_p. For a given I_p, t_c can be found by solving Equation 15.3.

$$t_c = \frac{3\,(I^2t)}{\hat{I}^2}$$

Both $\hat{I}$ and t_c as a function of circuit parameters can be found from the fuse manufacturer's data.

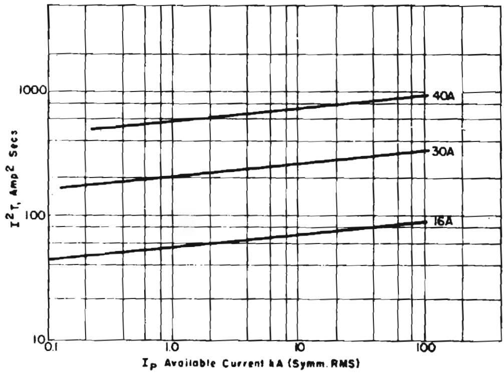


FIGURE 15.6 FUSE PERFORMANCE IN 480 V RMS CIRCUIT

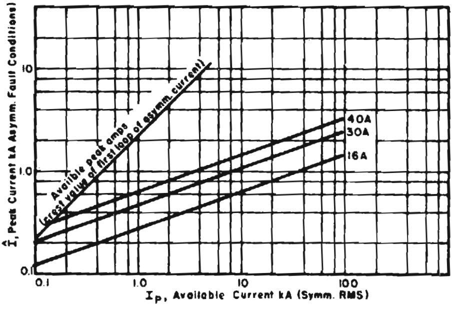


FIGURE 15.7 FUSE PERFORMANCE IN A 480 V RMS CIRCUIT

Figure 15.9 is provided to aid in the conversion of data from the format consisting of Figures 15.6 and 15.7 to 15.8 which provides a common basis of comparing SCR capability with fuse let-through performance.

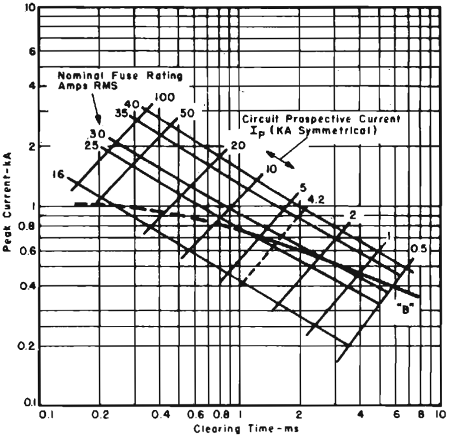
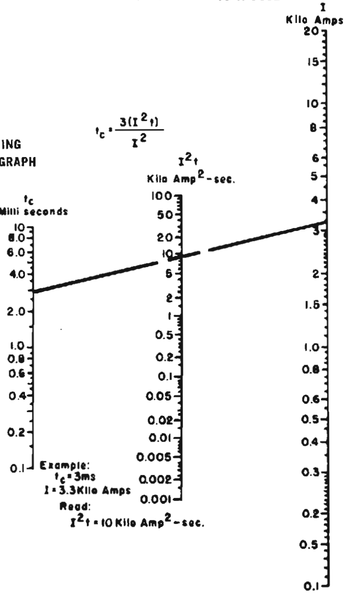


FIGURE 15.8 FUSE-SCR APPLICATION CHART. THE FUSE PORTION OF THE CHART IS DERIVED FROM FIGS. 15.6 AND 15.7 AND THE NOMOGRAPH SHOWN IN FIG. 9. TABLE 1 SHOWS THE DERIVATION PROCEDURE FOR THE 16 A FUSE LINE

FIGURE 15.9 FUSE CLEARING TIME NOMOGRAPH



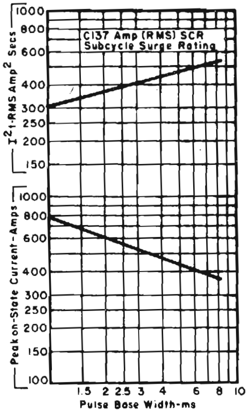


FIGURE 15.10 I^2t AND I VS PULSE WIDTH FOR A 35 A RMS SCR

Fuse circuit definitions

- t_m Fuse melting time
- t_A Fuse arcing time
- t_c $t_m + t_A$ fuse clearing time
- $\hat{I}$ Peak instantaneous fuse let-through current

$$\hat{I} = \sqrt{2}\,\frac{V_{source}}{Z_s + Z_L} \tag{15.1}$$

Maximum symmetrical rms circuit fault current
Abbreviated prospective current

- V_A Peak fuse arc voltage
- i_f Instantaneous fuse current

$$I^2t_c = \int_{t_o}^{t_o + t_c} i^2_f\, dt = \text{clearing } I^2t \tag{15.2}$$

$$= I^2t_m + I^2t_A$$

$= (\hat{I}^2/3)\, t_c$ for a triangular waveform
Note: I as used in I^2t_c is a rms current value.

For a triangular waveform:

$$I^2t = \frac{\hat{I}^2 t_c}{3} \tag{15.3a}$$

And for a half sinusoidal waveform:

$$I^2t = \frac{\hat{I}^2 t_c}{2} \tag{15.3b}$$

$$\hat{I} = \sqrt{2\,\frac{(I^2t)}{t_c}}^{\,*} \tag{15.4}$$

*sinusoidal waveform I^2t value

Available fault current symmetrical RMS
(Prospective current I_p) in kA

		0.5	1	2	5	10	20	50	100
1) From Figure 15.6	I^2t (A^2s)	52	55	60	65	70	77	85	90
2) From Figure 15.7	$\hat{I}_I$ (kA)	0.21	0.265	0.34	0.47	0.6	0.79	1.1	1.3
3) Data from 1, 2 above using Figure 15.9	t_c (ms)	3.5	2.5	1.6	0.9	0.58	0.37	0.21	0.16

Fuse data conversion from manufacturer's data sheet to fuse-SCR application chart. 480 V circuit voltage, 16 A fuse.

TABLE I

A list of fuse manufacturers supplying current limiting fuses is given in Table II.

General Electric Company
Power Systems Management Department
6901 Elmwood Avenue
Philadelphia, Pennsylvania 19142

Bussmann Manufacturing Division
McGraw-Edison Company
St. Louis, Missouri 63100

Chase-Shawmut Company
347 Merrimac Street
Newburyport, Massachusetts 01950

English Electric Corporation
One Park Avenue
New York, New York 10016

Carbone-Ferraz Inc.
P. O. Box 324 (Elm Street)
Rockaway, New Jersey 07866

TABLE II MANUFACTURERS OF CURRENT LIMITING FUSES

15.4.2.2 SCR Rating For Fuse Application

SCR rating data for use with fuses is provided by means of sub-cycle surge curves as discussed in Section 3.5.5 and shown in Figures 3.8 and 15.10. Note the curves are provided for half sinusoidal pulse waveshapes for testing convenience. Since the fuse let-through current waveshape is triangular the designer must account for the difference in waveshape upon SCR surge capability. From test results and analytical studies it has been shown that matching SCR peak current capability with that of the fuse let-through capability provides a conservative basis for SCR protection by means of current limiting fuses. Use of I^2t provides a gross error if matched directly. That is: an SCR can typically withstand a current surge having a sinusoidal waveshape I^2t value that is 150% higher than that of a triangular current surge waveshape of the same pulse base width.

15.4.2.3 Selecting a Fuse For SCR Protection

Fuse selection is simplified by plotting SCR sub-cycle peak current capability (obtained directly from the SCR data sheet), directly over a family of fuse characteristics (for the given circuit voltage conditions) as shown in Figure 15.8; [formerly the RMS current was given. (If using an old data sheet convert RMS to peak current prior to plotting.)] A fuse current rating is then selected such that the SCR rating curve exceeds that of the fuse let-through current rating curve under worst case circuit prospective current conditions.

The reason for showing the semiconductor curves dotted below 1 ms results from a lack of vigorous test data on the semiconductor's short term surge capability in the 100 to 1000μs range. It is known that due to di/dt restrictions, peak current capability of an SCR is reduced below approximately 100μs pulse width. Until firm test data is available, use discretion in this range.

Worked Example

Referring to Figure 15.3 assume

1. The source transformer is rated 100 KVA with 5% short circuit impedance.
2. To select a fuse/SCR combination in a 480 volt RMS circuit with a 20 ampere RMS load. The fuse must be able to protect the SCR in case of a fault occurring across the load.

Design Steps

1. Choose the SCR. Based upon voltage and current considerations a C137 is chosen with a case temperature of 90°C at 9 amperes average per SCR to deliver a 20 ampere RMS load current.
2. Obtain Figure 15.8 information from fuse manufacturer or plot from manufacturer's data of the form shown in Figures 15.6 and 15.7.
3. Superimpose on it the C137 sub-cycle surge current data derived from SCR data sheet.
4. Calculate the maximum RMS symmetrical available short circuit (prospective) current assuming that the transformer react-

ance is the only available short circuit impedance

$$I_A = \frac{KVA}{P.U.\ Impedance \times KV} = \frac{100}{(.05)\,(.480)} \cong 4.2\ KA$$

5. Select the fuse. The fuse current rating must be greater than the load current but must limit the maximum let-through current to a value below the sub-cycle surge current capability of the SCR. In this case a fuse rating of 25 amperes will properly protect the SCR.
6. Check fuse manufacturer's data to determine fuse arcing voltage. In many circuits it should not exceed the SCR's rated voltage as SCR's adjacent to the device being protected may be called upon to block the fuse arcing voltage.
7. To avoid nuisance fuse blowing mount the fuse such that the SCR does not contribute to fuse heating. Provide thermal isolation by providing adequate distance between SCR connections and that of the fuse.

15.4.3 Fuse-SCR Coordination in DC Circuits

The fundamental problem in applying fuses for the protection of SCR's in either AC or DC circuits is to ensure that the fault let-through energy comes within the withstand capability of the SCR under all circumstances which can arise in service. Protection can only be applied to the extent that the essential parameters and conditions to be met can be identified and specified in the properly related terms. In the case of AC applications, the parameters on which the SCR withstand capability is normally compared to the fuse are:

1. Peak let-through current (and thus available current) versus clearing time
2. Clearing I^2t (in absence of #1)
3. Applied voltage
4. Power factor

In the case of DC applications, the essential parameters become:

1. Peak let-through current versus clearing time
2. Clearing I^2t (in absence of #1)
3. Applied voltage
4. Rate of rise of fault current, di/dt
5. Time constant

The fuse interrupting behavior in AC and DC circuits is essentially different, consequently there is simply no relationship between AC and DC fuse performance. It is therefore necessary for fuse manufacturers to supply separate DC peak let-through current values in relation with fuse clearing time in order to coordinate with the SCR's sub-cycle capability. Figures 15.11 and 15.12 show one manufacturer's method of relating energy, current and time coordination in terms of fuse design and circuit parameters. Based on these figures a fuse-SCR coordination curve, Figure 15.13, can be easily plotted. The DC fuse-SCR coordination curve can be interpreted and applied in a similar way as that of the AC curve discussed in the previous section.

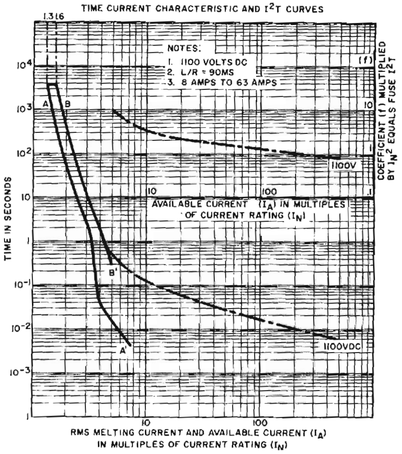


FIGURE 15.11 TIME CURRENT CHARACTERISTIC AND I²t CURVES

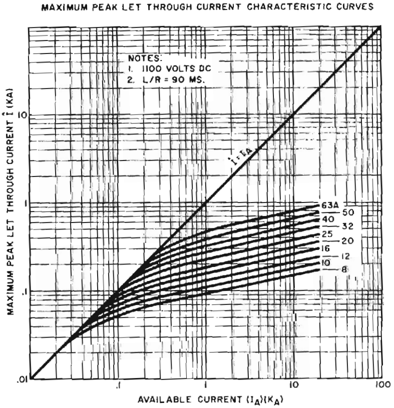


FIGURE 15.12 MAXIMUM PEAK LET THROUGH CURRENT CHARACTERISTIC CURVES

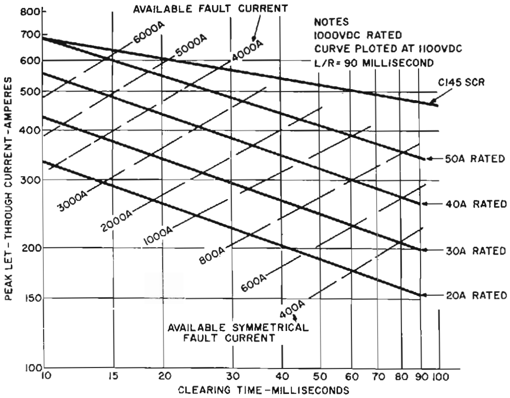


FIGURE 15.13 DC FUSE-SCR COORDINATION CURVE

15.5 INTERRUPTED SERVICE TYPE FAULT PROTECTION WITHOUT CURRENT LIMITING IMPEDANCE

By inserting the protective device in the AC lines feeding a semiconductor AC to DC converter, protection can be provided both against DC faults and semiconductor device faults if there is no possibility of DC feed into faults of the semiconductor devices themselves. DC feed into cell faults will occur in single-way circuits when other power sources feed the same DC bus or when the load consists of CEMF types of loads such as motors, capacitors, or batteries. The following is an example of this type of AC line protection in a circuit without current limiting impedance. Upon functioning of the protective system, the circuit is interrupted and shut down.

Worked example: Referring to Figure 15.15

Assume:
- 120 V RMS AC supply, 60 Hz.
- Single-phase bridge employing two C35H SCR's for phase control in two legs and two 1N2156 diode rectifiers in the other two legs. See Figure 15.14.
- Maximum continuous load current = 12 amperes.
- Choke input filter.
- Line impedance negligible. Peak available fault current in excess of 1000 amperes.
- Maximum ambient = 55°C free convection. Each semiconductor mounted to a 4″ x 4″ painted copper fin 1/16″ thick.

Requirements for Protective System:
- Protection system must be capable of protecting

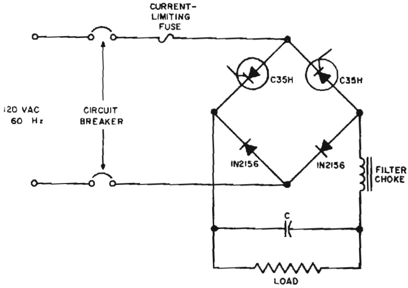


FIGURE 15.14 FAULT PROTECTION CIRCUIT

SCR's and diodes against overloads, DC shorts, and shorting of individual semiconductors. System can be shut down when any of these faults occurs.

Solution: – Since the current rating of the 1N2156 is higher than the C35 both at steady-state and under overload, the protection, if properly coordinated with C35, will be ample for protecting the 1N2156 also. Using the data for a C35 on a 4″ x 4″ fin given in Figure 3.4 for a C34 (the C35 thermal characteristics are identical to the C34) and the load current rating equation in Figure 3.9(e) which applies for the continuous square wave of current experienced in a single-phase circuit with inductive load.

$$P_{OL} = \frac{125 - 55}{\frac{0.0083}{0.0167} \times 5.1 + \left(1 - \frac{0.0083}{0.0167}\right) 0.4 - 0.35 + 0.2}$$

= 27 watts maximum peak heating allowable per SCR on steady-state basis.

From the specifications for the C35, this level of heating will be developed by 18 amperes peak or 9 amperes average load current at 180 degree conduction angle with a rectangular current waveshape. Under inductive load conditions, the maximum steady-state RMS rating of the complete circuit is equal to the peak rating of each SCR = 18 amperes. Assuming that faults and overloads will be superimposed on the steady-state equipment rating of 12 amperes, the semiconductor overload rating can be calculated from Figure 3.9(f).

$$P_{OL} = \frac{T_J - T_A - P_{CD} \times R_\theta}{R\Theta_{(t)}} + P_{CD}$$

For example, for 10 seconds the SCR can dissipate the following power without its junction exceeding 125°C:

$$P_{OL} = \frac{125 - 55 - 8 \times 5.1}{2.2} + 8 = 21.3 \text{ watts/cell}$$

Average current rating per cell = 13.3 amps (from specification sheet).
Rated bridge output current = 2 × 13.3 = 26.6 amps RMS.

This point and others calculated by the same means are plotted on the coordination chart of Figure 15.15. Overload ratings achieved by this technique limit junction temperature to 125°C.

For non-recurrent types of overload as typified by accidental short circuits and failure of filter capacitors, the SCR is able to withstand considerably higher overloading as specified in the multi-cycle surge current ratings. A typical point of this kind can be calculated as follows. At 0.1 second, a time which is equivalent to 6 cycles on the surge curve, the peak surge current rating of the C35 is 92 amperes. The RMS bridge rating is $92 \div \sqrt{2} = 65$ amperes. This curve blends into ratings determined from the I^2t rating below approximately 50 milliseconds. The I^2t rating of the C35 is 75 amps²-sec. At .001 second, the current rating of the SCR is

$$\sqrt{75 \text{ amps}^2\text{-sec.}/.001 \text{ sec.}} = 274 \text{ amps RMS}$$

Below ½ cycle, the rating of a single SCR and the rating of the bridge are identical. Thus, at .001 second, the bridge is rated 274 amps RMS also.

To afford protection against short circuits of the load and shorted semiconductors in this type of circuit, a current limiting fuse is required.

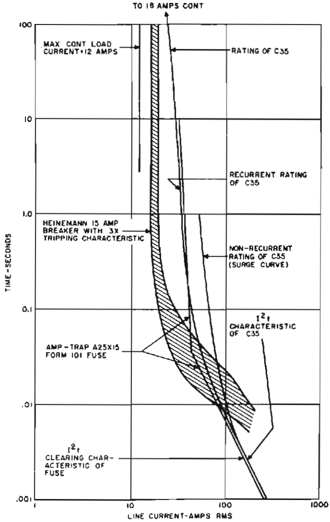


FIGURE 15.15 CO-ORDINATION CURVE FOR EXAMPLE OF FAULT PROTECTION

15.6 NON-INTERRUPTED SERVICE UPON FAILURE OF SEMICONDUCTOR

In the foregoing discussion and example, the semiconductors are protected against overloads and short circuits of the output and also against the fault currents that occur if another semiconductor in the circuit should short. Protection is afforded by disconnecting the entire circuit from its supply voltage.

In some types of service such as high reliability military systems and continuous industrial processes, a service interruption due to a semiconductor failure cannot be tolerated regardless of how remote this possibility may be. To maintain service under these conditions requires redundancy of semiconductors and a means of disconnecting faulty cells whenever failure of a semiconductor occurs. It has been observed that, when failures of SCR's have occurred, they could be classified into three main categories:

1. Loss of reverse blocking ability. In rectifier circuits this generally causes a high fault current to flow.
2. Loss of off-state blocking ability. In a rectifier circuit, this will generally result in loss of control of output voltage, the SCR remaining in the forward on-state.
3. Failure to fire or switch into the forward conduction state. This will also result in loss of control of output voltage since the SCR will remain in the off-state.

   (Conditions 1 and 2 may be combined in a short-circuited device.)

Figures 15.16 and 15.17 suggest two of several possible methods of detecting and isolating defective SCR's from the circuit without interrupting the flow of controlled power to the load. Figure 15.16 illustrates a single-phase centertap phase-controlled power supply in which the SCR's in each leg of the circuit are grouped into pairs of parallel-matched cells. A low value of resistance R is connected in series with each SCR. The value of R is selected to limit fault current through good SCR's if one SCR loses its reverse blocking ability. The contacts of an isolating circuit breaker are connected in series with each pair of SCR's. The trip coil of each breaker or the coil of a pilot relay is connected across the bridge formed by the pair of SCR's and

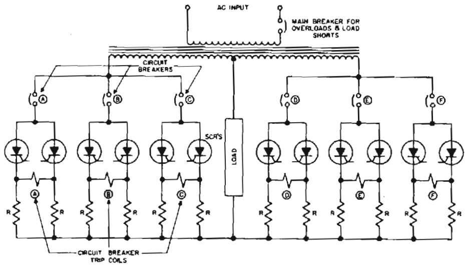


FIGURE 15.16 PARALLEL SCR PAIRS FOR NON-INTERRUPTED SERVICE

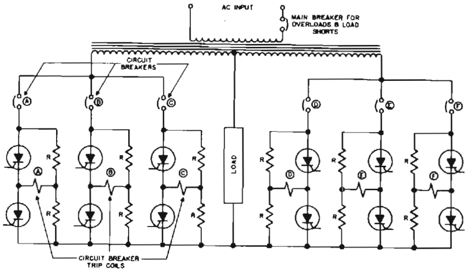


FIGURE 15.17 SERIES SCR PAIRS FOR NON-INTERRUPTED SERVICE

their respective series resistors. When both SCR's of a pair are functioning properly and therefore identically, the instantaneous currents through the SCR's and their series resistors are essentially equal and therefore no current flows through the circuit breaker trip coil. If either SCR in a pair fails in any one or more of the three modes enumerated above, unequal currents will flow for at least part of each cycle through the SCR's. Current will flow through the trip coil associated with that SCR pair, tripping the series circuit breaker and isolating the pair from the main circuit. As long as the remaining SCR's in that leg of the circuit are capable of handling the full load current, the circuit will be capable of continuing operation indefinitely. The circuit breakers can be used to actuate an alarm or annunciator scheme to warn the equipment operator of the failure so that he can replace the faulty SCR during a scheduled maintenance shutdown of the equipment.

The circuit shown in Figure 15.17 is more economical than Figure 15.16 for circuits requiring high output voltages rather than high currents. In this circuit the SCR's are grouped in series-connected pairs for the purpose of handling higher voltages. A resistor R is connected in shunt with each SCR to assist in voltage sharing and to provide in conjunction with the pair of SCR's a bridge across which to connect the circuit breaker trip coil. When both SCR's are functioning properly, only the difference in leakage currents between the two SCR's flows through the trip coil. When either SCR in a pair malfunctions for one of the reasons cited earlier, a substantial current will flow for at least part of the cycle through the trip coil, thus opening the circuit breaker and isolating that pair of SCR's from the circuit. In order that the trip coil will reliably discriminate between the normal leakage balancing current of the SCR's and the unbalance current resulting from a faulty SCR, it may be necessary to reduce the value of each resistor R somewhat below the value otherwise adequate for forcing voltage sharing between the SCR's.

Proper functioning of the type of protection shown in Figures 15.16 and 15.17 requires that:

1. None of the circuit breakers in series with the SCR's should trip on DC overloads or faults. Separate protection in the AC or DC lines should disconnect the load from the supply voltage for this type of fault.

2. Adequate SCR and circuit breaker capacity should be provided to handle the maximum load current with one of the parallel paths removed from the circuit by operation of a breaker.
3. In isolating a pair of SCR's, the circuit breaker must cut off the current at a slow enough rate so that induced voltage (L di/dt) does not exceed the transient voltage rating of the SCR's in parallel with that pair. If they occur, excessive transients peaks may be reduced to tolerable levels by means of transient suppression techniques. (Refer to Chapter 16.)

15.7 OVERCURRENT PROTECTION USING GATE BLOCKING

In many phase-controlled and inverter type circuits, SCR's and other circuit components can be protected against overcurrent conditions by removing the gate triggering signal from the main power handling SCR's, as soon as excessive current is detected in the circuit. In a phase-controlled system, this will result in fault interruption within one-half cycle after the gate signal has been interrupted since the line voltage reversal will commutate (turn-off) the fault current. In an inverter type of circuit operating from DC without line commutation, the gate signal must be interrupted while the current is still low enough to be commutated by the circuit parameters.

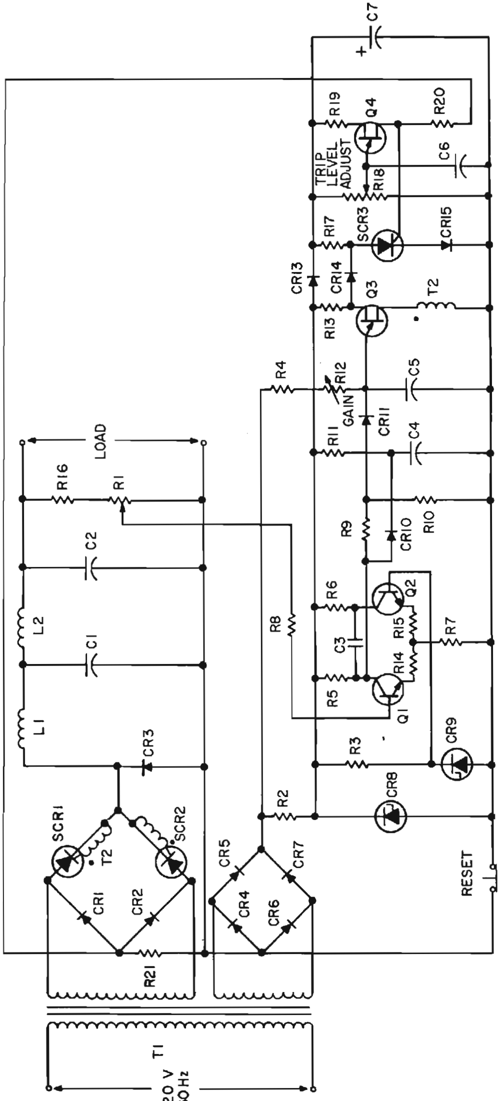
Figure 15.18 illustrates a typical gate blocking circuit as applied to the phase-controlled voltage regulator. Under normal operation UJT Q3 develops triggering pulses which are coupled to the gates of SCR1 and SCR2 through pulse transformer T2. The triggering angle and, therefore, the average load voltage are controlled by the feedback action of the differential amplifier Q1 and Q2 on the pedestal height of the voltage waveform on capacitor C5. The UJT Q4, SCR3, a current-sensing resistor R21, and associated components are added to the basic voltage regulator to provide the overcurrent protection feature.

Normally the voltage on the emitter of Q4 is slightly below the peak point triggering level of the UJT, as set by the "Trip Level Adjust" potentiometer. When an overload occurs, the additional voltage drop across R21 drops the voltage on Base 1 of UJT Q4, thus reducing the critical level of voltage required on the emitter to trigger this UJT. If the overload is sufficiently high, Q4 triggers SCR3 and thereby shorts out through CR9 the interbase power supply to UJT Q3. This locks out Q3 from further triggering of the main SCR's in the regulator. SCR3 remains conducting, and the load voltage remains interrupted until the "Reset" button is depressed.

Similar gate blocking circuits for protective purposes can be devised for other types of thyristor applications where the rate-of-rise of fault current is not excessive and where means for commutating this current are available.

15.8 OVERCURRENT PROTECTION CIRCUIT

When the fault currents due to short circuits may reach destructive proportional levels beyond the "time-current" capability of available fuse to interrupt, in other words, when fuse cannot clear the fault



CR8 – IN1776
CR9 – IN1767
CR10 – IN5060

SCR3 – G-E C106Y
Q4 – G-E 2N2646
R17 – 330 Ω

R18 – 1 MEG POT, 2 W.
R19 – 1K, 1/2 W.
R20 – 22 Ω, 1/2 W.

R21 – 0.007 Ω, 5 W.
C6 – 0.04 MFD
C7 – 100 MFD, 30 WVDC G-E 62F403

FOR OTHER PARTS, SEE FIG. 12.23

FIGURE 15.18 PHASE CONTROLLED D.C. POWER SUPPLY WITH OVERCURRENT TRIP

current fast enough, a form of electronic crowbar circuit shown in Figure 8.20 can be very useful. When a fault condition develops in the load, the crowbar circuit will shunt away the fault current in a few microseconds for a finite time interval until the interruption of the fault current can be performed by conventional means such as by circuit breaker or fuse.

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16 VOLTAGE TRANSIENTS IN THYRISTOR CIRCUITS

In an SCR controlled power system, in order to fully utilize the SCR's capabilities, it is essential to protect SCR's against effects of overvoltages whether they may be of a transient or long-time duration nature. A good working knowledge of the magnitude and energy content of overvoltage in the system may often spell the difference between success and failure of the application. Any switched energy storage system is a potential source of overvoltage. If the voltage is high enough above the blocking voltage of the SCR, destruction may follow either from energy initially stored in the system or by the fault current which follows as a consequence of the breakover. A number of common voltage transients occur in electrical systems including lighting surge, switching transients from elsewhere in the system, switching transients within the control elements themselves, and regenerative voltages, to name a few. The effects of overvoltages on an SCR can be either degrading or catastrophic. A catastrophic failure usually manifests itself immediately upon the incidence of the overvoltage to the SCR. However, it is also possible for degradation of the SCR to occur causing latent defects resulting in failure at some future time. Consequently, for system reliability as well as economic reasons, it is a good design practice to provide the correct means of preventing possible overvoltages from damaging the SCR's. This can be accomplished by operating SCR's well below their voltage ratings to provide a factor of safety against long time duration overvoltages and by using additional circuit elements to suppress transient overvoltages at the SCR terminals to a safe level.

Because of the profound influence of voltage transients on successful and reliable operation of SCR circuits an understanding of the sources of transient voltages and the means of reducing them is essential. Thoughtful design practices can then achieve optimum and economical use of the ratings of semiconductor components.

16.1 WHERE TO EXPECT VOLTAGE TRANSIENTS[1,2,3]

In the following discussion transients are considered to be those voltage levels which exceed the normal repetitive peak voltage applied to the semiconductor components. In the more common rectifier circuits operating from an AC source, the repetitive peak reverse voltage (V_{ROM}) applied to the semiconductors is equal to the peak line-to-line voltage feeding the circuit. In inverter circuits and other types of DC switches, the repetitive peak voltage applied to SCR's is a function of the particular circuit and must be analyzed on an individual basis. Either or both forward and reverse voltage may change widely in normal circuit operation as load current, conduction angle, load power factor, etc., are varied.

In general, the effect of transient voltages on SCR's and other thyristors is similar to their effect on conventional silicon rectifier diodes, but it should be kept in mind that a thyristor is capable of acting as a high resistance in the forward direction as well as the reverse. In some instances, this blocking action will prevent transient energy from being delivered to and dissipated in the load unless the thyristor first breaks over in the forward direction.

In addition to random line disturbances such as lightning which have been recorded as high as 5600 volts on a 120-volt residential power line, transient voltages across thyristor circuits may be generated by occurrences such as those described in Figures 16.1 through 16.8. The indicated power semiconductors may be rectifiers, thyristors or a combination of both as shown.

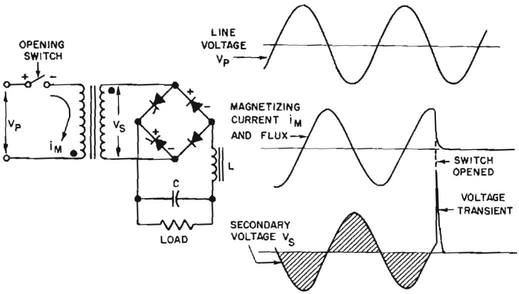


FIGURE 16.1 VOLTAGE TRANSIENT DUE TO INTERRUPTION OF TRANSFORMER MAGNETIZING CURRENT

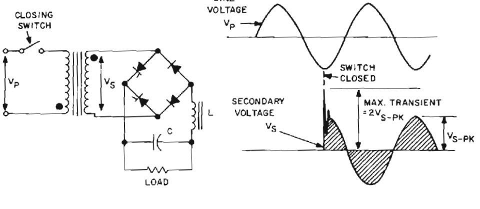


FIGURE 16.2 VOLTAGE TRANSIENT DUE TO ENERGIZING TRANSFORMER PRIMARY

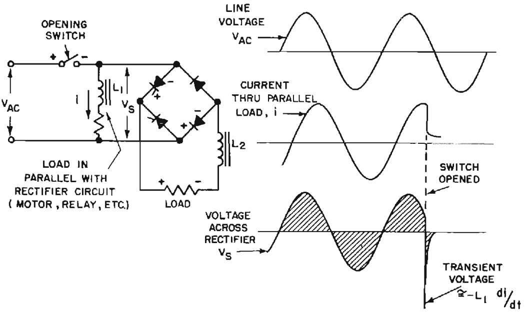


FIGURE 16.3 VOLTAGE TRANSIENT DUE TO SWITCHING CIRCUIT WITH INDUCTIVE LOAD ACROSS INPUT

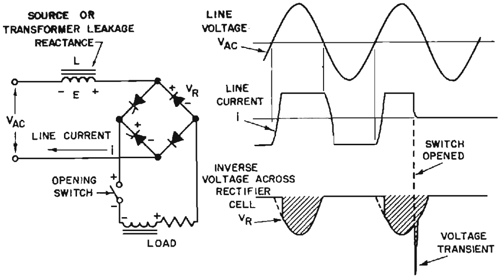


FIGURE 16.4 VOLTAGE TRANSIENT DUE TO LOAD SWITCHING

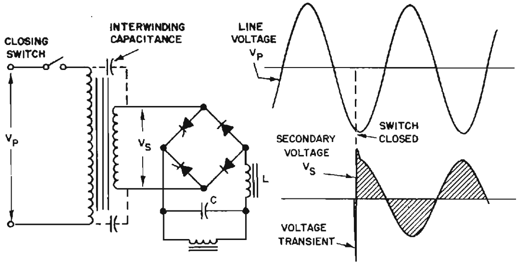


FIGURE 16.5 VOLTAGE TRANSIENT DUE TO ENERGIZING STEP-DOWN TRANSFORMERS

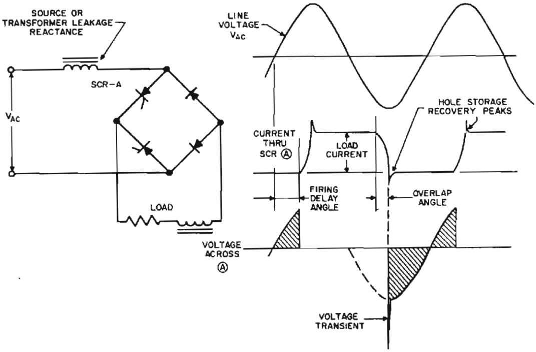


FIGURE 16.6 CYCLICAL COMMUTATION TRANSIENT DUE TO REVERSE RECOVERY OF SCR's AND RECTIFIER DIODES

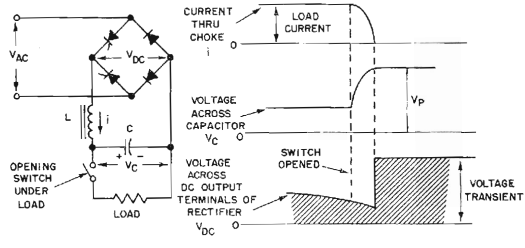


FIGURE 16.7 VOLTAGE TRANSIENT DUE TO DROPPING LOAD FROM EL-TYPE FILTER WITH HIGH L/C RATIO

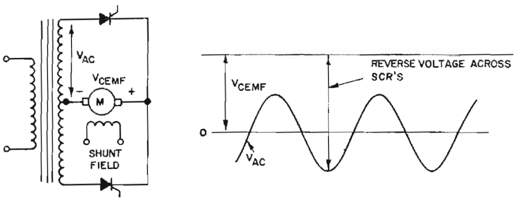


FIGURE 16.8 OVERVOLTAGE DUE TO REGENERATIVE LOAD

16.2 HOW TO FIND VOLTAGE TRANSIENTS

Sometimes the presence of excessive voltage transients in an SCR control circuit is first suspected because of a rash of semiconductor failures in the prototype equipment in the laboratory. Worse yet, these first symptoms sometimes wait until the first equipment is shipped into the field where operating conditions, may on occasion, differ from the conditions that had been successfully passed in the laboratory. When these failures occur at very light loads or immediately following circuit switching, voltage transients should be suspected as the culprit.

Since the search and measurement for possible voltage transients in a circuit may destroy or at least permanently harm semiconductors in the circuit, the anode supply voltage should be reduced to about ¼ or ½ the normal level initially and then gradually increased as measurements indicate the absence or reduction of transients to levels that the semiconductors can withstand.

AC switching transients are usually worst at no load. Therefore, it may be desirable to test the circuit for this type of transient at no load with semiconductors of a lower current rating subsituted for the main devices in order to reduce the cost of components that may be destroyed in the course of the test. Also, the higher blocking resistances of lower current components will aggravate voltage transients and thus will generally make measurements and corrective measures conservative.

16.2.1 Meters

Except for very slow high energy transients, instruments with moving coils as their detecting and indicating means are almost useless in measuring transient voltages because of their high inertia and low input impedance. Of the several transient voltage problems discussed earlier, this type of meter may be useful only in measuring the amplitude of regenerative voltage transients such as those generated by a hoist motor being driven by an overhauling load.

16.2.2 Oscilloscopes

A high speed oscilloscope with long persistence screen is probably the most useful single tool for analysis of voltage transients. For significant results in detecting and measuring all the types of transients that may cause SCR failure, the oscilloscope should have a transient response of at least 0.1 microsecond rise-time and be capable of writing rates in excess of ten million inches per second. Many commercial oscilloscopes meet this specification. A practical screen material is the P11 phosphor. Storage or memory scopes, although handicapped by relatively slow writing speeds and rise-times, are very useful for recording the longer duration types of transients.

For looking at cyclical transients such as those due to reverse recovery effects as discussed in Figure 16.6, the use of a scope is straightforward. In this case, the sweep should be repetitive and synchronized with the power system. However, for nonrecurrent types of

transients due to switching, more careful precautions are necessary. The scope should be equipped with a hood, and for visual inspection the room should be darkened if possible and the eyes of the operator permitted to become accustomed to a low light level. For checking the amplitude of voltage transients visually, it is sometimes more effective not to use a horizontal sweep, but to use instead only the vertical deflection of the trace. Thus, the eyes can be focused on the precise part of the scope face where the transients will appear, if and when they occur.

When a sweep is employed, it can be triggered by the transient itself or by some external means such as an extra contact or interlock on the circuit switch which initiates the transient. By this latter means, the sweep can be initiated before the transient occurs and any doubt about missing an early part of the transient is eliminated.

The objectiveness of studying and measuring non-cyclical types of transients is enhanced if a photographic record is secured in addition to the fleeting image recorded in the mind by the human eye. In many cases, fast film such as Polaroid Type 42, 44, or 47 (exposure index 200, 400, and 3000, respectively) will catch traces that are not perceptible to the eye.

Circuits should be checked for possible destructive voltage transients by connecting the scope input directly across the semiconductor to be checked.

16.2.3 Peak Recording Instruments

Electronic peak recording instruments with a memory can be very useful in checking for transients when their occurrence is random and cannot be predicted.

The ideal voltage measuring equipment for this purpose should indicate amplitude, waveshape and duration, and frequency of occurrence of overvoltages while recording and maintaining this record over long periods of time while unattended. This ideal combination of characteristics is extremely expensive, and difficult if not impossible, to secure in a commercially available instrument.

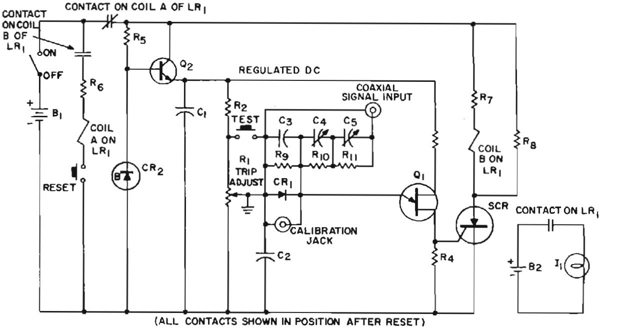
A simple and easy-to-build instrument of this type is discussed here. The primary features of the transient voltage indicator described here are its:

1. Accuracy and Sensitivity . . . 2% of "full scale" down to 1 μsecond pulse duration.
2. High input Impedance . . . 1 megohm shunted by 5 $\mu\mu$f.
3. Wide Voltage Range . . . dependent on voltage divider design.
4. Unattended Operation . . . retains record of transient occurrence up to 12 days.
5. Low Cost
6. Battery Operation . . . portable, unaffected by line disturbances. Records transients caused by power failures, and maintains reading through power failures. Can be operated above ground potential.

The transient voltage indicator acts as a "go-no-go" type instrument. The user presets a level of voltage on the precision potentiometer dial. If this instantaneous voltage is exceeded, the circuit energizes

the indicating lamp which remains lit until the circuit is reset by pushing the reset button.

The electrical circuit shown in Figure 16.9 employs a unijunction transistor, Q1, to compare the input signal with the reference and to actuate the tripping and latching circuits. The unijunction transistor



SCR–GE C220F CONTROLLED RECTIFIER
Q1 – GE 2N490 UNIJUNCTION TRANSISTOR
Q2– GE 2N3416 TRANSISTOR
CR1–GE DT230H RECTIFIER
CR2–Z4X18B ZENER DIODE, 17–21 V
B1– 22 1/2 VOLT BATTERY, BURGESS 4156
B2– 1 1/2 VOLT BATTERY, BURGESS 2FBP
R1–50,000 Ω HELIPOT, SERIES C, 3 TURN
R2– 4700 Ω 1/2 WATT
R3– 470 Ω 1/2 WATT
R4–100 Ω 1/2 WATT
R5– 4700 Ω 1/2 WATT
R6, R7 – 47 Ω 1 WATT
R8 –200 Ω 1 WATT
R9–2500 Ω 1 WATT, 1 % TOLERANCE
R10, R11– 499,000 Ω 1 WATT, 1% TOLERANCE
LR1 - POTTER-BRUMFIELD LATCHING RELAY TYPE KE17D-12V DC
I1–GE TYPE 49 LAMP BULB, .06A, 2 VOLTS
C1–100 MFD, 50V DC ELECTROLYTIC CAPACITOR GE 76F02LN101
C2–2.0 MFD, 200V DC PAPER CAPACITOR GE 8A17B205B
C3–2000 MMFD MICA CAPACITOR
C4, C5–1 TO 7.5 MMF CERAMIC TRIMMER CAPACITORS

FIGURE 16.9 CIRCUIT DIAGRAM OF TRANSIENT VOLTAGE INDICATOR

is an ideal device for these functions since it has a very stable firing point and presents a high impedance to signals below its tripping voltage.

The input signal at which the unijunction transistor Q1 trips is set by potentiometer R1. Figure 16.10 shows a calibration chart which

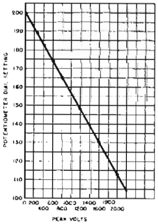


FIGURE 16.10 CALIBRATION CHART FOR TRANSIENT VOLTAGE INDICATOR

defines the input tripping voltage in terms of the potentiometer dial setting. When the unijunction trips, it fires a silicon controlled rectifier SCR, thereby actuating a latching relay LR1 and lighting an indicating lamp I1 in a separate low voltage circuit. At the same time the latching relay de-energizes the tripping circuit from its battery to shut off the controlled rectifier and conserve battery energy.

Depressing the "reset" button energizes the other coil in the latching relay, extinguishing the lamp and readying the circuit for the next trip.

Transistor Q2 in conjunction with reference diode CR2 applies a regulated DC voltage to the unijunction transistor and its bias circuit. Thus battery voltage fluctuation with life do not affect the accuracy of the circuit until the battery voltage drops below the avalanche voltage of CR2.

The voltage signal to be monitored by the equipment is introduced at the coaxial signal input and, depending on the desired voltage range of the instrument, is stepped down by a suitable voltage divider. In this instrument, the signal introduced to the unijunction circuit across resistor R9 is 1/400th of the input voltage, having been stepped down by the RC network consisting of R9, R10, R11, C3, C4, and C5.

Capacitor C2 provides sufficient energy for triggering the SCR. When Q1 triggers, C2 discharges through diode CR1, Q1, and resistor R4.

Tests on the equipment described here showed a maximum error of the dial reading using a 3-turn precision potentiometer that was no greater than 2% of "full scale" for pulses from 1 μsecond duration up to pure DC. Thus, with this 2000 volt instrument maximum error was 40 volts. For pulses of shorter duration than 1 μsecond, the error increases. At ½ μsecond, the maximum error is approximately 5%.

These tests were conducted with a square wave pulse generator furnishing the signal. For peaked voltage waveforms, the instrument reads the voltage level at which the waveform is approximately ½ μsecond wide.

While this instrument has accuracy well beyond instruments many times its cost, and is ample for the purpose intended, it is felt that a substantially higher level of accuracy could be incorporated by using more precise components, a more stable voltage supply, and a better optimized voltage divider.

16.2.4 Spark Gaps

For high voltage systems, calibrated sphere spark gaps can be used to measure the crest values of transient voltages. Current through the spark gap after it has broken down should be limited by a non-inductive resistance (at least one ohm per volt of test voltage) in series with the gap on the grounded side. Suitable overcurrent protective devices should be used to interrupt the power follow-through after the voltage surge has passed. In general, the breakdown voltage level for gaps varies significantly with the waveshape of the voltage being measured as well as with many environmental factors.

16.3 SUPPRESSION TECHNIQUES

Three basic approaches can be employed for the suppression of transient overvoltages:

1) Series suppression
2) Shunt suppression
3) Combination of 1 and 2

Functionally, series transient suppressors act as a series impedance which varies from a low resistance under normal operating conditions to a high resistance when a transient appears; shunt transient suppressors appear as an open circuit under normal operating conditions and become a low-impedance shunt path during a transient. Two distinct advantages of using shunt suppressors in comparison with series suppressors are the absence of insertion loss and simplicity of the circuit arrangement. However, since it presents a low impedance to the transient, the shunt suppressor must be able to absorb large amounts of power for a short duration of time under repetitive pulsed conditions.

The most practical method of suppressing voltage transients is the third approach. By utilizing the available circuit inductance together with a properly designed shunt suppressor, a series-shunt suppression network is formed with the combined advantages of series and shunt suppression. Such a technique will be discussed later.

In general, voltage suppressors may be grouped into two distinct categories: suppression components and suppression networks.

16.3.1 Suppression Components[4,11]

There are many types of voltage suppression components available on the market today. This section will discuss two of the more popular ones applied in SCR controlled power circuits.

16.3.1.1 Polycrystalline Suppressors:

Selenium Thyrectors and Metal Oxide Varistors

Comparable samples of two families of polycrystalline suppressors available to the designer are shown in Figure 16.11. Selenium Thyrectors evolved from selenium diode rectifier technology in the late fifties and early sixties. When arranged in a bipolar configuration by stacking plates of opposite polarity together in a series electrical arrangement the V-I characteristic is as shown in Figure 16.12. While selenium Thyrectors consist of an integral number of plates each having a fixed maximum operating voltage at steady-state conditions as shown on Point A of the curve, General Electric GE-MOV™ Metal Oxide Varistors are fabricated from a ceramic powder by a pressing operation. GE-MOV varistor characteristics depend upon bulk action within the ceramic of the crystal structure. Unlike the selenium suppressor an effective continuous variation of characteristic voltage rating can be achieved by pressing to controlled dimensions (thickness, length, etc.). Similarly to selenium, average power handling capability as well as pulse energy capability is determined by the diameter of the GE-MOV varistor and means used to cool it.

Referring again to Figure 16.12, the slope of the V-I characteristic beyond the maximum rated voltage Point A defines the clamping performance of the suppressor. This slope together with the so-called knee of the linear characteristic is best defined by redrawing the V-I curve on log-log scales as shown in Figure 16.13 where the characteristics of three different families of suppressors plus a resistor are given.

The curves can all be expressed as:

$$I = KV^{\alpha}$$

where K is a device constant

α is the slope of the curve on log-log scales and is defined as:

$$\alpha = \frac{\text{Log}\,(I_2/I_1)}{\text{Log}\,(V_2/V_1)}$$

where I_1 and I_2 are taken a decade apart

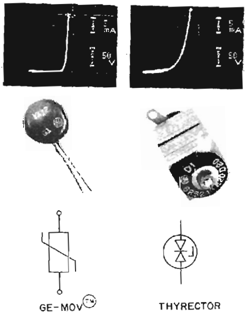


FIGURE 16.11 TWO FAMILIES OF POLYCRYSTALLINE SUPPRESSORS

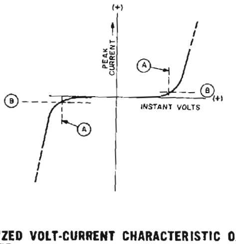


FIGURE 16.12 NON-POLARIZED VOLT-CURRENT CHARACTERISTIC OF POLYCRYSTALLINE SUPPRESSORS

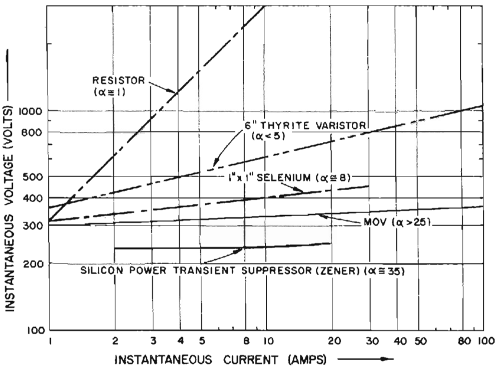


FIGURE 16.13 LOG-LOG VOLT/AMPERE CHARACTERISTICS OF COMMON VOLTAGE SUPPRESSORS

Both selenium Thyrectors and GE-MOV varistors are thus seen to be voltage dependent symmetrical resistors having a high degree of non-linearity. Terminal impedance at voltages lower than nominal are very high while impedance progresses to an extremely low value as voltage is increased to a model's upper range, providing the desired suppressing or clamping function. Thus polycrystalline suppressors provide a means of absorbing transient energy pulses while limiting the rise of transient voltage in the circuit to controlled levels.

An examination of a typical SCR controlled circuit will illustrate the usefulness of such a device. Consider the single phase bridge circuit in Figures 16.1 and 16.2. Transient voltages may result from either switching on or off the primary of the transformer. The voltage applied to the SCR AC terminals is the voltage appearing at the transformer secondary winding. If the transformer magnetizing current is interrupted at its peak, the SCR's may be subjected to a transient voltage up to ten times the normal peak secondary voltage of the transformer (Figure 16.1). On closing the primary circuit at the peak of the voltage wave SCR's may be subjected to a voltage transient double that of the normal peak secondary voltage of the transformer (Figure 16.2).

By connecting a suppressor across the secondary winding of the transformer, the voltage transient appearing at the SCR AC terminals will be limited. In order to assist engineers in selecting the proper suppressor for this application, the following design outline is given:

Suppressor Selection Guide for Transformer Circuit Applications:

1. What voltage should be used?
   a) Determine *maximum* steady state RMS voltage that will be applied to the suppressor and specify the same or closest

higher rating. For non-sinusoidal voltages, use recurrent peak voltage ratings.

2. What clamping voltage will be obtained?
   a) Determine maximum peak current that will be carried by the suppressor. In transformer circuits this is the peak magnetizing current (i_M) X transformer turns ratio. For most cases assume $i_M = I_E \times \sqrt{2}$ where I_E = exciting current which is the no load RMS input current read at max. RMS design voltage. Check to see that i_M does not exceed rated peak current value of suppressor chosen.
   b) Using Figure 16.14, read the suppressed peak voltage ratio at peak current and multiply times the recurrent peak voltage spec of the chosen model in the max. rating table of the pertinent data sheet.
3. What energy rating is required?
   a) $E = \frac{1}{2} L_M i_M^2$ where L_M is the equivalent magnetizing inductance.
   b) $L_M = \frac{X_{LM}}{2\pi f}$ where $X_{LM} = \frac{\text{Primary Voltage}}{I_M}$ (RMS) and $\left(I_M = \frac{i_M}{\sqrt{2}}\right)$
   c) Choose model with an energy rating higher than the calculated value.
4. What is the power dissipation?
   a) For repetitive pulses:
      Avg. Pwr = Energy/pulse × Rep. Rate
   b) Make sure the specified power capability of the device is not exceeded and is properly derated.

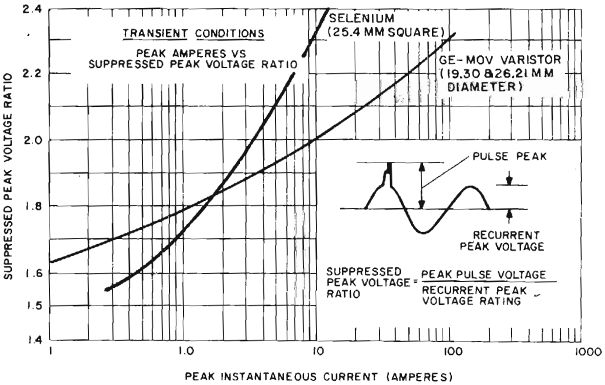


FIGURE 16.14 POLYCRYSTALLINE SUPPRESSION RATIO CURVES

Table 16.1 lists the major design parameter capabilities of two comparably sized polycrystalline suppressors. Larger sizes are available having higher transient energy handling properties. For further information consult device data sheets.

RMS Voltage Rating	Non-Repetitive Energy Dissipation Watt-Seconds		Max Average Power Dissipation Watts		Max Peak Transient Current Amperes		Standby Current Drain at Max Rated Peak Voltage Milliamperes	
	1" Thyrector Max T_A = 100°C	¾" MOV Max T_A = 85°C	1" Thyrector Max T_A = 25°C	¾" MOV Max T_A = 85°C	1" Thyrector 1 ms Max Pulse Width	¾" MOV 7 µs Max Pulse Width	1" Thyrector	¾" MOV
130	4	10	12	0.5	30	1000	12	1
250	8	20	20	0.6	30	1000	12	1
480	16	40	40	0.7	30	1000	12	1

TABLE 16.1 COMPARISON OF 1" THYRECTORS WITH ¾" GE-MOV VARISTORS

Being able to limit voltage transients to a controlled value, a circuit designer can add value to the application by increasing reliability and life of the components protected thus providing additional margins of safety and reliability to the equipment and user.

Although suppression components, such as Thyrector diodes, metal oxide varistors and others, are effective in clipping voltage transients to a designed level, they do very little to limit the rate of change of the transient voltage. Since SCR's are sensitive to the forward applied dv/dt, if an excessive rate is applied, it may turn-on without having a gate signal applied. The spurious turn-on may even occur though the applied forward voltage amplitude is considerably below the rated peak anode voltage V_{DRM} of the SCR. Such an unscheduled turn-on may result in excessive surge current which can cause SCR's to fail. For dv/dt protection, consequently, normal suppression components, such as Thyrector diodes, metal oxide varistors, controlled avalanche diodes, or spark gaps will not be sufficient. A properly design resistor-capacitor network will not only limit the dv/dt to a desired level, it can also aid in reducing the repetitive peak transient voltage to a more practical value.

16.3.2 Suppression Network

One form of suppression network is commonly called a snubber circuit. The snubber circuit basically consists of a series-connected resistor and capacitor placed in shunt with an SCR. The snubber circuit in conjunction with the circuit effective series inductance controls the maximum rate of change of voltage and the peak voltage across the device when a stepped forward voltage is applied to it. Referring to Figure 16.15 when an input is suddenly applied, it is transiently divided between the inductance, L, which functions as a series suppressor and the R-C snubber circuit.

16.3.2.1 Snubber Calculation for D.C. Circuit[6]

When a circuit designer works with power SCR's in designing a snubber, he is likely to use a cut-and-try method. Such a technique can be tedious and time consuming. By using designed nomograph, Figures 16.16 through 16.18, the various trial steps can be eliminated. The construction of these nomographs is based on the analysis of a basic R-C snubber circuit in response to a step input signal. The analysis shows that the effect of damping in a L-R-C circuit can be described in terms of a single parameter, designated ϵ, which is the ratio of the resistance to the surge impedance of the circuit. The effective total circuit inductance is normalized in terms of ϵ, R, and C of the circuit. The relationship is shown by the following expression:

$$\epsilon = \frac{2}{R}\sqrt{C/L} \qquad (16.3)$$

It is desirable to have a high value of L. A higher value of L will allow higher value of R and a lower value of C to retain the desired damping effect, controlled dv/dt and peak overshoot voltage (these relationships are clearly expressed by Figures 16.16 and 16.17. Yet a higher value of R and a lower value of C not only minimizes the power dissipation in the snubber circuit, but also limits the initial current discharging into the SCR during its turn-on interval. Based on experience and test, it is desirable to select a circuit damping ratio, ϵ, in the range of .5 to 1.0, both to limit the peak overshoot voltage applied to the SCR and to minimize the "ringing" of the L-R-C circuit within the maximum required dv/dt value.

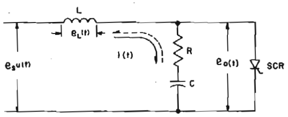


FIGURE 16.15 EQUIVALENT CIRCUIT OF SNUBBER

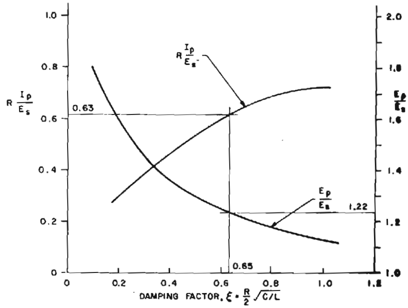


FIGURE 16.16 NORMALIZED PEAK SNUBBER CURRENT AND OVERSHOOT VOLTAGE Vs CIRCUIT DAMPING RATIO

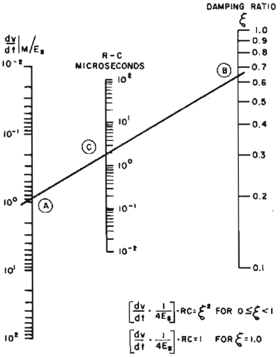


FIGURE 16.17 NORMALIZED SNUBBER CIRCUIT TIME CONSTANT SELECTION CHART

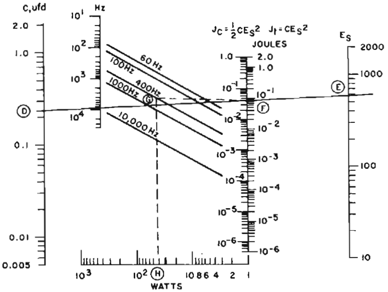


FIGURE 16.18 SNUBBER LOSS NOMOGRAPH

Worked Example

Assume:
1. Peak switching voltage, $E_S = 600$ volts.
2. Operating frequency, $f_o = 400$ Hz.
3. $dv/dt|_m$ to be limited $\leqq 500$ V/μsec.
4. Chosen $\epsilon = .65$ for a controlled voltage overshoot of approximately 22% (Figure 16.16).

Solution:
1. To determine the required R-C time constant of the snubber, go to Figure 16.17, connecting two points specified by:

$$\text{Point A: } \frac{dv/dt|_m}{E_S} = \frac{500}{600} \cong .83$$

Point B: $\epsilon = .65$

R-C is located (Point C) to be 2.0 μsec.

2. To determine the value of R, go to Figure 16.16 and locate:

$$I_P \frac{R}{E_S} = .63$$

Assume the $I_{P(Snubber)}$ is limited to 50 amperes, R is found to be: $R = (.63)\left(\frac{600}{50}\right) = 7.6\ \Omega$. Use 8 Ω.

3. From Steps 1 and 2, C is determined

$$C = \frac{2.0}{8.0} = .25\ \mu Fd.$$

4. Based on C, Hz and E_S, go to Figure 16.16 and find the peak snubber power dissipation. By connecting two points specified by:

   Point D: $C = .25\ \mu Fd$
   Point E: $E_S = 600$ volts

   Point F ($J_C = .045$ Joules) is located.
   Project Point F horizontally to "Hz" scale on Point G, then vertically project G to watts scale on Point H. The maximum power dissipation is found to be 40 watts.

It has been stated that SCR's can be affected by voltage transients from the AC power supply. Voltage transients from the power supply are primarily caused by the effects of switching inductive circuits such as are always present in the supply transformer. Consider the single-phase bridge circuit in Figure 16.19. Transients may result from switching off the primary of the transformer. If a non-inductive load is always connected and the load is able to absorb sufficient energy to attenuate the induced voltage, no transient suppression measures are required. However, if appreciable inductance is present in the load and no-load operation is possible, transient suppression is a must. A properly chosen R-C snubber connected across the secondary of the transform will dampen the transient voltage to a desired level. The size of resistor-capacitor required for a particular suppression job is a function of many circuit parameters such as the type of load, load current level, the transformer characteristics and the frequency of interruption and switching.

16.3.2.2 Snubber Calculation for AC Circuit[6,7,8]

The following equation has proved useful in selecting the required capacitance sufficiently to limit the voltage transients within SCR voltage ratings:

$$C = 10 \frac{VA}{V_S^2} \frac{60}{f} \text{ microfarads} \qquad (16.4)$$

where C = the minimum required capacitance
VA = the transformer volt-ampere rating
V_S = the transformer secondary RMS voltage
f = frequency other than 60 Hz

The required resistance to ensure adequate damping can be calculated from the following relationship:

$$R = 2\epsilon\sqrt{L/C}$$

where R = the required resistance to damp the transient voltage to a desired level

ϵ = damping factor

L = effective circuit inductance

C = minimum required capacitance

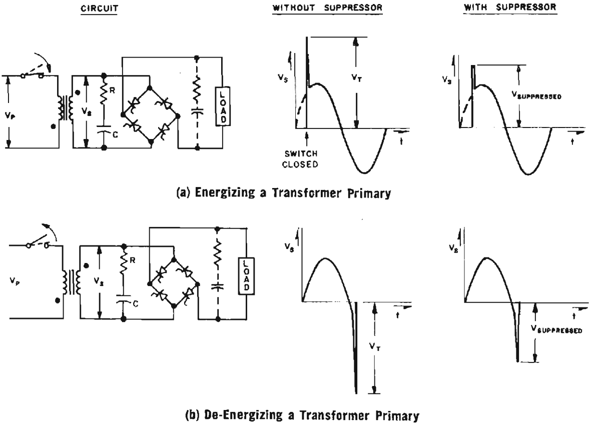


FIGURE 16.19 VOLTAGE TRANSIENTS DUE TO SWITCHING OF TRANSFORMER PRIMARY

Work Example – Refer to Figure 16.19

Assume:
1. Supply transformer is rated 5 KVA with secondary voltage of 120 V_{RMS}
2. Switching frequency, $f_o = 400$ Hz
3. Circuit inductance, L = 100 μhy at 400 Hz
4. Peak transient voltage is to be limited at 200 volts

Solution:
1. To determine required snubber capacitance, using formula

$$C = 10 \frac{VA}{V_S} \frac{60}{f}$$

$$= 10 \frac{5000}{(120)^2} \frac{60}{400}$$

$$= .52\ \mu fd - \text{use } .5\ \mu fd$$

2. Calculate peak transient voltage vs peak switching voltage ratio

$$\frac{V_P}{V_{S_P}} = \frac{200}{120\sqrt{2}} = 1.18$$

Go to Figure 16.22 and locate $\epsilon = .75$

3. To determine required damping resistance, using following relationship

$$R = 2\,(\epsilon)\,\sqrt{L/C}$$

$$= 2\,(.75)\,\sqrt{\frac{100}{.5}}$$

$$= 21.2\,\Omega - \text{use } 20\,\Omega$$

4. To determine the maximum power dissipation, go to Figure 16.16 using same procedure as outlined in Step 4 of the previous sample with following specified parameters

$$C = .5\ \mu fd$$

$$E_S = \sqrt{2}\,(120) = 170 \text{ volts}$$

$$f_o = 400 \text{ Hz}$$

The maximum power dissipation in the resistor is found to be 10 watts.

To suppress the voltage transients generated from the power supply of a single-phase system, the snubber should be connected across the secondary of the transformer.

For a three phase system, the snubber should be connected either from line to line or line to neutral across the secondary of the transformer depending upon the secondary connections whether it may be of delta or star configurations.

16.4 MISCELLANEOUS METHODS

Several other transient suppression means may be used to good advantage depending on the particular circumstances of the application. Spark gaps may be used in high voltage circuits provided the precautions outlined in Section 16.2.4 are maintained.[6] Silicon diodes can be used as discharge paths for the energy stored in inductive circuit elements such as generator fields and magnetic brakes.

Electronic crowbar circuits of the type shown in Figure 8.20 use the SCR to provide microsecond protection against overvoltage conditions for entire circuits. Properly selected and applied triac and diac components can also be used to shunt transient energy away from sensitive electronic circuitry when voltage tries to rise above the breakover switching level of the particular protective semiconductor component.

Figure 16.20 illustrates a technique by using SCR's to control dynamic braking to a DC motor load, thus preventing the occurrence of overvoltage from damaging the motor and subsequently limiting the DC voltage imposed on SCR's in the power circuit. Under normal operation neither SCR_1 or SCR_2 conduct and no energy will be dissipated in R_1 and R_2. When the motor CEMF voltage rises above a level predetermined by the selection of avalanche diodes CR_1 and CR_2, SCR_1 and SCR_2 are triggered, connecting R_1 and R_2 across the load. As soon as the motor CEMF voltage drops below the controlled supplied voltage, SCR_1 and SCR_2 will be commutated off by the AC line

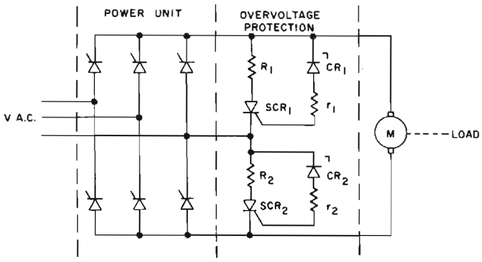


FIGURE 16.20 REGENERATIVE VOLTAGE PROTECTION

and return to their non-conducting state. The circuit performs a dual function of limiting overvoltage and overcurrent in a continuous mode of action. Such a function provides an attractive feature in motor control applications where non-interruptive performance is demanded.

In general, if the protective network is properly designed, the system reliability can be greatly improved. In order to design the protective network properly, a designer must know the source and nature of possible transients in his circuit and the characteristics of the control elements to be protected.

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11. GE-MOV™ Varistors, Voltage Transient Suppressors by F. B. Golden and R. W. Fox, Application Note 200.60,* General Electric Company, Auburn, N. Y.

*See Chapter 23 for availability and ordering information.

17 RADIO FREQUENCY INTERFERENCE AND INTERACTION OF THYRISTORS

17.1 INTRODUCTION

Each time a thyristor is triggered in a resistive circuit, the load current goes from zero to the load limited current value in less than a few microseconds. A frequency analysis of such a step function of current would show an infinite spectrum of energy, with an amplitude inversely proportional to frequency. With full wave phase control in a 60 Hz circuit, there is a pulse of this noise 120 times a second. In applications where phase control is used in the home, such as lamp dimming, this can be extremely annoying, for while the frequencies generated would not generally bother television or FM radio reception, the broadcast band of AM radio would suffer severe interference. In an industrial environment, where several control circuits may be used, these noise pulses cause interaction between one thyristor control and another. The power system can act as a large transmission line and antenna system, propagating these radio frequency disturbances for a considerable distance.

With the newer inverter types of SCR's and their growing use, an additional problem is created since the basic inverter frequencies may be in excess of 10 kHz. The harmonics generated in these systems can cause interference sources which are orders of magnitudes larger than those of phase control systems and also the fundamental frequency over 10 kHz may put the equipment under specific provisions of the FCC rules.

At this time the Federal Communications Commission rules (Part 15) require that incidental radiation devices "... shall not cause any harmful interference in use." It is under this section of the law which most thyristor systems fall. The Commission has stated a willingness to allow industry to police itself. To this end several of the national associations have proposed standards for their members. It is strongly urged that anyone desiring to sell or lease, offer for sale or lease, import, ship or distribute such equipment, ascertain whether or not he is in compliance with the applicable standards. Included at the end of this chapter is a list of some of the currently available standards for both the United States and European countries.

17.2 THE NATURE OF RADIO FREQUENCY INTERFERENCE (RFI)

There are two basic forms of RFI to consider. The first (and most commonly measured) is conducted RFI. In this form, the high frequency energy generated by the thyristor switching transients propagates through the power lines, which act as transmission lines. By using standard methods and equipment, quantitative measurements may be

fairly easily obtained on conducted RFI. These standards are listed in Section 17.7.

The other main form is that of radiated RFI. This is the RF energy which is radiated directly from the equipment. This is a difficult type of RFI to measure since it can never be separated from the problems of location, wiring layout, ground effects, etc.

In most cases, the radiated RFI from a properly designed piece of equipment is insignificant compared to the re-radiation of conducted RFI from the large antenna system we call power lines.

The following military specifications set quantitative interference levels and give test procedures to which an equipment must be qualified if it is to conform to the specification:

MIL-STD-461A (Requirements for Equipment)
MIL-STD-462 (Measurement Methods)
MIL-STD-463 (Definitions)

17.2.1 Filter Design

Since thyristors generate essentially a step function of current when they turn on into a resistive load, the conducted RFI has the frequency distribution of a step function, that is, a continuous spectrum of noise with an amplitude which decreases with frequency at a rate of 20 db per decade. This indicates that even unfiltered thyristor circuits would show very little tendency to interfere with such VHF services as television or FM broadcasting. The AM broadcast band however lies between 550 and 1600 kHz, and would receive severe interference, if the thyristor circuits were not properly filtered.

The simplest type of filter is merely an inductor in series with the load resistance to slow the rate of rise of current. This would give a filter effectiveness of about 20 db/decade. The typical example shown in Figure 17.1 shows that the bottom of the broadcast band requires from 40 to 50 db of suppression to reach a level of interference which could be considered adequate (about 500 quasi-peak μvolts).* To achieve this, the breakpoint frequency, $f_o = R/(2\pi L)$ (where R is the

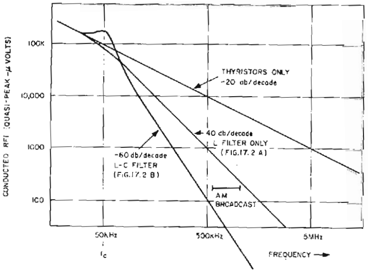
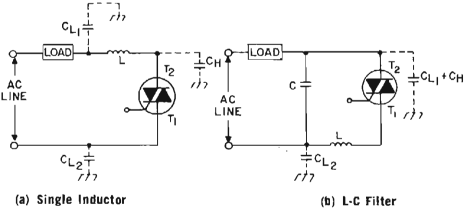


FIGURE 17.1 THEORETICAL THYRISTOR CIRCUIT NOISE SPECTRUM WITH AND WITHOUT FILTERING

*"Quasi-peak Volts" is a unit of measure which is determined by the standard test methods. It is in effect a measure of the "Nuisance Value" conducted RFI.

load resistance), would have to be at 5 kHz, or below. This would be a rather large and costly inductor.



C_{L1}; C_{L2} = Line Capacitance to Ground
C_H = Heatsink Capacitance to Ground

FIGURE 17.2 SIMPLE FILTERS

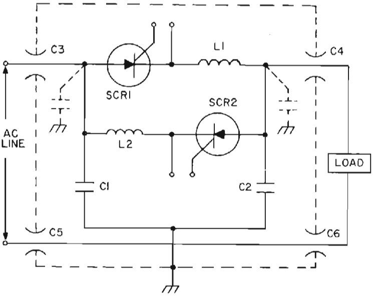


FIGURE 17.3 RFI FILTERING AND SHIELDING FOR BACK-TO-BACK SCR'S

The addition of a shunt capacitance to the filter as shown in Figure 17.2(b) gives a far superior characteristic as can be seen in Figure 17.1. Now the required 40 db of suppression can be obtained in a single decade. As a rule of thumb, the proper values for L and C may be found by making the L-R and L-C breakpoint frequencies equal.

$$f_o = \frac{R_L}{2\pi L} = \frac{1}{2\pi\sqrt{LC}}$$

or in other words

$$2\pi f_o L = \frac{1}{2\pi f_o C} = R_L$$

This allows a value of L one tenth that needed for a purely inductive filter.

In a practical thyristor circuit, one side of the device is usually connected to a heatsink, which because of its size or mounting, is capacitively connected to ground. In the case of the triac shown in Figure 17.2 main terminal T_2 is the heatsink side. If the choke L were in series with T_2, as in Figure 17.2(a), the heatsink capacitance in conjunction with stray line capacitance would shunt the choke, thereby reducing its effectiveness as a filter. The proper connection of L in series with T_1 actually puts the stray capacitances in parallel with C, thus enhancing filter effectiveness.

The optimum connection for back-to-back SCR's is shown in Figure 17.3. If a shielded enclosure is not present, C_1 and C_2 should be a single capacitor connected between the anodes of SCR_1 and SCR_2.

It is important to note that any pulse transformers or triggering circuits should put the smallest possible capacitive loading on the cathode of the SCR's, since this capacitance will appear across the chokes.

If you look at the circuits of Figure 17.2, you can see that the L-C's and triac or SCR pair form a resonant discharge circuit, which depends on the load impedance for damping. For circuit Q's greater than about 2.5 the current through the thyristor will reverse, as shown in Figure 17.4, and a specific triac might turn off if it is a relatively fast device.

This condition is aggravated for light loads, in this case about 100 watts or less, or somewhat inductive loads, which contribute little damping to the circuit. The simple L-C circuit does behave properly however with heavier resistive loads, as shown in Figure 17.4(b). To obtain proper operation under light load conditions, for instance a lamp dimmer with a 60 watt lamp, it is necessary to build the damping required into the filter. This can be done by adding another resistor and capacitor as shown in the circuit of Figure 17.5. The component values are chosen to give about the same filtering effect as the L-C filter of Figure 17.2(b).

(a) 60 Watt Load
High Q > 2.5

(b) 150 Watt Load
Low Q < 2.5

VERT. – 2 AMP/CM
HORIZ. – 5 μSEC/CM

L = 100 μH
C = 0.1 μF
Supply Voltage = 120 V

FIGURE 17.4 TRIAC CURRENT FOR THE CIRCUIT OF FIGURE 17.2(B) IMMEDIATELY AFTER THYRISTOR TURN-ON

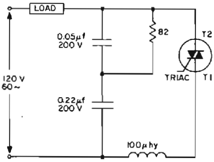


FIGURE 17.5 TYPICAL DAMPED R-F FILTER

17.2.2 Components for R-F Filters

The above discussion centers on the simplest forms of filters. It is reasonable to assume that more complex filters can do more adequately if they are required. Figure 17.6 shows the conducted RFI measurements for triac fan motor speed control circuit. The test measurement was made in accordance with the American National Standards Association's Standard Method C63.4.** Also included on the graph is the NEMA Standard per WD.2-1970** which sets a maximum allowable limit for conducted interference.

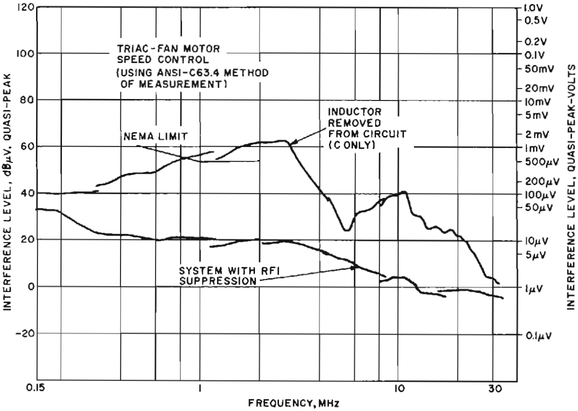


FIGURE 17.6 TYPICAL CONDUCTED RFI WITH AND WITHOUT SUPPRESSION NETWORK

**Refer to end of chapter for ordering information.

When choosing components for R-F filters it is extremely important that the components chosen act in the manner in which they should. At high frequencies capacitors tend to act like inductors and inductors like capacitors. When this occurs all filtering is lost.

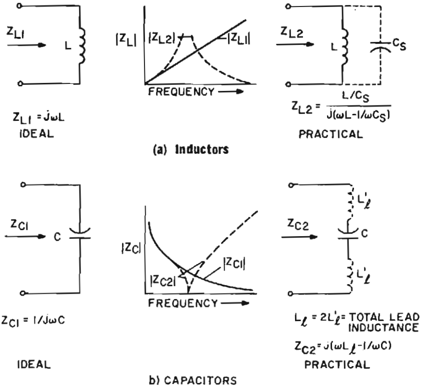


FIGURE 17.7 FILTER ELEMENTS—IDEAL, PRACTICAL AND THEIR FREQUENCY RESPONSE

Figure 17.8(a) shows how 0.05 μF capacitor's characteristics change with frequency. Figure 17.8(b) shows the characteristics of a 157 μH inductor.

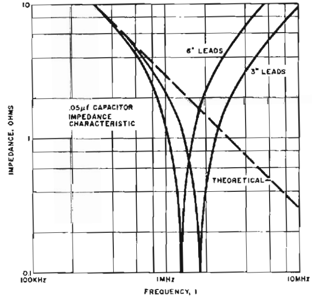


FIGURE 17.8(A) TYPICAL IMPEDANCE CHARACTERISTICS OF .05μF CAPACITOR

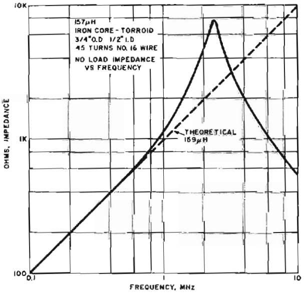


FIGURE 17.8(B) TYPICAL IMPEDANCE CHARACTERISTICS OF 157μH INDUCTOR

Besides an inductor maintaining its inductance at high frequencies, it should also be designed to prevent saturation from occurring too soon. When the core of an inductor becomes saturated, the inductor

acts like it has an air core and its reactance drops thus losing its ability to lower the di/dt of the circuit. Most non air core inductors can be rated for a minimum volt-second withstand capability to guarantee that saturation does not occur too soon. The volt-second capability of the reactor should be large enough to provide a load current rise time of not less than approximately 50 μsec.

17.2.3 Fast Recovery Rectifiers

In circuits which use rectifier diodes, RF noise may be generated by the reverse recovery performance of the diodes. Due to the minority carrier storage effect, the diode does not immediately block voltage when the circuit causes current reversal. When, after a few μseconds, the charge which had been stored in the diode is "swept-out," the diode can again block the flow of reverse current. At this point, the current can stop quite suddenly, giving a "snap-off" effect. The energy stored in the circuit inductance at this point can be shown to be equal to

$$W_T = Q_R E_C$$

where Q_R is the total charge swept-out
E_C is the circuit commutation voltage.

Figure 17.9 shows the waveform of the recovery current of a conventional as well as a fast recovery diode.

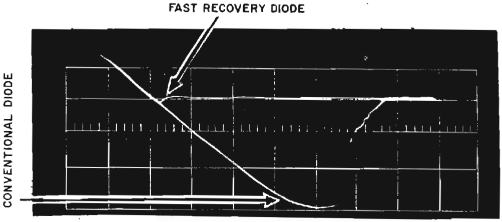


FIGURE 17.9 COMPARISON OF REVERSE RECOVERY PERFORMANCE OF TYPICAL RECTIFIER DIODES. VERTICAL = 8 AMPS. PER CM. HORIZONTAL = .5 μSEC. PER CM.

On each "snap-off" commutation of a diode there is a step of current of height I_{RP}. The RF components of this current step are given by

$$I(\omega) = \frac{I_{RP}}{\pi \omega}$$

where ω is an RF noise component frequency.

This result is found by Fourier Integral Analysis of a step function. But I_{RP}^2 is proportional to W_T or

$$I_{RP} \propto \sqrt{W_T}$$

Thus, the RF interference generation at a given frequency is

$$I(\omega) \propto \frac{\sqrt{W_T}}{\pi\ \omega}$$

Since the value of W_T runs better than 100 times less for a fast recovery rectifier than for a conventional rectifier, there is a considerable reduction in RFI problems when using fast recovery devices.

17.2.4 Reduction of Radiated RFI

The minimization of radiated RFI is as much a matter of good construction practice as anything else. Referring to Figure 17.2(b), the current through the loop formed by C, L, and the thyristor contains high frequency components of a much greater magnitude than the line current. (The inner loop has only a single L filter). The wiring of this loop can act as an antenna for direct radiation. Since the radiation efficiency of an antenna of this type is proportional to the area enclosed by the loop, good practice requires that this current loop be constructed with a minimum of enclosed area. It should be pointed out that trigger circuits can also be offenders in direct radiation, and the same techniques apply.

Figure 17.3 illustrates proper shielding techniques. The SCR's with their filter circuitry are enclosed inside their own shielded compartment, with leads from the power line and to the load passing through feedthrough capacitors C_3-C_6.* Either the pulse transformer or the gate pulse generation circuitry should be located within the compartment, since locating them remotely forces one to hang leads on the cathodes of the SCR's, thereby providing excellent antennas.

*For devices where "leakage" current criteria must be met the magnitude of these capacitors may be severely limited.

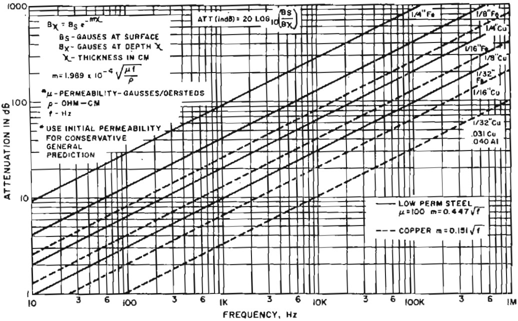


FIGURE 17.10 PENETRATION LOSS (ATTENUATION) OF DIFFERENT SHIELDING MATERIALS

The design of the shielded compartment can be equally as important. Figure 17.10 shows the effectiveness of different materials and thicknesses in reducing the radiated magnetic field.

17.2.5 Zero Voltage Switching

As we have seen, the RF noise contribution of thyristors is primarily due to a sudden step in current as the thyristor switches. In some applications, particularly in electric heating, satisfactory control may be obtained by turning the thyristors on at line voltage zeros, giving only complete half cycles of current to the load. By eliminating the sudden steps of voltage, the RF noise contribution is brought to an absolute minimum. This eliminates the need for R-F filter components, which, for a large heating load, can become quite large and costly. For details on this type of circuit, see Chapter 11.

17.3 INTERACTION

In some instances the thyristor system acts as a "receiver" of voltage transients generated elsewhere in the circuit. These transients act either (or both) on the thyristor trigger circuit or directly on the anode of the thyristor in the main power circuit. Interaction will cause the thyristor system acted upon to completely or partially follow, or track, another thyristor system. Also, various types of partial turn on, depending on the nature of the trigger circuit, have been known to arise. Elimination of interaction phenomena must take total system layout into consideration. Section 17.6 gives some general design practices which should be followed to minimize possible sources of interaction. Beyond good design practice in the system as well as in triggering circuits very specific steps for decoupling can be taken as outlined for UJT circuits in Section 17.4. In general it should be noted that the suppression of RFI emanations also serves to minimize susceptibility.

17.3.1 Interaction Acting on Anode Circuit

When a thyristor circuit is acted upon with its gate circuit disconnected (open gate or terminated per specification bulletin) the nature of the interaction is usually attributable to a rate of rise of forward voltage (dv/dt) phenomenon. When energizing the circuit, such as by a contactor or circuit breaker, applicable dv/dt specifications for the device must be met. This subject is discussed in detail in Chapters 3 and 5. Once the circuit is energized the thyristor will sometimes respond to high frequencies superposed on the anode supply voltage. For example, a 1-megacycle oscillation having a peak amplitude of 10 volts has an initial rate of rise in the order of 60 volts per microsecond. Applicable specifications for the thyristor must meet this condition or steps should be taken to attenuate the rate of rise of voltage.

Due to the nature of anode circuit interaction a thyrisor will rarely track another circuit over the full control range of phase control. Usually, it will tend to lock in over a very limited range near the top of the applied anode voltage half cycle where the dv/dt is greatest. The best means of suppressing this type of interaction is to select a device with increased dv/dt withstand capability, to increase dv/dt withstand capability by means of negative gate bias, or, conversely, to

reduce the rate of rise of positive anode voltage by suitable circuit means. The effect of negative gate bias on SCR dv/dt withstand capability and dv/dt suppression circuitry is discussed in Section 3.11. Often a combination of these steps yields the desired results. In addition, of course, good circuit layout and system practices should be observed as outlined in Section 17.6.

17.3.2 Interaction Acting on the Trigger Circuit

There are basically two cases to distinguish here:

1. The trigger circuit is acted upon from the supply line directly;
2. The trigger circuit is acted upon from the thyristor gate circuit.

Both of these mechanisms may cause the trigger circuit to fire prematurely, giving rise either to spurious triggering or complete or partial tracking of the thyristors in the circuit. The response of the trigger circuit to incoming transients will determine the degree of interaction, if any. There are no general rules for every type of trigger circuit. However, in the design of a trigger circuit it is well to take the possibility of interaction into account. The designer will be in the best position to assess the transient susceptibility and stability of his circuit.

When using the unijunction transistor trigger circuit there are a few relatively simple steps that can be taken to decouple these circuits against both supply voltage and gate circuit transients. These methods are outlined in the following two sections.

17.4 DECOUPLING THE UJT TRIGGER CIRCUIT AGAINST SUPPLY TRANSIENTS

Depending on the nature of the particular circuit conditions, either one or a combination of the following will give effective decoupling against line voltage transients acting on the unijunction transistor trigger circuit:

1. Use of control (isolation) transformer with a properly grounded shield between primary and secondary or an RF filter across its secondary, if necessary;
2. Use of "boot strap" capacitor between base two and the emitter of the unijunction transistor;
3. Use of a Thyrector diode connected across the supply to the unijunction circuit.

The value of the "boot strap" capacitor C_1 should be chosen so that the voltage divider ratio of C_1 and C_2 in Figure 17.11(A) is approximately equal to the intrinsic standoff ratio of the UJT, or:

$$\frac{C_1}{C_1 + C_2} = \eta$$

If this condition is met, positive or negative transients on the unijunction supply voltage will not trigger the UJT.

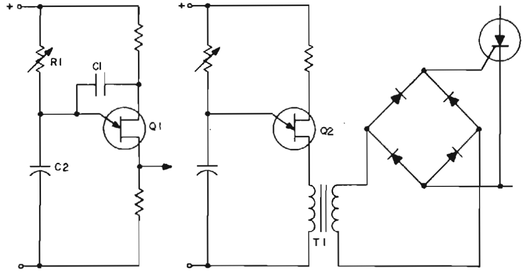


FIGURE 17.11 CIRCUITS FOR ELIMINATION OF ERRATIC FIRING FROM VOLTAGE TRANSIENTS IN UJT CIRCUITS

17.5 DECOUPLING UJT CIRCUITS AGAINST SCR GATE TRANSIENTS

Negative voltage transients appearing between the gate and cathode of the SCR's when transmitted to the UJT can cause erratic triggering. When transformer coupling is used, these transients can be eliminated by using a diode bridge in the gate circuit of the SCR as shown in Figure 17.11(B). Negative transients often arise in SCR gate circuits in forced-commutated circuits (see Chapter 5) and under certain conditions in AC phase control circuits.

17.6 GOOD DESIGN PRACTICES TO MINIMIZE SOURCES OF SCR INTERACTION

Radio frequency interference and interaction are both total system phenomena and no one step is necessarily the most effective in attaining the desired level of suppression. A combination of good system design practices, good circuit layout, good equipment layout, and, if necessary, a small amount of circuit filtering, as was outlined above, will suppress RFI to acceptable levels and eliminate various types of interaction phenomena.

When the following system considerations are met it is often unnecessary to take additional specific steps to filter trigger or anode circuits (Section 17.2) or use negative gate bias and dv/dt suppression circuitry (Section 3.11):

1. Operate parallel and potentially interacting thyristor circuits from a stiff (low reactance) supply line;
2. If supply line is soft (high reactance), consider using separate transformers to feed the parallel branch circuits; each transformer should be rated no more than the required rating of the branch circuit load;
3. Avoid purely resistive loads operating from stiff lines—they give highest rates of current rise on switching;
4. Keep load moderately inductive—limiting rate of current rise on switching is in the direction of attenuating RFI and minimizing the possibility of interaction;
5. Keep both leads of a power circuit wiring run together—avoid loops that encircle sensitive control circuitry;
6. Arrange magnetic components so as to avoid interacting stray fields.
7. Use twisted pair or shield wires for control power wiring and gate driver wiring.

17.7 E.M.I. STANDARDS AND RESTRICTIONS

1. American National Standards Institute, Inc., 1430 Broadway, New York, N. Y. 10018.
   C63.4-1963 "Radio-Noise Voltage and Radio-Noise Field Strength"
   C63.2-1963 "Radio-Noise and Field Strength Meters 0.015 to 30 Megacycles/Sec."
2. National Electrical Manufacturers Association, 155 East 44th Street, New York, N. Y. 10017
   WD2-1970 "Semiconductor Dimmers for Incandescent Lamps"
3. Department of Defense, Washington, D. C. 20360
   MIL-STD-461A "Electromagnetic Interference Characteristics Requirements for Equipment"
   MIL-STD-462 "Electromagnetic Interference Characteristics, Measurement of"
   MIL-STD-463 "Definitions and System of Units, Electromagnetic Interference Technology"
4. Federal Communications Commission
   Title 47 CFT, Chapter I, Part 2, Sub-part I, Paragraphs 2.801 to 2.813.
   Printed in *Federal Register*, Vol. 35, No. 100, May 22, 1970, pages 7898-7899.
   Vol. II of the FCC Rules and Regulations includes the following up-dated parts of interest:
   - Part 2, Frequency Allocations and Radio Treaty Matters: General Rules & Regulations
   - Part 15, Radio Frequency Devices
   - Part 18, Industrial, Scientific and Medical Equipment

   (Can be ordered from the Superintendent of Documents, Government Printing Office, Washington, D.C. 20402. Substitute pages, incorporating amendments, will be mailed to all purchasers of this volume.)

5. Comite International Special des Perturbations Radioelectriques, Verband Deutscher Elektrotechniker—Verlag, Berlin 12, Bismarkstrabe 33, VDE-0872 through VDE-0877.

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1. "Application of Fast Recovery Rectifiers," J. H. Galloway, General Electric Company, Auburn, N. Y. Application Note 200.38.*
2. "Frequency Analysis Modulation and Noise," book, Stanford Goldman, McGraw Hill Inc., New York, 1948.
3. "Radio Frequency Interference," a series of editorial features appearing in "Electronic Industries," 1960-1961.
4. "Electrical System Transients and Sensitive Circuit Control," T. B. Owen, AIEE Applications and Industry, November 1960.
5. "One-Point Ground System With RF Shielding and Filtering," R. A. Varone, AIEE Conference Paper 60-1067, Fall General Meeting, August 1960.
6. "How to Locate and Eliminate Radio and TV Interference," book, R. D. Rowe, John F. Rider, Inc., New York, 1954.
7. "Transmitter-Receiver Pairs in EMI Analysis," J. A. Vogelman, *Electro-Technology*, November 1964.
8. "Electromagnetic-Interference Control," Norbert J. Sladek, *Electro-Technology*, November 1966.
9. "Signal Conditioning," Gould Brush, Application Booklet No. 101, Gould Inc., Cleveland, Ohio.
10. "Interference Control Techniques," Sprague Electric Company Staff, Technical Paper No. TP62-1, Sprague Electric Company, North Adams, Mass.
11. "Radio Frequency Interference," Onan Staff, Onan Division of Studebaker Corp., Minneapolis, Minn.
12. "Interaction Between SCR Drives," Ben Stahl, IEEE Transactions on Industry and General Applications, Vol. IGA-4, No. 6, November/December 1968.

*Refer to Chapter 23 for availability and ordering information.

NOTES

18 MOUNTING & COOLING THE POWER SEMICONDUCTOR

Successful application of SCR's depends to a great extent on adequate cooling of these devices. If junction temperature of an SCR rises high enough, permanent damage may occur in its characteristics and the device may fail by thermal runaway and melting. Circuits may fail before thermal runaway or melting in the SCR occurs since insufficient cooling can reduce the forward breakover voltage, increase SCR turn-off time, moving these and other SCR characteristics outside specifications sufficiently to induce circuit malfunction. For these reasons, all SCR's and rectifier diodes are designed with some type of heat transfer mechanism to dissipate internal heat losses.

Mounting surfaces are generally an integral part of an SCR's heat transfer path. Proper mounting is always needed for successful SCR cooling. Thus cooling and mounting the SCR are part of the same problem and must be treated together.

18.1 LEAD-MOUNTED SCR's

For small lead-mounted SCR's like the C3, C5, C6, C7, C8 and C103 series, and some configurations of the C106, C107 and C122 (see Figure 18.1), cooling is maintained by radiation and convection from the surface of the case and by thermal conduction down the leads.

Several good common sense practices for minimizing the SCR temperature should be used whenever possible. Minimum lead length to the terminal board, socket, or printed board permits the mounting points to assist in the cooling of the SCR most efficiently. Other heat dissipating elements such as power resistors should not be connected directly to the SCR leads where avoidable. Also, high temperature devices like lamps, power transformers, and resistors should be shielded from radiating their heat directly on the SCR case. To increase heat dissipation of the standard TO-5 case, clip-on transistor radiators are available from a number of commercial vendors.

Several of the General Electric lead mounted SCR's in the TO-5 case are also available on a power transistor type of base for attachment by clamping screw or the like to a heatsink or chassis. Directions for mounting these devices are given on the specification sheet for that type of SCR.

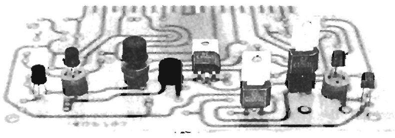


FIGURE 18.1 LEAD MOUNTED SCR's

18.2 MOUNTING SCR's TO HEAT EXCHANGERS

The importance of proper SCR mounting can be seen from Figure 18.2.The electrical circuit analog for an SCR's thermal path shows the mounting interface, $R_{\theta CS}$, to be a series limiting factor to the flow of thermal power (heat) from the junction to the ambient. Attention is not focused on $R_{\theta JC}$ in this chapter since it is beyond the control of the equipment designer. Mention is made of it regarding selection of the proper value from the SCR specification sheet where an SCR has a multivalued $R_{\theta JC}$. Somewhat like a chain, a series circuit is limited by its weakest link, i.e., highest resistance component. In order to prevent $R_{\theta CS}$ from becoming the weak link, general instructions and guide lines for the proper mounting of the various types of SCR packages will be discussed first. Following the general guide lines specific sections deal with considerations peculiar to each package type.

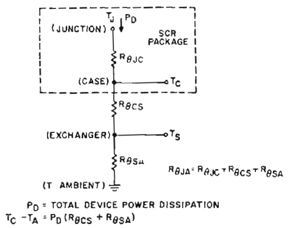
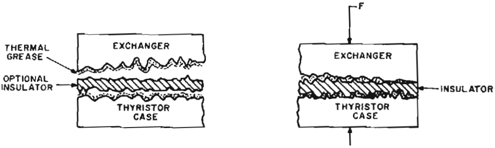


FIGURE 18.2 EQUIVALENT THERMAL RESISTANCE NETWORK ANALOG FOR A POWER SEMICONDUCTOR COOLING PATH

18.2.1 Case to Heat Exchanger Interface Considerations

The interface formed between the SCR package case and the heat exchanger can take many forms. The corresponding values of case to heat exchanger thermal resistance will vary greatly depending upon the given interface conditions.

Figure 18.3 illustrates the effect of metal surface conditions on interface performance. The exchanger surface distortion as well as smoothness of surface finish is exaggerated to show its effects.



(a) Before Mounting Force **(b) After Mounting Force Applied**

FIGURE 18.3 EFFECT OF INTERFACE SURFACE AND FLATNESS CONDITIONS ON THERMAL CONDUCTIVITY

After force is applied to the joint the surfaces are forced together at the points of contact. The net contact area is then a function of contact metal ductility, surface finish, flatness and net force applied. In addition a thermal grease is shown which serves to fill in the voids left by the valleys due to poor surface finish. Note from Figure 18.3(b) the large void in the top contact area due to the poor flatness of the sink as compared to the bottom interface where the insulator and thyristor case are shown to be flat. The insulator's thickness and thermal conductivity further adds to the interface resistance.

18.2.1.1 Exchanger Surface Preparation

The surface under the semiconductor contact surface should be flat to within 0.001 inch per inch and have a surface finish of 63 micro-inches or less for all stud and tab mounted devices. For press paks exchanger surface should be flat to within 0.0005 inch per inch and have a surface finish of 32 micro-inches or less.

Before final assembly, the semiconductor case surface should be checked for removal of all burrs or peened-over corners that may have occurred during shipping and subsequent handling and that would otherwise cause reduced heat transfer across the surfaces.

Most heat exchanger surfaces have some treatment to aid radiation heat transfer and give corrosion protection. Copper fins are plated, painted, or ebnoled. Aluminum fins are generally painted or anodized. The heat exchanger surface under the semiconductor contact surface must be free of paint, anodization, or ebnol to give minimum contact thermal resistance. While plating in this area does not have to be removed, excessive oxides should be removed whenever the exchanger surface has been exposed to the ambient air for more than sixty minutes after machining.

Oxide removal prior to assembly may be accomplished by polishing the mounting surface with No. 000 fine steel wool and silicone oil. Following the polishing the surface should be wiped clean with a lint free paper towel. As a final step a thin layer of thermal grease or oil should be applied.

Applications where a moist or corrosive atmosphere are expected, galvanic action between aluminum and the copper SCR case may lead to gradual deterioration of the joint, and an increase in thermal resistance. A good nickel (ALSTAN 70 Process), silver or cadmium plate over the copper case as provided on General Electric SCR's, combined with the use of a corrosion inhibitor, such as Burndy-Penetrox A; Alcoa No. 2, Dow Corning DC 19 or Penn-Union Cual-Aid, minimizes corrosion at this joint.

18.2.1.2 Interface Thermal Grease

Thermal greases serve two functions. They serve to resist corrosion and secondly they enhance the interface substantially by filling in the voids with a more thermally conductive material than air as shown in Figure 18.3. Note the decreased thermal resistance of interfaces having grease over those without grease shown in Table 18.1. Thermally conductive greases and oils come with and without metal fillers. These

suspended metal fillers generally serve to enhance the joint's thermal properties over the non-filled greases but not to a substantial value. They have the disadvantage of indenting the mounting surface slightly requiring a careful refinishing of the surfaces with 400 or 600 grit sandpaper should disassembly or reassembly become necessary. Table 18.2 provides an application guide to the many oils and greases available to the user. The chief advantage of the oil over the grease lies in the better control of film thickness possible with oil. The user can specify one or two drops from an eye dropper. Excessive grease or oil can be detrimental to interface thermal resistance.

Stud Size	Hex Size Across Flats or Flat Base Dia.	Case-Exchanger Thermal Resistance ← $R_{\theta CS}$ – °C/Watt → With Thermal Grease Min.	Nom.	Max.	Dry Min.	Nom.	Max.
10-32	7/16″	.09	.3	.8	.2	.5	1.2
1/4″-28	9/16″	.07	.25	.6	.15	.4	.9
1/4″-28	11/16″	.05	.15	.4	.10	.25	.6
3/8″-24	1 1/16″	.02	.06	.15	.05	.1	.25
1/2″-20	1 1/16″	.02	.065	.2	.05	.12	.3
3/4″-16	1 1/4″	.025	.08	.2	.06	.15	.35
3/4″-16	1 5/8″	.015	.04	.10	.03	.07	.15
Flat Based	1 7/8″	.01	.025	.07			

Stud Insulated With 5 Mil Mica Washer

10-32	7/16″	1.2	2.5	4.5
1/4″-28	9/16″	.9	2.0	3.5
1/4″-28	11/16″	.7	1.5	2.5

PRESS PAK SINGLE INTERFACE – LUBRICATED

Press Pak Interface Dia.	Nominal Clamp Force	← $R_{\theta CS}$ – °C/W → Minimum	Nominal	Maximum
3/4″	800	0.04	0.06	0.20
1″	2300	0.02	0.03	0.10
1 1/4″	2300	0.015	0.022	0.08
1 1/3″	4000	0.014	0.02	0.07

TABLE 18.1 INTERFACE CASE TO EXCHANGER THERMAL RESISTANCES

—APPLICATION—

Corrosive & High Moisture Ambient Environment		Dry, Pollution Free Ambient Environment
Plated Heat Exchangers Necessary		A) Heat Exchanger unplated:
Silicone Oil	Silicone Grease	Dow Corning DC19
Dow Corning DC 703	Dow Corning DC 3, 4, 340 and 640	Burndy Penetrox* A
		Alcoa #2
General Electric SF 1017	General Electric G623	B) Heat Exchanger plated: Grease or oil not critical

*Contains Filler Particles.

Additional oils and greases available from all major heat exchanger suppliers. The above thermal oils and greases have been tested and stressed by thermal cyclic life testing.

TABLE 18.2 THERMAL COMPOUND APPLICATION TABLE

The values of $R_{\theta CS}$ given in Table 18.2 under the nominal heading are easily achieved by following the recommendations listed above and on the thyristor data sheets. If one or more surfaces are not per recommendations, values of $R_{\theta CS}$ can easily reach the maximum values indicated and under extreme conditions exceed given values where torque or force applied is grossly misapplied. Minimum values are achievable under tightly controlled assembly conditions. It is not recommended that minimum values be used for design purposes unless quality sampling audits are made to ensure conformance to design values.

18.2.1.3 Electrical Isolation Case to Heat Exchanger

In some applications it is desirable to electrically insulate the semiconductor case from the heat exchanger. Hardware kits for this purpose are available for stud-mounted semiconductors with machine threads in the low and medium power ratings. These kits generally employ a .003 to .005 inch thick piece of mica or bonded fiberglass to electrically isolate the two surfaces, yet provide a thermal path between the surfaces. As evidenced by the data in Table 18.2, the thermal resistance of the joint may be raised as much as ten times by use of this insulation. As in the direct metal-to-metal joint, some improvement in thermal resistance can be made by using grease on each side of the mica.

Tests using beryllium oxide (99 per cent) for electrical insulation have shown this material to be excellent in heat transfer. Insulating a semiconductor with a ½-20 stud, using BeO (99 percent) washers (1.00 inch OD x .52 inch ID x .125 thk) gave a stud-fin contact thermal resistance of 0.14°C/watt. Applying thermal grease to all contact surfaces decreased that thermal resistance to 0.1°C/watt.

Beryllium oxide discs are also available with one or both sides metalized. With this metallization it is possible to solder the semiconductor case, the heat exchanger, or both to the BeO disc. This technique is particularly useful with the flat-bottom press fit package. Figure 18.4 shows the drastic improvement in case-to-sink thermal impedance using the metalized BeO and solder technique.

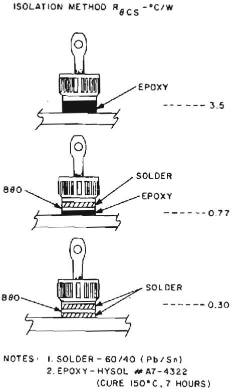


FIGURE 18.4 MOUNTING THE PRESS FIT PACKAGE WITH BERYLLIUM OXIDE INSULATION

Low Power stud thyristors are available from General Electric with integral beryllium oxide washers as shown in Figure 18.5. The additional thermal resistance, $R_{\theta JC}$, due to the beryllium isolation is 0.3°C/watt for the ¼-28 stud shown in Figure 18.5.

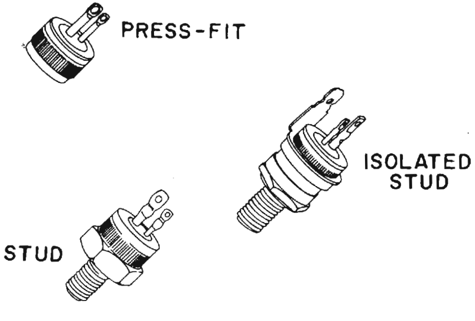


FIGURE 18.5 EXAMPLE OF AVAILABLE BERYLLIUM OXIDE ISOLATED STUD THYRISTORS

WARNING: Beryllium oxide discs and/or products incorporating beryllium oxide ceramics should be handled with care. Do not crush, grind, or abrade these portions of the thyristors because the dust resulting from such action is hazardous if inhaled.

Beryllium oxide washers in large, formed sizes and small quantities are basically somewhat expensive items. However, careful consideration should be given to the over-all economics before using any other material when electrical insulation is required. Several standard washer sizes are available from companies such as National Beryllia Corporation, Frenchtown Porcelain, or Brush Beryllium Company.

Another method used for insulating the semiconductor case from the heat exchanger is to directly solder the device to a small metal plate and then insulate that from the heat exchanger. Figure 18.6 shows this approach used with the flat-bottomed press-fit package. The SCR is soldered to a flat metal plate (say 3 or 4 square inches in area). Soldering must be accomplished below 200°C; a 60-40 (Pb-Sn) solder can be employed at about 180°C. A solder which looks quite promising for this application is "Alloy 82" from Alloys Unlimited Inc. This is a lead-tin-indium (37½-37½-25) perform of 468 mils diameter and 9.5 mils thickness. Soldering with this alloy can be accomplished at 150°C.

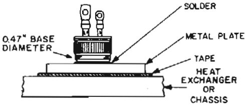


FIGURE 18.6 MOUNTING THE PRESS-FIT PACKAGE WITH TAPE INSULATION

The SCR-flatplate assembly is then mounted to the heat exchanger by means of an epoxy coated, mylar tape. The tape recommended is Scotch* Brand #75. This is a one mil mylar tape with about 2 mils of epoxy (when cured) on both sides. The epoxy cures at 121°C in three hours.

The advantage of the above outlined mounting technique is that the operating heat generated at the device junction is first spread out over a large physical area before it tries to traverse the insulating medium. This reduces the total thermal resistance of that insulation.

Other techniques employing the direct use of epoxy adhesives, epoxies with a filler, and the direct use of insulating tape have been successfully employed.[4] Since in most cases a rather high price in current rating is paid in thermal resistance for insulated mounting, such mounting is not recommended for high power SCR's.

For comparison of the tape insulation method with the beryllium oxide method of Figure 18.4 a conservative case to exchanger value of 1.2°C/watt has been measured using the following geometry and a press fit package as shown in Figure 18.6. 2″ x 1⅜″ x .050″ copper spreader plate with a Scotch* Brand #75, one mil mylar tape, with 2 mil epoxy layer (when cured) on each side.

Figure 18.7 illustrates the design trade-off factors available to the designer regarding heat spreader plate size and plate thickness.

*Trademark of 3M Corp.

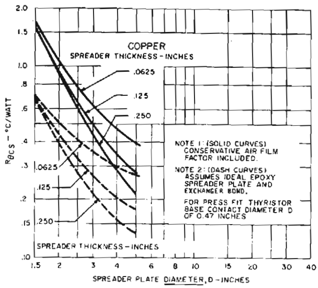


FIGURE 18.7 EFFECT OF SPREADER PLATE AREA & THICKNESS ON CASE TO EXCHANGER R_θ

The curves are based on the assumption that the heat spreader plate acts like a heat exchanger fin with cooling on one side only. Thus the nomograph of Figure 18.31 is applicable. The design example below details the use of the nomograph for this application. Figure 18.7 is applicable for square plates as well. Using the conversion factor $D = 1.128E$, where D is the spreader plate diameter as given in the figure and E is the length of the side of a square plate.

Example heat spreading plate calculation

Given: – Copper spreading plate 2″ x 2″ square and 0.10″ thick

– Thyristor press fit base diameter $d = 0.59''$

– Insulation material

1 mil mylar

2 mils epoxy each side (cured)

Problem: Determine case to exchanger thermal resistance $R_{\theta CS}$

Solution:

1st step: Find total heat transfer coefficient, h. For mylar and epoxy:

$$h_m \Delta x = 0.004 \frac{\text{watt in}}{\text{in}^2\ ^\circ\text{C}} \text{ where } \Delta x = \text{film thickness,}$$

0.005 inches

$$\text{Then } h_m = \frac{0.004 \dfrac{\text{watt in}}{\text{in}^2\ ^\circ\text{C}}}{0.005 \text{ in}} = 0.8 \text{ (watt/in}^2\ ^\circ\text{C)}$$

$$\text{and } h = 1/\left(\frac{1}{h_m} + \frac{1}{h_f}\right)$$

where h_f is due to air film in epoxy voids. $1/h_f$ is conservatively found to be equal to 1.25.

$$\text{Then } h = \frac{1}{1/0.8 + 1.25} = 0.4.$$ Since h has the units of thermal conduction/area, 1/h has the units of thermal resistance x area.

2nd step: Determine fin effectiveness from nomogram of Figure 18.31.

$D = 1.128E$ where E is the square fin size

$D = 1.128 \times 2''$

$= 2.256''$

$$b = \frac{D - d}{2} = (2.256 - 0.47)/2$$

$= 0.89$

$D/d = 2.256/0.47$

$= 4.8$

$\delta = 0.100$ inch plate thickness

Using the nomogram:

Note: the h value is halved. Since the nomogram was designed for both sides of the fin to transfer heat and only one side of the plate is assumed to be conducting heat.

Thus for $h/2 = .2$ watt/in² °C and thickness $\delta = 0.100$ inch, $\alpha = .6$.

Through $b = 0.89$ and $\alpha = .6$, a line is extended to the graph where $D/d = 4.8$, η is found to be 0.83.

3rd step: Determine $R_{\theta CS}$

$$R_{\theta CS} = \frac{1}{\eta A h} = \frac{1}{0.83 \times 2^2 \text{ in}^2 \times 0.4 \dfrac{\text{watt}}{\text{in}^2\,°\text{C}}}$$

$$= \frac{1}{1.33}$$

$$= 0.75\ °\text{C/watt}$$

18.2.2 Mounting the Power Tab

Figure 18.8 shows various configurations of the power tab package. Some configurations of the package are provided with an anode tab for mounting directly to an appropriate heat exchanger. Because of this unique package design, it can be mounted in a variety of methods, depending upon the heat exchanger requirements and the circuit packaging methods.

As a service to its customers, the General Electric Company provides a lead and tab shaping capability. Any of the derived types shown in Figure 18.8 are available.

The tab and the leads will bend easily, either perpendicular to the flat or to any angle, and may also be bent, if desired, immediately next to the plastic case. For sharp angle bends (90° or larger), a lead should be bent only once since repeated bending will fatigue and break the lead. Bending in other directions may be performed as long as the lead is held firmly between the case and the bend, so that the strain on the lead is not transmitted to the plastic case.

The mounting tab may also be bent or formed into any convenient shape so long as it is held firmly between the plastic case and the area to be formed or bent. Without this precaution, bending may fracture the plastic case and permanently damage the unit.

When used as a lead mounted device, without heat exchanger, thermal characteristics are available from the device data sheet in the form of ambient temperature vs on-state current curves for all four types.

In-line sockets to accommodate the 2 or 3 flat leads of the power tab package are available for printed circuit board or chassis mounting. These sockets, No. 77-115 (press-fit) or No. 77-116 (flange), may be obtained from the Connector Division, Amphenol Corp., 1830 South 54th Avenue, Chicago, Illinois 60650.

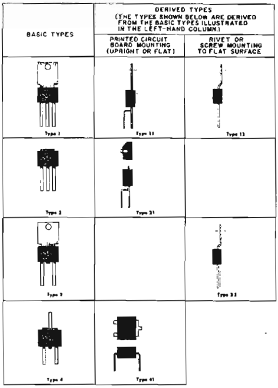


FIGURE 18.8 POWER TAB PACKAGE CONFIGURATIONS

Insulated hardware kits are available from General Electric. Kit details are given on power tab device specification sheets.

When mounting the power tab package to a heat exchanger the tab or "case" to exchanger thermal resistance $R_{\theta CS}$ is a function of mounting method. Table 18.3 illustrates the various combinations of mounting methods with accompanying values of $R_{\theta CS}$. The reference point for tab temperature measurements is illustrated by Figure 18.9.

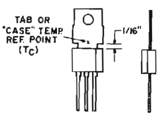
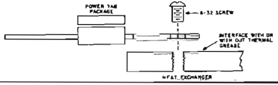
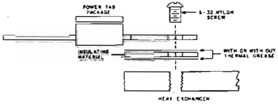


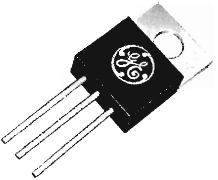
FIGURE 18.9 TAB OR "CASE" TEMPERATURE REFERENCE POINT FOR POWER TAB PACKAGE

MOUNTING ILLUSTRATION	INSULATING MATERIAL	THERMAL GREASE	FASTENER USED	NOMINAL $R_{\theta CS}$ °C/WATT
	None	None	Screw(1)/ Rivet(2)	5.25
	None	Yes	Screw/Rivet	2.0
	None	None	60/40 Solder	.25
	.003″ Mica	None	Screw/Rivet	9.15
	.003″ Mica	Yes	Screw/Rivet	3.75
	.002″ Mylar Tape(3)	None	Screw/Rivet	10.3
	.002″ Mylar Tape	Yes	Screw/Rivet	5.7
	.006″ Black Elect. Tape	None	Screw/Rivet	12.5
	.006″ Black Elect. Tape	Yes	Screw/Rivet	10.3

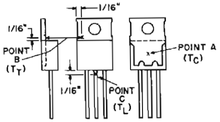
Notes: (1) 6-32 screw torqued to 5-6 in-lbs.
(2) Use good quality 3/32″ diameter semi-tubular rivet and eyelet of brass backed .250″ OD washers under both ends. Top washer may be omitted if rivet head is larger than 0.250″ diameter. Hydraulic or pneumatic force should be used for rivet pressure application. Follow rivet manufacturer's instructions for force level values.
(3) Tapes greased on non-stick surfaces only.

TABLE 18.3 NOMINAL $R_{\theta CS}$ FOR POWER TAB PACKAGES

18.2.3 Mounting the Power Pac Package (TO-220)



(a) Photo of Power Pac



(b) Outline Drawing of the Power Pac Package Showing Reference Temperature Locations

FIGURE 18.10 POWER PAC PACKAGE & REFERENCE TEMPERATURE LOCATIONS

The power pac package (Figure 18.10) sometimes presents a difficulty in measuring the case temperature reference point because of its inaccessibility after the device has been attached to a heat exchanger. $R_{\theta JC}$ is defined as the thermal resistance from the junction to point A on the case. However, this point becomes inaccessible to the user (not to mention the manufacturer) when the device is correctly mounted to a heat exchanger.

It has been verified experimentally that the temperature 1/16″ from the molding of the round center lead common to the case (T_L of point C in Figure 18.10(b)) closely approximates T_C. Experiments have shown that, with 5 mil copper-constantan thermocouples mounted to points A and C and under free air conditions and no I^2R heating in the center lead, that T_L and T_C are within 1°C of each other. If the center lead conducts a 10 amp (rms) current, this will raise the T_L approximately 3°C higher than T_C. Therefore, T_C and T_L are used interchangeably and, in general:

$$R_{\theta LS} \cong R_{\theta CS}$$

However, T_L can also be difficult to measure because of the small size of this lead. T_L can best be measured by first lightly filing a flat surface on the rounded lead at point C. A .015″ diameter hole can then be drilled completely through the lead. A 5 mil copper-constantan is then fed into this hole and soldered in place using 60/40 solder. One must still guard against measurement errors due to thermal conduction along the lead or because of I^2R heating if that lead is being used to conduct load current.

The next logical reference point would be the tab temperature (T_T) at point B, also of Figure 18.10(b). Call this thermal resistance $R_{\theta TS}$. Unfortunately, this is not an absolute quantity but depends upon how the device is mounted. Figure 18.11 illustrates this point. There are two main paths for heat flow from point A to the heat exchanger, namely via $R_{\theta 1}$ and $R_{\theta 2} + R_{\theta 3}$. $R_{\theta 1}$ and $R_{\theta 2}$ actually represent a distributed thermal network but it has been simplified to just two paths for clarity. The combined thermal resistance $[R_{\theta 2} \times (R_{\theta 1} + R_{\theta 2})/(R_{\theta 1} + R_{\theta 2} + R_{\theta 3})]$ varies from a very small value, typically .4°C/watt if the power pac is soldered down to the heat exchanger to a very high

value ($\sim$ 1.5°C/watt) if the package overhangs the heat exchanger.

Since $R_{\theta JT}$ is not an absolute device quantity, it cannot be specified on the manufacturer's spec sheet.

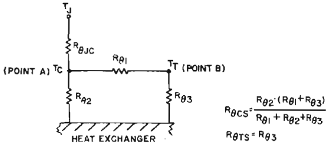


FIGURE 18.11 THERMAL MODEL FOR THE POWER PAC CASE SHOWING THE POSSIBLE HEAT PATHS CASE TO EXCHANGER

However since by definition:

$$T_J = T_C + P \cdot R_{\theta JC} \tag{1}$$

or

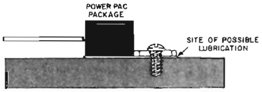
$$T_J = T_T + P \cdot R_{\theta JT} \tag{2}$$

it can be shown that

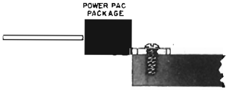
$$R_{\theta JT} = R_{\theta JC} + R_{\theta CS} - R_{\theta TC} \tag{3}$$

Then by listing nominal values of $R_{\theta TS}$ and $R_{\theta CS}$, $R_{\theta JT}$ can be computed and the designer can easily verify his design by placing a thermocouple at point B and using Equations 3 and 2.

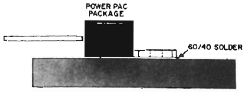
Figure 18.12 illustrates some possible mounting methods for the standard power pac package. Table 18.4 lists nominal thermal resistance values for each of the configurations shown in Figure 18.12.



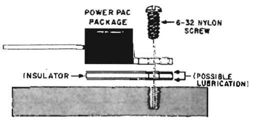
(a) Basic Power Pac Mounting Configuration



(b) Power Pac Overhanging the Heat Exchanger



(c) Power Pac Soldered Down to Heat Exchanger



(d) Basic Insulated Power Pac Mounting Configuration

FIGURE 18.12 STANDARD POWER PAC PACKAGE MOUNTING CONFIGURATIONS

Formed lead configurations of the power pac package are available for TO-66 equivalent mounting and other configurations as shown in Figures 18.13(a) and (b).

Mounting Illustration Figure 18.12	Electrical Insulating Material	Grease	Type of Mounting	Nominal $R_{\theta TS}$	Nominal $R_{\theta CS}$
(a)	None	None	Screw(1)/ Rivet(2)	0.5°C/W	1.85°C/W
(a)	None	Yes	Screw(1)/ Rivet(2)	0.3	1.45
(b)	None	Yes	Screw(1)/ Rivet(2)	0.5	2.0
(c)	None	None	60/40 Solder(5)	0.028	0.45
(d)	.003″ Mica Washer	None	Screw/Rivet	4.9	6.5
(d)	.003″ Mica Washer	Yes(3)	Screw/Rivet	1.3	2.5
(d)	Mylar	None	Screw/Rivet	5.2	6.8
(d)	Mylar	Yes(4)	Screw/Rivet	2.6	3.9
(d)	Black Elect. Tape	None	Screw/Rivet	6.4	8.0
(d)	Black Elect. Tape	Yes	Screw/Rivet	3.9	5.3

Notes: (1) 6/32 screw to 12 in-lbs.
(2) Use good quality 1/8 inch diameter semi tubular rivet and eyelet of brass backed by 0.300 inch OD washers under both ends. Top washer may be omitted if rivet head is larger than 0.300 inch diameter. Hydraulic or pneumatic force should be used for rivet pressure application. Follow rivet manufacturer's instructions for force level values.
(3) Mica washer greased on both sides.
(4) Tapes greased on non-stick surfaces only.
(5) Maximum solder temperature – 200°C. Activated flux is recommended.

TABLE 18.4 CASE TO HEAT EXCHANGER THERMAL RESISTANCE VALUES FOR POWER PAC PACKAGE

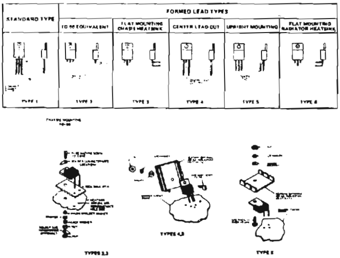


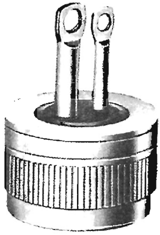
FIGURE 18.13(a) TO-66 EQUIVALENT & OTHER POWER PAC PACKAGE CONFIGURATIONS
(b) SUGGESTED MOUNTING METHODS FOR POWER PAC PACKAGE TYPES 2 THROUGH 6

Insulated hardware kits are available from General Electric. Kit details are given on power pac device specification sheets.

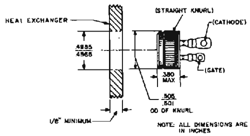
The leads of the power pac package may be bent subject to the same constraints of Section 18.2.2 stated for the power tab leads.

18.2.4 Mounting the Press Fit Package

Many medium current SCR's employ the popular "press fit" package shown in Figure 18.14(a).



(a) Photo of Press Fit Package



(b) Mounting the Press Fit Package

FIGURE 18.14 PRESS FIT PACKAGE

This package is designed primarily for forced insertion into a slightly undersized hole in the heat exchanger. When properly mounted this type of SCR has a lower thermal drop to the heat exchanger than the stud type mounting. Also, in high volume applications the cost of this type of mounting is generally less than that for the stud type of SCR.

The following simple procedures should be followed when press-fitting appropriate SCR's:

1. Heat exchanger materials may be copper, aluminum, or steel in order of preference. The heat exchanger thickness should be a minimum of 1/8 inch, the width of the knurl on the housing.
2. The hole dimensions are shown in Figure 18.14. The hole may be punched and reamed in a flat plate or extruded and sized in sheet metal. A slight chamfer on the hole should be used to guide the housing.
3. To insure maximum heat transfer the entire knurl should be in contact with the heat exchanger. The unit must not be inserted into the heat exchanger past the knurl. This is to prevent the header from taking pressure off the knurl in a deep hole.
4. The insertion force must be limited to 800 pounds. This is to prevent misalignment with the hole and/or excessive unit-to-hole interference. Pressure must be uniformly applied to the face of the header as shown in Figure 18.15.

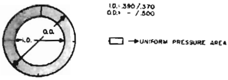


FIGURE 18.15 AREA OF APPLYING PRESSURE TO PRESS-FIT POWER SEMICONDUCTOR

If the device is inserted in the above prescribed manner (using a copper heat exchanger), the thermal resistance, case to heat exchanger, will be less than 0.5°C/watt. The insertion is generally accomplished by means of an hydraulic ram. Reading the pressure and knowing the piston area, one can pre-set the maximum insertion force. Another possible insertion method which is simple to employ, but which gives no provision for measuring insertion force, is accomplished by the use of two blocks of wood and a bench vise as shown in Figure 18.16.

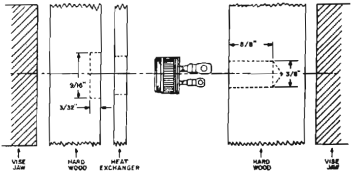


FIGURE 18.16 USE OF VISE TO INSERT PRESS-FIT POWER SEMICONDUCTOR

There are commercially available heat exchangers specifically designed to accommodate press-fit devices. One such is a radial fin semiconductor cooler (NC-300-R series) manufactured by Wakefield Engineering Inc. These coolers are available in different sizes with hole accommodation for one or two press-fit units.

Several other mounting methods for press-fit devices are possible. Different types of mountings will demonstrate different thermal characteristics and in a good many cases the characteristics will not be readily predictable from theory. For suggestions on different mounting techniques, see Reference 5.

18.2.5 Mounting the Stud Type SCR

The stud-mounted SCR is a particularly flexible component and has wide acceptance. This type of SCR uses a copper or aluminum stud with a machine thread for making mechanical, electrical and thermal contact to a heat exchanger of the user's choosing.

If the hole is punched, the fin should be subsequently blanked. If the hole is drilled, the burr should be carefully removed. The hole size should be between 0.005 and 0.015 inch larger than the stud outside diameter. If the stud has a fillet where the thread meets the flat surface of the hex, the fin hole should be chamfered to prevent the stud from hanging up on this fillet.

Mounting straight threaded copper studs into a threaded hole in an aluminum fin is not recommended. Unequal temperature coefficients of expansion of aluminum and copper cause "thermal ratcheting." This tends to unscrew the copper stud from the threaded hole as the temperature cycles. The result is higher stud-fin contact thermal resistance.

Where a copper stud is screwed into a tapped hole in a copper heat exchanger, extreme care must be taken to assure that drilling and tapping are at right angles with the heat exchanger surface.

When mounting studs to a fin through a clearance hole by means of a nut on the backside, relaxation and metal creep may cause the mounting to gradually loosen. This condition is accelerated by temperature cycling and is dependent upon the magnitude of the time-temperature relation. As a consequence of this condition, the stud-fin contact thermal resistance will increase with time-at-temperature because of a loss of contact pressure. Tests have shown that after 1000 hours of operation, the stud-fin contact thermal resistance can increase as much as three times the initial value.

To minimize the effect of relaxation, which is common in any fastener under torque, it is recommended that a belleville spring washer be used between the nut and fin. A commercially available nut-belleville washer assembly, made by Shakeproof Corp., Elgin, Illinois, has been found to be satisfactory for maintaining the initial stud-fin contact thermal resistance. Tests using the ⅜, ½ and ¾ inch nut-washer assembly, Shakeproof numbers ND16470, ND16105, and ND16501 respectively, showed a 11 per cent maximum increase in the initial stud-fin contact thermal resistance after 1000 hours at 150°C.

Good thermal contact between the semiconductor stud and the heat exchanger requires adequate pressure between these two surfaces as applied by torque on the threads of the device. However, torque beyond a certain point no longer improves the thermal contact and may mechanically stress the SCR junction and materials soldered or brazed to the stud inside the housing. Permanent damage to the device characteristics may result. For this reason, precise adherence to the manufacturer's torque recommendations is necessary, and a torque wrench should *always* be used in mounting this type of semiconductor.

Data sheets list recommended torque values. The torques are for clean, dry threads except for the C280, C282, C286 and C290 SCR types and A291, A295 rectifier types where torque values apply for greased threads. Also, on semiconductors with a ⅜-24 stud or larger, the torque is applied on the nut while holding the semiconductor stationary.

Torque wrenches, such as those made by the P. A. Sturtevant Company, should be chosen for the accurate range of torque that is to be used on a given rectifier diode or SCR.

18.2.6 Mounting the Flat Base Semiconductor

A number of General Electric high current SCR's and rectifier diodes are provided in a flat base package such as shown in Figure 18.17. At present only one package size is available in this flat base configuration and therefore our discussion can be specific. However, the points covered will generally apply to any similar flat-base package.

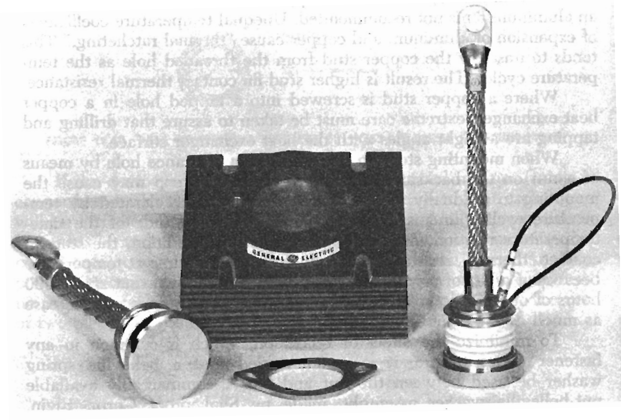


FIGURE 18.17 THE FLAT-BASE POWER SEMICONDUCTOR

The following mounting hardware is supplied with each device:

- 4 bolts (2 lengths)
- 2 hex nuts
- 1 spring clamp
- 2 spacers

For those mounting situations requiring a second spring clamp (see Figure 18.19), it should be requested when ordering SCR. The second clamp for this SCR is supplied at no additional cost. Heat exchanger surface preparation is described in Section 18.2.1.

18.2.6.1 Heat Exchanger Thickness

1. *For all heat exchangers over 7/8″ in thickness at mounting surface*, two holes are to be drilled and tapped for a 5/16-18 UNC2A bolt to a depth of 7/8″. See Figure 18.18.
2. *For all heat exchangers 7/8″ and under in depth*, two clearance holes are to be drilled for a 5/16″ bolt, 2 1/2″ ± 1/64″ apart, center line to center line.

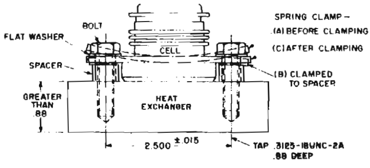
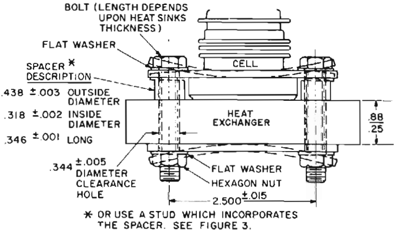


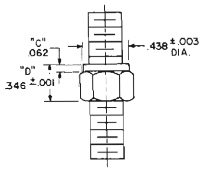
FIGURE 18.18 DRILLING THE HEAT EXCHANGER FOR HEAT EXCHANGERS THICKER THAN 7/8 INCH

18.2.6.2 Mounting Procedure

1. Place the spring washer down over the cell, (A) and insert the two bolts with washers in mounting holes of the spring clamp. When mounting this cell to the heat exchanger, insert two spacers (0.335 ± .001″ in height) between the spring clamp and heat exchanger on the bolts (see Figures 18.18, 18.19(a)).
2. Run both bolts or nuts down symmetrically with the fingers till they contact the spring; then with a torque wrench alternately turn the bolts or nuts ½ turn maximum apiece until they contact the spacers. (B) Then back off, 1 flat (60°). (C) Wipe excess grease from around the base of the cell.
   a) On heat exchangers thicker than .88″ use .3125 – 18UNC-2A x 1.25″ long bolts. See Figure 18.18.
   b) On heat exchangers from .25″ to .88″ thick use longer bolts and a back-up spring clamp or equivalent. See Figure 18.19(a).
   c) Heat exchangers under .25″ shall not be used.
3. When connecting the cell lead to its terminal do not put a strain on the lead by using a bolt or similar implement to bring the terminal hole in the lead in line with its contact point. This lead should be positioned so that the terminal lines up before assembling the bolt through the hole in the lug of the cell lead.
4. If current take-off is used as shown in Figure 18.19(c), the maximum thickness of the take-off should be added to spacer height. If a stud which incorporates the spacer is used, dimensions "C" and "D" should be increased by maximum thickness of the take-off. As an example, if take-off thickness is .094″ ± .003″ spacer height will be (.346″ + .097″) ± .001″.



(a) Mounting With Through Bolts



(b) Stud With Spacer

(c) Mounting With Separate Current Take-Off

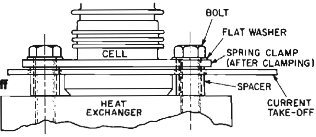


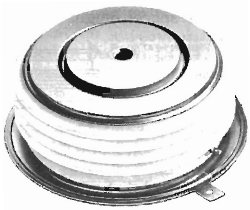
FIGURE 18.19 MOUNTING THE FLAT BASE PACKAGE

18.2.7 Mounting the Press Pak SCR

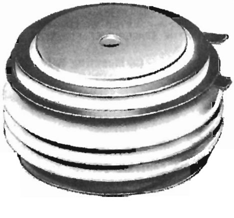
The outstanding advantage of the press paks shown in Figure 18.20 are their improved heat transfer characteristics in double-side cooled applications. The large smooth flat anode and cathode surfaces provide two direct heat flow paths which allow approximately 60% more power dissipation at the same junction temperature than the conventional stud-mounted package. This increase in performance is obtained at the expense of a more optimized mounting.

The press pak is a pressure mounted device wherein the pressure is externally applied and retained; that is, proper internal as well as external electrical and thermal contacts are maintained by pressure mounting the press pak between two heat exchangers. Of course, single sided cooling is also feasible with a heat exchanger on one side and a retaining surface on the other side.

(a) ½″ Thick Package



(b) 1″ Thick Package
1″ Diameter Pole Face for C3___ Series
1⅓″ Diameter Pole Face for C6___ Series



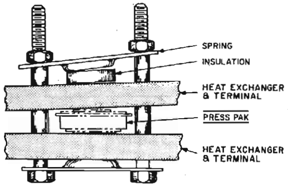
(c) 1″ Thick Package, for C5___ Series
1¼″ Diameter Pole Face

FIGURE 18.20 PRESS PAK PACKAGES AVAILABLE FROM GENERAL ELECTRIC

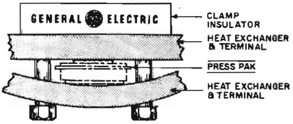
18.2.7.1 Mounting Clamp Requirements

Clamp requirements are listed below.

a) Provide provision for insuring that the force is applied through the center line of the SCR. Figure 18.21(a) illustrates what can happen should the clamp not provide for this. The resulting uneven force distribution and subsequent poor thermal and electrical contact will seriously impair device performance.



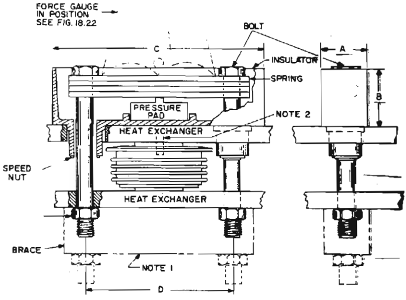
(a) Clamp Without Swivel



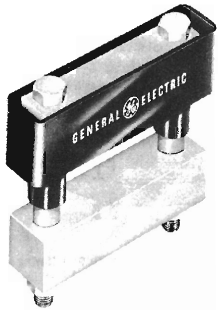
(b) Clamp With Sink Having Inadequate Rigidity

FIGURE 18.21 POTENTIAL PRESS PAK MOUNTING PROBLEMS

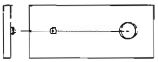
Figure 18.22 illustrates the manner in which the GE Series 2500 mounting clamp provides for force centering by means of the swivel point on top of the pressure pad in conjunction with provision for use of a grooved locating pin between the semiconductor and exchangers.



(a) Cross Section



(b) Photo



(c) Single Side Terminal

NOTES:

1. The backup brace should be used when the mounting web of the heat exchanger is not sufficiently thick to prevent the heat exchanger from bending when the clamp is tightened. Extruded aluminum heat exchangers with mounting webs less than 3/8″ thick require this brace in order to withstand the full 2500 lbs. mounting force. Refer to MOUNTING PROCEDURE for complete mounting instructions.
2. The semiconductor device to be mounted must be positively located in the center of the clamp. A 1/8″ diameter by 1/4″ long grooved or spring pin is recommended for locating the device. Use a #30 drill (0.1285″ dia.) for the hole in the heat exchanger.

FIGURE 18.22 SERIES 2500 PRESS PAK

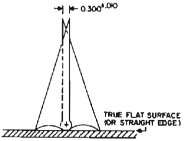
b) Maintain rated SCR package force level with provision for easily and reliably measuring force applied in assembly or in the field. Furthermore calibration means for measuring device where possible is advantageous. Figure 18.23 illustrates the operation and calibration of the force gauge designed to be used with the GE Series 2500 Series Clamp.

Place the Force Indicator Gauge firmly against the springs, as shown on the Outline Drawing, so that both ends and the middle are in solid contact with the springs (see top of Figure 18.21). The upper points of the gauge will then indicate the spring deflection, or force; correct mounting force is indicated when the points coincide.

Examples:

Less than rated force. Tighten nuts alternately ¼ turn at a time until points coincide.	Correct force.	Excessive force. Loosen nuts and start over. *NEVER* try to adjust spring force by backing off the nuts, spring friction will produce false readings. Always start at Step 1.

(a) Use of GE Series 2500 Force Gauge



To Calibrate Force Gauge:

If the gauge is suspected of being out of calibration due to wear or damage, check it on a flat surface as shown below.

If the points are not 0.300 ± .010 apart, calibrate the gauge by filing the bottom contact points.

(b) Calibration of GE Series 1000 and 2500 Force Gauges

FIGURE 18.23 USING THE PRESS PAK CLAMP FORCE INDICATOR GAUGE

c) Force spreading. The force should be transmitted through the clamp insulator by means of a pressure pad to prevent possible fracturing of the insulator and cold flow due to application of excessive compressive forces in the insulating material (see Figure 18.22).

d) Insulator dimensions. The insulator should provide creep and strike distances equal to or greater than the press pak it is clamping.

e) Provisions for maintaining assembly rigidity should be part of the clamping system. Figure 18.21(b) illustrates the uneven contact surface resulting from too weak of an exchanger on the bottom surface of the press pak. The GE clamps are supplied with an optional stiffening brace shown in Figure 18.22 (Note 1) to preclude this problem.

f) Temperature Limitations. All insulating materials and springs have temperature limitations.

Component limitations should be given. This is most apt to be a problem when cooling rectifier diodes where case temperatures greater than 100°C are the norm. The series 1000 and 2500 press pak clamps are capable of operating at insulator temperatures up to 125°C and spring temperatures up to 110°C. Clamp temperature can be reduced by inserting ceramic or other poor thermal conductivity material between the clamp insulator body and the heat source. The material should be mechanically stable with time at temperature to insure maintenance of clamp force levels by preventing spring relaxation. Rectifier diodes operated at rated T_J and single side cooled will always require a thermal insulating member between clamp and cell when the clamp insulator is opposite the heat exchanger.

Press pak semiconductors may be mounted using other than GE clamps but attention of force requirements listed on device data sheets (generally 800 lbs for ½″ press paks and 2000 lbs for the 1″ press pak except the 600 series which requires 4000 lbs per cell) must be adhered to in addition to the above requirements. Table 18.5 gives the basic data for GE power pak clamps.

Clamp No.	Data Sheet No.	Force Range Pounds	Insulator Dimension Inches—Max. A B C(1)	Center Line Mounting Hole Dimension Min.—Max. Inches D(1)	Mounting Hole Diameter Inches
1000	170.48	700-900	.885 x .855 x 2.965	2.115-2.135	0.516 ± .005
2500	170.49	2200-2400	1.000 x 1.270 x 4.520	3.095-3.105	0.875 ± .005

(1) Dimensions A, B, C and D refer to Figure 18.22.

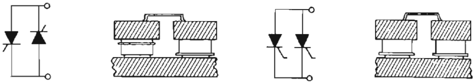
TABLE 18.5 PRESS PAK CLAMP DATA

Detailed mounting instructions concerning clamp tightening and available bolt lengths are found on the clamp data sheets. Press pak interface thermal resistance values; case-exchanger are found in Table 18.1.

18.2.7.2 Multiple Unit Mounting

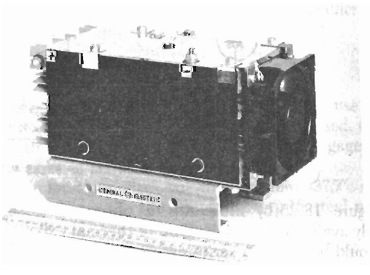
18.2.7.2.1 Parallel

The symmetry of the top and bottom surfaces of the press pak permit a variety of mounting configurations. In some applications it is desirable to mechanically parallel units. An electrical inverse parallel connection may be used as in Figure 18.24(a) or an electrically paralleled connection as in Figure 18.24(b) may be employed. The devices must not be clamped between two rigid heat exchangers because of difference in device height. One rigid heat exchangers may be common to the units on one side; on the other side either individual exchangers should be used or the heat exchangers should be flexible enough to permit good contact with each Press Pak surface. Individual clamps are needed for each device to provide the specified force. Figure 18.25(a) shows a photo of a parallel assembly available from GE as a complete unit.

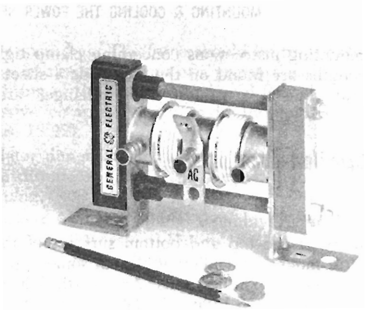


(a) (b)

FIGURE 18.24 PARALLEL MOUNTING OF PRESS PAKS



(a) Parallel (Forced Air Cooled)



(b) Series (Liquid Cooled)

FIGURE 18.25 EXAMPLES OF MOUNTED PRESS PAKS FROM FACTORY AS STANDARD ASSEMBLIES

18.2.7.2.2 Series

In-line mounting is suitable for many applications. It has the advantage of employing only one clamp. Many electrical configurations are possible with in-line mounting. Figure 18.26(a) shows a series string which could be used for high voltage circuits, or top and bottom terminals could be connected together to produce an inverse parallel pair. Figures 18.26(b) and 18.26(c) are doubler circuits (cathode common or anode common); here top and bottom terminals could be tied together to yield a parallel pair.

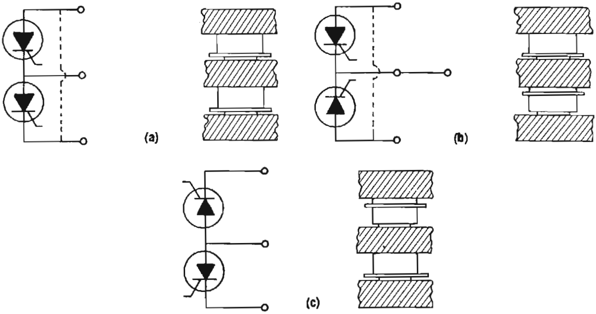


FIGURE 18.26 SERIES MOUNTING OF PRESS PAKS

Figure 18.25(b) illustrates a photo of a series liquid cooled assembly available from GE. Due to thermal expansion and contraction care should be taken in seriesing more than two cells in a given assembly. Reference 6 gives detailed calculations for making design decisions relative to material use and dimensions of a multi-cell assembly.

18.2.7.3 Handling of Press Pak

Although the press pak is a rugged component, reasonable care in handling is recommended. Dropping, or other hard jarring, of the devices can damage the silicon pellet and destroy electrical characteristics. Dents, nicks, or other distortion of the contact surfaces will also retard the flow of heat through the heat exchanger and cause the junction to overheat.

18.2.8 Unit Pak Mounting

The unit pak as shown in Figure 18.27 is intended for one-side cooling by application to one heat exchanger with two bolts. The unit pak comes from the factory equipped with both clamp and current take-off. The standard current take-off is shown, but other configurations are available and are needed should the unit pak be used with liquid cooled heat exchangers.

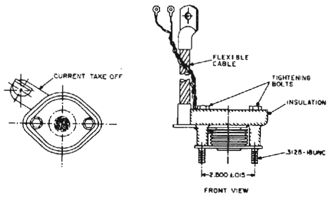


FIGURE 18.27 UNIT PAK CLAMP OUTLINE

The unit pak is only compatible with C501, C520, C530, C506, C507, C508, C510 SCR's and A500, A540 and A570 rectifier diodes.

18.2.8.1 Preparation of Heat Exchanger

With heat exchanger thickness of .80″, or greater, use tapped hole for steel Helicoil #1185-5LN-781. If Helicoil is not used, tap hole for 5⁄16″-18 thread with a minimum of 1″ length of bolt engagement in heat exchanger.

If aluminum, thinner than .80″ but thicker than .375″, is used, the bolts should be secured with the standard 5⁄16″-18 steel nut supplied with the Unit Pak

For heat exchanger mounting area thinner than .375″ use a hardened back-up plate of steel, approximately 0.5″ thick x 1″ wide x 3.500″ long.

18.2.8.2 Mounting Procedure

1. Check mounting surface for foreign particles, nicks, etc. Wipe off with lint-free paper towel.
2. Place Unit Pak on greased heat exchangers with end of bolts in mounting holes. By pressing Unit Pak down to the heat exchanger the bolts will snap up to align properly.
3. Pull down bolts hand tight with spring leveled. Locate current take off in desired orientation.
4. Turn each bolt 1½ turns with a wrench. Adjust level of spring with an additional 1 to 3 flats. The spring should now be flat and can be checked with a straight edge. Adjust the spring for flatness by turning an additional 1 to 3 flats on each bolt.

18.3 SELECTING A HEAT EXCHANGER

Heat exchanger selection is governed by the SCR package and environmental constraints. Because the heat exchanger thermal path is in series with the SCR package thermal resistance, diminishing returns are reached rapidly when attempts are made to make $R_{\theta SA}$ substantially lower than $R_{\theta JC}$. For this reason this section is divided into two sub-sections dependent upon SCR current ratings which in turn determine a particular range of heat exchanger types.

18.3.1 Low to Medium Current SCR's

SCR's in this classification have a $R_{\theta JC}$ falling in the range of 1 to 10°C/watt. Consequently heat exchangers typically used have $R_{\theta SA}$ values of from 1 to 30°C/watt. The design used most often in this range is the flat plate or "fin" and variations of it. The flat fin's chief advantage is its low cost and design flexibility. Heat is dissipated from the fin to the ambient air by both radiation and free or forced convection heat transfer. Fin selection is accomplished by use of design nomographs as illustrated in the following paragraphs.

18.3.1.1 Designing the Flat Fin Heat Exchanger

18.3.1.1.1 General

Because the mechanisms of radiation and convection heat transfer are of distinctly different nature, the so-called heat transfer coefficient

Symbol	Definition	Dimensions
A	Surface Area of Fin	$in.^2$
c	Thermal Capacity	watt-sec/lb. °C
h	Heat Transfer Coefficient	$watts/in.^2$ °C
k	Thermal Conductivity	watts/°C-inch
L	Length of Fin (in specified direction)	inches
q	Rate of Heat Flow	watts
T	Temperature	°C
ΔT	Temperature Difference	°C
T_S	Surface Temperature of Heat Exchanger	°C
T_A	Ambient Temperature	°C
V	Air Velocity	ft./min.
ϵ	Radiation Surface Emissivity	—
η	Fin Effectiveness	—
$R_{\theta SA}$	Thermal Resistance (Exchanger to Ambient)	°C/watt

TABLE 18.6 BASIC THERMAL UNITS

(h) for each effect must be calculated separately and combined with the fin effectiveness (η) to determine the over-all heat transfer coefficient if any degree of confidence is to be placed in the analytical design. The rate of heat flow, q, from the fin to the ambient air can be expressed as follows:

$$q = h\,A\,\eta\,\Delta T \tag{18.4}$$

Correspondingly the fin's thermal resistance can be expressed by

$$R_{\theta SA} = \frac{1}{h\,A\,\eta} \tag{18.5}$$

where h = total heat transfer coefficient of the fin
A = surface area of the fin
η = fin effectiveness factor
ΔT = temperature difference between hottest point on fin and ambient
$R_{\theta SA}$ = Thermal resistance (exchanger to ambient)

Table 18.6 lists these and other symbols used in the following discussion together with their dimensions.

A short discussion on each of the major factors in Equation 18.4 will reveal the variables on which they depend. The examples cited all apply to the same size fin and temperature conditions so that the reader can compare the relative magnitude of each of the various mechanisms of heat transfer.

It should be emphasized that while the individual equations are quite accurate when the conditions on which they are based are fulfilled in detail, the practical heat exchanger design will depart from the conditions to some extent because of local turbulence in the air due to mounting hardware and leads, thermal conduction down the electrical leads and the mounting for the fin, nearby radiant heat sources, chimney cooling effects caused by other heated devices above or below the cooling fins, etc. Fortunately most of these additional effects enhance rather than reduce the heat transfer. Therefore, it is common practice to disregard these fringe effects in the paper design stages except

where designs are being optimized to a high degree. Even in a highly optimized design, precisely calculated values may be subjected to substantial corrections when the design is actually checked in the prototype. The final measure of the effectiveness of the cooling fin will always be the fin temperature at the case which should never be allowed to exceed the manufacturer's rating for a given load condition.

18.3.1.1.2 Radiation

For stacked fins with surface emissivity of 0.9 or more and operating up to 200°C, the radiation coefficient (h_r) can be closely approximated by the following equation:*

$$h_r = 1.47 \times 10^{-10} \epsilon (1 - F)\left(\frac{T_S + T_A}{2} + 273\right)^3 \frac{\text{watts}}{\text{in.}^2\ °\text{C}} \quad (18.6)$$

where ϵ = surface emissivity (see Table 18.7)
F = shielding factor due to stacking ($F = 0$ for single unstacked fins)
T_S = surface temperature of cooling fin (°C)
T_A = ambient temperature (°C)

Table 18.7 indicates the wide variation in emissivity for various surface finishes. In free convection cooled applications, the radiation component of the total heat transfer is substantial, and it is therefore desirable to maximize radiation heat transfer by painting or anodizing the fin surface.

Note that oil paints regardless of color improve surface emissivity to practically an ideal level (unity).

Figure 18.28 presents Equation 18.6 in the form of a nomogram which considers the detrimental effects of stacking cooling fins. As fin spacing is reduced shielding effects become more marked, and radiation heat transfer is reduced.

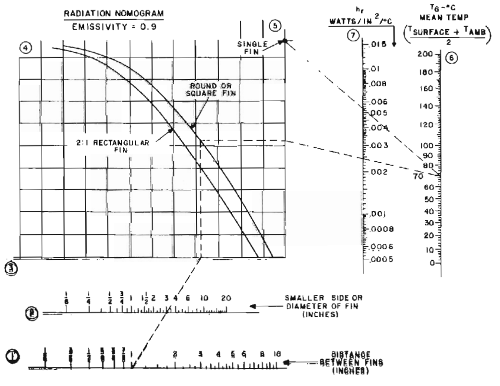


FIGURE 18.28 RADIATION NOMOGRAM (EMISSIVITY = 0.9)

Surface	Emissivity (ϵ)
Anodized Aluminum	0.7–0.9
Commercial Aluminum (Polished)	0.05
Aluminum Paint	0.27–0.67
Commercial Copper (Polished)	0.07
Oxidized Copper	0.70
Rolled Sheet Steel	0.66
Air Drying Enamel (any color)	0.85–0.91
Oil Paints (any color)	0.92–0.96
Lampblack in Shellac	0.95
Varnish	0.89–0.93

TABLE 18.7 EMISSIVITIES OF COMMON SURFACES

Example of Use of Radiation Nomogram

Given:
- Stack composed of 3″ x 3″ square cooling fins
- 1″ spacing between fins
- ambient temperature = 40°C
- fin surface temperature = 100°C

Problem: Determine coefficient of radiation heat transfer (h_r) and total radiation heat transfer (q_r) assuming fin effectiveness = 1. (See Section 18.3.1.1.5)

Solution: $$T_G = \frac{T_S + T_A}{2} = \frac{100 + 40}{2} = 70°C$$

Following the dashed line sequence starting at 1 for the above conditions, $h_r = .0024$ w/in.^{2} °C.

$q_r = h_r A \Delta T = (.0024 \text{ watts/in.}^2\ °C)(3 \times 3 \text{ in.}^2)(2 \text{ sides})(100 - 40°C) = 2.6$ watts per fin.

For single unstacked fins surrounded by 40°C ambient $h_r = .0054$ watts/in.^{2} °C by the indicated line on the nomogram.

$q_r = h_r A \Delta T = (.0054)(3 \times 3 \times 2)(100 - 40) = 5.8$ watts per fin.

18.3.1.1.3 Free or Natural Convection

For vertical fins surrounded by air at sea level and at surface temperatures up to 800°C, the free convection heat transfer coefficient (h_c) can be approximated by the following equation which assumes laminar flow of the cooling medium:[2]

$$h_c = 0.00221 \left(\frac{\Delta T}{L}\right)^{0.25} \frac{\text{watts}}{\text{in.}^2\ °C} \qquad (18.7)$$

where ΔT = temperature difference between surface and ambient air (°C)

L = vertical length of fin (inches)

This equation remains conservative for fin spacing down to approximately $\sqrt[4]{L}$ inch. Figure 18.29 presents Equation 18.7 in the form of a nomogram for convenience.

*This equation can be derived from Equations 31-3 and 31-90 in Reference 1.

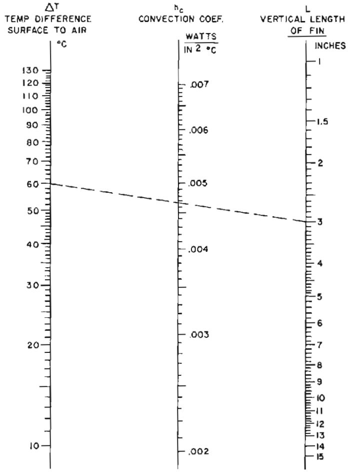


FIGURE 18.29 FREE CONVECTION NOMOGRAM (VERTICAL FINS—SEA LEVEL AIR)

Example of Use of Free Convection Nomogram

Given:
- 3″ x 3″ square cooling fin
- ambient temperature = 40°C
- fin surface temperature = 100°C

Problem: Determine free convection coefficient of heat transfer (h_c) and total convection heat transfer (q_c) assuming fin effectiveness = 1.

Solution: $\Delta T = T_S - T_A = 100 - 40 = 60°C$

$L = 3$ inches

As shown by dashed line on nomogram, $h_c = .00465$ watts/in.^{2} °C.

$q_c = h_c A \Delta T = (.00465 \text{ w/in.}^2 \text{ °C}) (3 \times 3 \text{ in.}^2) (2 \text{ sides}) (100 - 40°C) = 5.02$ watts.

Altitude derating factors for the free convection heat transfer coefficient are shown in Figure 18.30 for fins from ½ inch to 2 feet on a side.

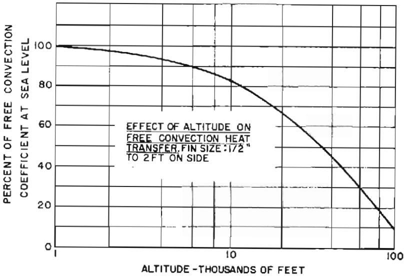


FIGURE 18.30 EFFECT OF ALTITUDE ON FREE CONVECTION HEAT TRANSFER

18.3.1.1.4 Forced Convection

When air is moved over cooling fins by external mechanical means such as fans or compressors, heat transfer is improved and the convection heat transfer coefficient can be approximated by the following equation:*

$$h_c = 11.2\sqrt{\frac{V}{L}} \times 10^{-4} \text{ watts/in.}^2 \text{ °C} \tag{18.8}$$

where V = free stream linear cooling air velocity across fin surface (ft./min.)

L = length of fin parallel to air flow (inches)

This equation is based on laminar (non-turbulent) air flow which exists for smooth fin lengths up to $L \cong C/V$, where C is a constant given in Table 18.8 for various air temperatures. For $L > C/V$, air flow becomes turbulent and heat transfer is thereby improved. Turbulent air flow and the resultant improvement in heat transfer may be achieved for shorter L's by physical projections from the fin such as wiring and the rectifier cell itself. However, turbulence increases the power requirements of the main ventilating system. Minimum spacing for the above is $B\sqrt{\frac{L}{V}}$ inches where B is also a constant given in Table 18.8.

Air Temperature	B	C
25°C	3.4	37,000
55°C	3.8	45,000
85°C	4.1	52,000
125°C	4.5	63,000
150°C	4.7	70,000

TABLE 18.8 LAMINAR FLOW LIMITATIONS

*This is accurate within 1% of Equation 7.48, Reference 2, p. 149 for air properties up to 250°C.

Figure 18.31 presents a nomogram for convenience in solving the forced convection equation, Equation 18.8 above.

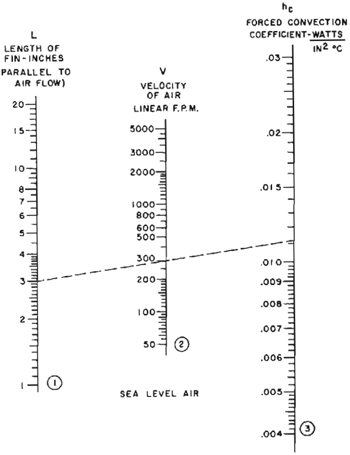


FIGURE 18.31 FORCED CONVECTION NOMOGRAM

Example of Use of Forced Air Convection Nomogram

Given: – 3″ x 3″ square cooling fin
– air velocity = 300 linear FPM
– ambient air = 40°C
– fin surface temperature = 100°C

Problem: Determine forced convection heat transfer coefficient (h_c) and total convection heat transfer (q_c) assuming fin effectiveness = 1.

Solution: L = 3 inches, V = 300 LFPM
As shown on dashed line on nomogram, h_c = .011 watt/in.^{2} °C.
$q_c = h_c\ A\ \Delta T$ = (.011 watts/in.^{2} °C) (3 x 3 in.^{2}) (2 sides) (100 – 40°C) = 11.9 watts.

18.3.1.1.5 Fin Effectiveness

For fins of thin material, the temperature of the fin decreases as distance from the heat source (the SCR) increases due to effects of surface cooling. Thus calculations of heat transfer, such as those above, which are based on the assumption that the fin is at a uniformly high temperature are optimistic and should be corrected for the poorer heat transfer which exists at the cooler extremities of the fin. The correction

factor which is used is called fin effectiveness (η). η is defined as the ratio of the heat actually transferred by the fin, to the heat that would be transferred if the entire fin were at the temperature of the hottest point on the fin. The hottest spot, of course, is adjacent to the stud of the SCR. The effectiveness depends on the length, thickness, and shape of the fin, on the total surface heat transfer coefficient h, and on the thermal conductivity k of the fin material. As defined in Equation 18.4, the total actual heat transfer may be calculated by multiplying the fin effectiveness factor by the total surface heat transfer (determined by adding the radiation and convection heat transfer as calculated in the examples above).

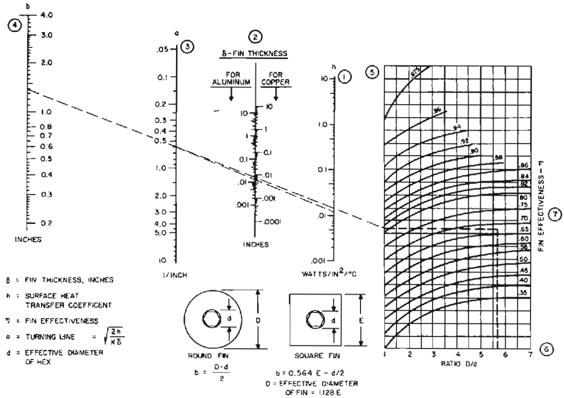


FIGURE 18.32 FIN EFFECTIVENESS NOMOGRAM FOR FLAT, UNIFORM THICKNESS FIN

Fin effectiveness can be computed by means of the nomogram shown in Figure 18.32. The typical sequence of proceeding through the nomogram is indicated by the encircled numbers adjacent to the scales.

Example of Use of Fin Effectiveness Nomogram

Given: – Stack composed of 3″ x 3″ square painted aluminum fins, each 1/64 inch thick.
– Effective stud hex diameter d = 0.59 inch.
– 1 inch spacing between fins
– 300 LFPM air velocity
– Fin temperature at stud = 100°C.
– Ambient air temperature = 40°C.

Problem: Determine total heat transfer of each fin.

Solution:

1st Step: Determine total heat transfer coefficient. Radiation heat transfer coefficient $h_r = .0024$ w/in.^{2} °C per example in Section 18.3.1.1.2.
Convection heat transfer coefficient $h_c = .011$ w/in.^{2} °C per example in Section 18.3.1.1.4.
Total heat transfer coefficient $= h_r + h_c = .0024 + .011$, $h = .0134$ w/in.^{2} °C.

2nd Step: Determine fin effectiveness factor from nomogram.

$$b = 0.564E - d/2 = (0.564)(3) - \frac{0.59}{2} = 1.39''$$

$$D/d = \frac{1.128 \times 3}{0.59} = 5.64$$

For $h = .0134$ w/in.^{2} °C and thickness $\delta = .0155$ inch. $\alpha = 0.58$ as indicated by the dashed line on the nomogram. Through $b = 1.39$ and $\alpha = 0.58$, a line is extended to the graph where $D/d = 1$. Projecting horizontally on this graph to $D/d = 5.64$, η is found to be 0.67.

3rd Step: Determine total heat transfer.
Total heat transfer $q = h\,A\,\eta\,\Delta T$
$q = (.0134 \text{ w/in.}^2\ °\text{C})\,(18 \text{ in.}^2)\,(0.67)\,(100 - 40°\text{C})$
$= 7.2$ watts per fin.

For fin materials other than copper or aluminum, use the "copper" scale on the nomogram by multiplying the actual fin thickness by the ratio of the thermal conductivity of the material being considered to the thermal conductivity of copper. Thus, for a ⅛ inch *steel* fin, enter axis 2 on the *copper* scale at 0.125 inch x 1.16/9.77 = 0.015 inch. Thermal conductivities of several commonly used fin materials are given in Table 18.9.

Material	Density (lbs/in.^{3})	Heat Capacity (c) (watt-sec./lb. °C)	Thermal Conductivity (k) (watts/in. °C)
Aluminum	0.098	407	5.23
Brass (70 Cu, 30 Zn)	0.30	179	2.70
Copper	0.32	175	9.77
Steel	0.28	204	1.16

TABLE 18.9 THERMAL PROPERTIES OF HEAT EXCHANGER MATERIALS

In general, it will be found that fin thickness should vary approximately as the square of the fin length in order to maintain constant fin effectiveness. Also, a multi-finned assembly will generally have superior fin effectivenss and will make better use of material and weight than a single flat fin.

18.3.1.1.6 Typical Example of Complete Fin Design

Given: – Four C35 SCR's with 9/16″ hex and 1/4″-28 thread are operated in a single-phase bridge at 10 amperes DC maximum each. The specifications for this rectifier indicate that at this current level each SCR will develop 16 watts of heat losses at its junction and that for satisfactory service at this current level, the stud temperature should be maintained below 92°C. The maximum ambient temperature is 40°C and free convection conditions apply.

Problem: Design a stack of fins to adequate cool the four SCR's in this bridge circuit.

Solution:

1st Step: Determine maximum allowable fin temperature at radius of stud hex. From Table 18.2, the thermal resistance from stud to fin for a joint with lubricant is 0.25°C/watt maximum. The maximum fin temperature therefore must not exceed 92°C – (0.25°C/watt x 16 watts) = 88°C.

2nd Step: Estimate required fin designs based on space available: 6″ x 6″ painted vertical fins at one inch spacing. Material .08 inch thick steel. Assume all cell losses are dissipated by fin.

3rd Step: Determine surface heat transfer coefficient and fin effectiveness of estimated fin design:

Radiation (from Nomogram in Figure 18.28)

$$T_G = \frac{88 + 40}{2} = 64°C \qquad h_r = .00145\ \text{w/in.}^2\ °C$$

Free Convection (from Nomogram in Figure 18.29)

$$\Delta T = 88 - 40 = 48°C \qquad h_c = .0037\ \text{w/in.}^2\ °C$$

$$h_{total} = .0052\ \text{w/in.}^2\ °C$$

Fin Effectiveness (from Nomogram in Figure 18.32)

$D = 1.128E = 1.128 \times 6 = 6.768$

$d = 0.57$

$$b = 0.564E - d/2 = 0.564 \times 6 - \frac{0.57}{2} = 3.0$$

$$D/d = \frac{6.768}{0.57} = 11.8;\ \delta\ Cu = (.08)\ \frac{1.16}{9.77} = .0095\ \text{in.}$$

Using these parameters in the nomogram, $\eta = 55\%$.

4th Step: Determine total heat transfer for estimated fin.

$q = h\ A\ \eta\ \Delta T$

$= (.0052)\ (6 \times 6\ \text{in.}^2)\ (2\ \text{sides})\ (0.55)\ (86 - 40°C)$

$= 9.7$ watts

5th Step: Determine error in approximation. Re-estimate fin requirements, and recalculate total heat transfer. In this example, the capabilities of the initial fin design fell considerably below the requirements of 16 watts. To sufficiently in-

crease the heat transfer, a ¼″ thick copper fin would be needed. Alternately a thinner fin of larger area could be used.

From the above example it is seen that the fin heat transfer or thermal resistance is a function of temperature as well as fin material, size and geometrical configuration. Because of this fin operating temperature conditions must always be known regardless of procedure used to select fin, i.e., from a manufacturer's catalog (see Tables 18.10, 18.12) or from the above design procedure. To give the designer some perspective on the subject, Figure 18.32 is shown for the power tab package at typical operating conditions. Similar curves can be made up by using the above design procedure for thicker fins and other SCR packages such as the power tab.

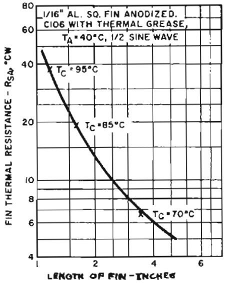


FIGURE 18.33 HEAT EXCHANGER SQUARE FIN DESIGN FOR POWER TAB PACKAGE (SINGLE FIN)

18.3.1.2 Example of Calculating the Transient Thermal Impedance Curve for a Specific Heat Exchanger Design

Problem: A cell is mounted on a painted copper fin 1/16″ thick and 4″ on a side. The fin is subjected to free convection air conditions. Find the transient thermal impedance curve for this fin. Assume that the temperature throughout the heat exchanger is uniform even under transient loading, thus permitting the heat exchanger to be represented by a single time constant. This is a good assumption for fins of relatively thick cross-section and fin effectiveness close to unity. This approach also assumes that the thermal capacity of the heat exchanger is large compared to the thermal capacity of the cell.

Solution: From fin design curves

$h_r = .005$ watt/inch² °C $h_c = .005$ watt/inch² °C

$h_{total} = h_r + h_c = .010$ watt/inch² °C

Fin thermal conductance $k = h \times A = .01 \times 4 \times 4$ inches² $\times$ 2 sides $= 0.32$ watt/°C

$$\text{Fin thermal resistance } \theta_f = \frac{1}{k} = \frac{1}{0.32} = 3.1 \text{ °C/watt}$$

$$\text{Fin thermal capacity } C = c_\rho V = \frac{175 \text{ watt-seconds}}{\text{lb } ^\circ\text{C}} \times 0.32 \text{ lb/in}^3$$

$$\times\ 4 \text{ in.} \times 4 \text{ in.} \times \tfrac{1}{16} \text{ in.} = \frac{56 \text{ watt-seconds}}{^\circ\text{C}}$$

$$\text{Thermal RC time constant} = 3.1\ ^\circ\text{C/watt} \times \frac{56 \text{ watt-seconds}}{^\circ\text{C}} = 174 \text{ seconds}$$

Equation of transient fin thermal impedance, $R\theta_{(t)F}$:

$$R\theta_{(t)F} = R\theta_F\,(1 - e^{-t/RC}) = 3.1\,(1 - e^{-t/174})$$

18.3.1.3 Selection of Commercial Heat Exchangers

Table 18.10 list heat exchanger vendors that offer heat exchangers compatible with the power tab and power pac SCR packages. Note that for the most part the exchangers are formed versions of flat plate fin designs. The formed fin offers a savings in space over the straight flat fin.

The vendor rating conditions must be carefully evaluated if the user expects the full thermal transfer capability of the exchangers to be achieved according to manufacturer's published characteristics since the actual heat transfer in a given environment is highly dependent on temperature and ambient air flow conditions. The heat exchangers shown in Table 18.10 vary in thermal resistance over the following range:

Convection Cooled	5 – 30°C/watt
Forced Cooled	2 – 15°C/watt

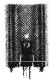
HEAT EXCHANGER VENDOR	GE POWER TAB PACKAGE	GE POWER PAC PACKAGE
Astrid Engineering, Inc. 30 Cook Court Laconia, New Hampshire Phone: AC 603 524-4443 Series 60130 Heat Sinks		
IERC 135 West Magnolia Blvd. Burbank, California 91502 Phone: AC 213 849-2481 "P" Series Dissipators Technical Bulletin 149 and 150		
Thermalloy Company 8717 Diplomacy Row Dallas, Texas 75247 Phone: AC 214 637-3333 Series 6106 and 6107 Bulletin B9-B-8		
Staver 41-51 North Saxon Avenue Bay Shore, L.I., New York 11706 Phone: AC 516 666-8000 Thermovanes Thermoflags Thermoclips		

TABLE 18.10 HEAT EXCHANGERS COMPATIBLE WITH THE POWER TAB AND POWER PAC PACKAGES

18.3.2 Medium to High Current SCR's

While the low current SCR's are predominantly cooled by flat fins, as we go up in current the designer is faced with an increasing array of possible cooling techniques. Table 18.11 shows this change in cooling technique. It is obvious that the medium current SCR straddles the fence between nearly exclusive use of flat fin at the low current and extruded heat exchangers design at the high current. Because of this overlap, part of the contents from Section 18.3.1 are applicable to medium current SCR's.

I_{RMS} Amperes	Low I	Medium I	High I
	< 25	25 – 100	> 100
Package Type	Power Tab, Pac Press Fit, Stud	Press Fit & Stud	Stud/Press Pac Flat Base
$R_{\theta JC}$ (°C/W)	> 1	1 – 0.4	.4 – .04
Predominant Heat Exchanger Type	a) Flat Fin b) Formed Flat Fin (Convection)	a) Flat Fin b) Formed Flat Fin c) Extruded Aluminum (Convection & Forced)	a) Extruded Aluminum (Convection & Forced) b) Liquid Cooling

TABLE 18.11 HEAT EXCHANGER TYPE GUIDE

18.3.2.1 Press Pak Vs Stud

Although not generally thought of as a heat exchanger question, the decision of which package type to use has a direct bearing on high current heat exchanger trade-offs. This relationship is clearly seen by Figure 18.34, where heat exchanger volume requirements for free convection press pac heat exchangers is 75% of stud heat exchangers. The savings become more pronounced when comparing forced convection exchangers where the press pak sink has a 100% volume advantage over its stud counterpart.

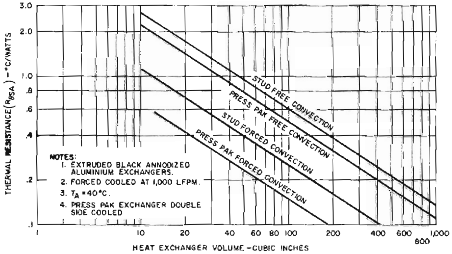


FIGURE 18.34 STEADY STATE THERMAL RESISTANCE Vs HEAT EXCHANGER VOLUME

Since heat exchanger volume has a direct relationship to heat exchanger cost, the relationship should not be taken lightly. When considering the total thermal circuit, the savings of press paks over stud packages becomes even more significant due to further reductions in thermal resistance within the semiconductor package of the press pak over the equivalent silicon when mounted in a stud package, as shown in Table 18.12.

Silicon Sub-Assembly Stud Rating Amps RMS	Stud	Press Pak (Double Side Cooled)
110 $R_{\theta JC}$ – °C/W →	C150 0.3	C350 0.135
235 $R_{\theta JC}$ – °C/W	C180 0.14	C380 0.095

TABLE 18.12 PRESS PAK Vs STUD PACKAGE THERMAL RESISTANCE

18.3.2.2 Free Vs Forced Air Convection

Forced cooling permits a four to one reduction in volume of heat exchangers. If this was the only consideration all high current SCR's would be forced cooled. Unfortunately the decision is not an easy one when equipment reliability considerations are factored into the decision. Blowers and fans due to their mechanical nature reduce equipment reliability. To compensate for reduced reliability when using blowers, designers have two options. Back-up or tandem blowers can be used to provide for blower failures. In addition the improved SCR cooling provided by blower operation may be used to provide for lower SCR operating junction temperatures. Thus blower unreliability is compensated by increased SCR reliability (see Chapter 19).

Blower requirements are determined from heat exchanger requirements. The trade-off in air flow vs thermal resistance for a typical heat exchanger is shown in Figure 18.35. Note that the knee of the curve

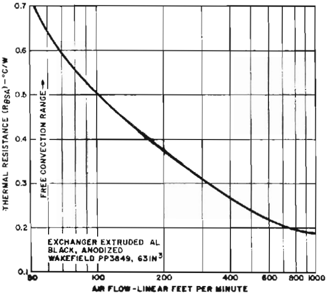


FIGURE 18.35 PRESS PAK HEAT EXCHANGER THERMAL RESISTANCE Vs AIR FLOW

beyond which diminishing returns commence to take place occurs at 500 LFPM. Blower selection procedure is outlined by use of curves similar to those shown in Figure 18.36. Blower head vs air flow curves can be likened to load lines, correspondingly the exchanger head vs air flow curve is drawn similar to a transistor or diode characteristic, the intersection of the two curves determine the operating point.

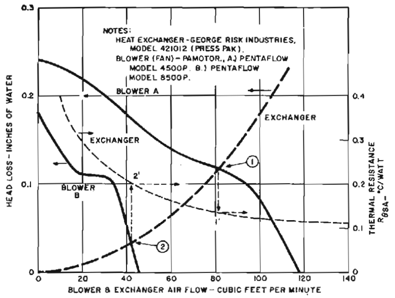


FIGURE 18.36 DETERMINING HEAT EXCHANGER-BLOWER AIR FLOW OPERATING POINT

For example the larger blower "A" intersects the heat exchanger curve at 82 CFPM thus resulting in a low thermal resistance at the operating point at 1 and 1′ of 0.14°C/watt. Since blower A provides an operating point well below the knee of the $R_{\theta SA}$ vs CPFM curve, little is to be gained by going to a larger fan. While the smaller fan's operating point is at the $R_{\theta SA}$ knee it may be a useful operating point since it provides better than a 2:1 improvement over the free convection $R_{\theta SA}$ value. Both the blower and heat exchanger curve data is provided on manufacturer's data sheets with the units shown such that a direct matching of blower to exchanger requirements is easily accomplished.

Care should be taken regarding the following additional factors when selecting exchangers and blowers.

1. Blower noise
2. Altitude effects
3. Additional head losses due to filters and ducting
4. Temperature rise in serial air flow arrangements

$$\Delta T = \left[\frac{1.76 \times P_{\text{dissipated}}}{\text{CFPM}}\right]$$

Air flow measurement techniques as well as additional considerations are discussed in detail in References 7, 8, 9, 10 and 11. For detailed manufacturer's literature consult the firms listed in Tables 18.12 and 18.13.

1. Astro Dynamic Inc.
   Second Ave. NW Industrial Park
   Burlington, Mass. 01803
2. Astrodyne Inc.
   207 Cambridge Street
   Burlington, Mass. 01803
3. International Electronic Research Corp.*
   135 W. Magnolia Blvd.
   Burbank, California 91502
4. George Risk Industries Inc.
   672 15th Avenue
   Columbus, Nebraska 68601
5. Thermaloy Co.*
   8719 Diplomacy Row
   Dallas, Texas 75247
6. Tor Inc.
   P. O. Box 8
   Irwindale, California 91706
7. Vemaline
   Wyckoff, New Jersey
8. Wakefield Engr. Inc.*
   Wakefield, Mass. 01880
9. Seifert Electronic
   Ing. Rolf Seifert
   5830 Schwelm
   Postfach 270
   West Germany
10. Hans Schaffner
    Elektronisches Bauteile
    4708 Luterbach
    Switzerland

*Supplies of liquid cooled heat exchangers in addition to extruded designs.

TABLE 18.12 MANUFACTURERS OF EXTRUDED HEAT EXCHANGERS

1. IMC Magnetics Corp.
   Eastern Division
   507 Main Street
   Westbury, New York 11591
2. Pamotor, Inc.
   770 Airport Blvd.
   Burlingame, California 94010
3. Rotating Components
   1560 5th Avenue
   Bay Shore, New York 11706
4. Rotron Inc.
   Woodstock, New York 12498
5. The Torrington Mfg. Co.
   Torrington, Conn.
6. W. W. Grainger Inc.
   3812 Pennsylvania Avenue
   Pittsburgh, Penn. 15201
7. Parker Hannifin UK (Ltd.)
   Tube & Hose Fittings Division
   Haydock Pk. Rd.
   Derby, England

TABLE 18.13 MANUFACTURERS OF BLOWERS

18.3.2.2 Liquid Cooling

Liquid cooling is gaining increasing acceptance in very high power applications because it offers the lowest values of $R_{\theta SA}$ in combination with extremely small volume requirements when using tap water for the liquid coolant. It is a natural progression from forced convection air cooling to forced liquid cooling. Space limitations do not allow adequate treatment of all facets of the subject. This section will concentrate on two aspects of the subject while providing references to further aid the designer in remaining areas.

18.3.2.2.1 Heat Exchanger Selection

Many of the same variables that determine air cooled exchanger selection also hold for liquid cooled exchanger selection criteria. The major variables are listed below.

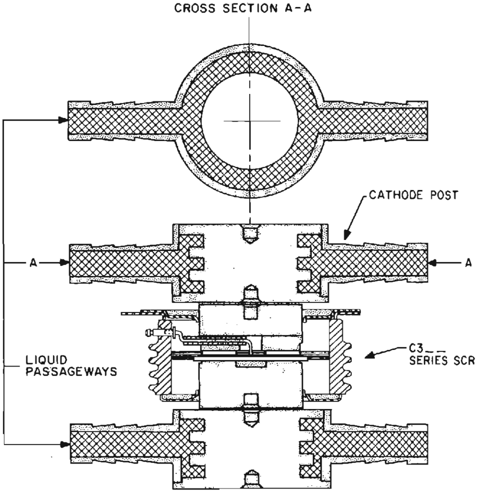
a) Thermal resistance — $R_{\theta CA}$ vs liquid flow rate
b) Pressure drop vs liquid flow rate
c) Exchanger material as it relates to atmospheric corrosion
d) Size, weight and cost
e) Ease of assembly and flexibility

Additional factors not generally met with air cooling consist of:

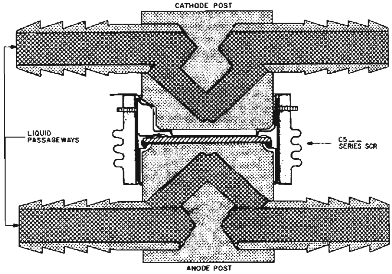
a) Susceptability to plugging (size of liquid passages)
b) Material compatability to liquid
c) Method of liquid conenctions, i.e., hose clamps, pipe fittings, etc.

These latter factors can be critical to proper exchanger selection, i.e., liquid passage ways should be a minimum of ⅜″ ID; unplated copper and aluminum is not recommended with water. Liquid connections, while not critical, should allow for tight leak free connections not generally a problem with water but definitely a consideration if liquid having low surface tension are contemplated and/or systems with high liquid pressures.

General Electric has two liquid heat exchanger designs employing two different concepts as shown in Figure 18.37(a) and (b).



(a) G6 Liquid Cooled Heat Exchanger



(b) G5 Liquid Cooled Heat Exchanger

FIGURE 18.37 HIGH PERFORMANCE LIQUID COOLED HEAT EXCHANGERS

The G6 liquid cooled exchanger or post as it is sometimes called, provides for both turbulent flow and large heat transfer area. This combined with a relatively large, short liquid passage way provides low values of $R_{\theta SA}$ and pressure drop. Furthermore, it transfers heat

to both post ends thus allowing most compact doubler and series arrangement of SCR's, with a minimum of liquid connections.

The G6 heat exchanger is available in conjunction with any of the Series C3__ SCR's in many different assembly configurations, i.e., AC switches, doublers, diode SCR combinations, etc.

The G5 heat exchanger employs a unique recessed liquid passage way as seen in Figure 18.37(b). The short Vee passage way combined with the relatively large diameter provides low pressure drops. While having a low pressure drop characteristic the Vee design also greatly reduces the SCR package thermal resistance due to the proximity of the Vee to the silicon sub-assembly. This, together with the enhanced heat transfer properties that take place at the bottom of the Vee due to liquid turbulence, enables the G5 heat exchanger to have an extremely low overall thermal resistance liquid to junction. The G5 heat exchanger is available in conjunction with any of the Series C5__ and C6__ SCR's. Like the G6, the G5 is available in a broad range of packaged assemblies.

Table 18.12 lists suppliers of liquid cooled heat exchangers.

18.3.2.2.2 Liquid Selection and Requirements

Pure, deionized, water is the best heat transfer medium when maintenance of closed loop systems are compatible with overall system design objectives and the water can be maintained at above freezing temperature. Many industrial systems employ raw tap water due to the lower initial cost.

The quality of raw water for cooling systems, where heat exchangers are not employed, should have the following purity:

1) A neutral or slightly alkaline reaction, i.e., a pH between 7.0 and 9.0.
2) A chloride content of not more than 20 parts per million: a nitrate content of not more than 10 parts per million; a sulphate content of not more than 100 parts per million.
3) A total solids content of not more than 250 parts per million.
4) A total hardness, as calcium carbonate, of not more than 250 parts per million.

Chemical analyses are not always available to assist in an appraisal of cooling water. In such cases, an electrical resistivity measurement of the water will provide a satisfactory guide to the total amounts of dissolved solids. Water having a resistivity of 2,500 ohm-centimeters or higher, when measured at about 25°C, is usually satisfactory as a coolant. The approximate amount of total dissolved solids can be determined by the equation:

$$\text{Total Dissolved Solids in Parts per Million} = \frac{640{,}000}{\text{Specific Resistivity in Ohm-Centimeters}}$$

Raw water insulating hose connections to the converter or ungrounded heat exchangers should be long enough to reduce the leakage current to a tolerable level (18″ or greater), or electrolytic targets, should be used at the hose fittings.

Reference 6 provides information on electrolytic targets, leakage currents and rust inhibitors for closed loop systems.

Whenever the coolant temperature is below ambient cabinet temperature, the possibility of accelerated external corrosion and electrolysis must be considered due to condensation of water vapor in the ambient air taking place on the semiconductor insulating surfaces. Dehumidifiers or water tempering are possible solutions to the problem.

Water tempering raises the water temperature slightly by mixing hot water with the cold supply water such that the coolant temperature is above air ambient. The dehumidifier removes moisture from the air thus substantially lowering the dew point.

When employing antifreeze solutions or oil coolants in closed loop systems, heat exchanger performance is degraded due to the inferior properties of cooling fluids other than water. Reference 13 provides formula for calculating the performance characteristic of the GE G6 heat exchanger with liquids other than water as a function of the liquid properties, i.e., viscosity, specific heat and density.

Table 18.13 contains an abbreviated list of tubing and tube fitting manufacturers.

Imperial Eastman
6300 W. Howard Street
Chicago, Illinois 60648

Norton Plastics & Synthetics Div.*
Akron, Ohio 44309

Parker & Hannifin
300 Parker Drive
Ostego, Michigan 49078

*Tubing manufacturer only

TABLE 18.13 TUBING & TUBE FITTINGS MANUFACTURERS

18.4 MEASUREMENT OF CASE TEMPERATURE

Heat exchanger design should be checked in the prototype equipment. A 10 or 12 mil thermocouple wire should be used. A copper-constantan thermocouple junction is suggested. The thermocouple junction should be carefully attached to the SCR case as indicated in Figure 18.38.

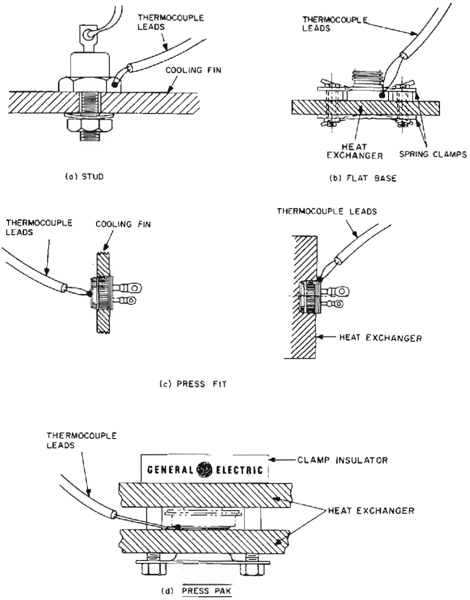


FIGURE 18.38 PREFERRED LOCATION FOR MOUNTING THERMOCOUPLE FOR CASE TEMPERATURE MEASUREMENTS

While soldering may be used for the method of attachment to low current devices, it is not practical or recommended for high current devices.

Use of an Amalgam provides the advantages of the soldering method without its danger. Its major drawback is the additional preparation time. It is far superior to fastening by peening.

18.4.1 Materials Used

Gallium – 32%; tin – 18%; copper – 50%.

325 mesh copper and tin are available from A. D. Mackay Inc., 198 Broadway, New York, New York 10038. Small balls of gallium are available from Eagle-Picher Industries, Inc., Quapaw, Oklahoma 74363.

18.4.2 Preparation

A small teflon bowl and teflon mixing stick is used to prepare Amalgam. A small amount of gallium is shaved from a gallium ball and copper is added, not quite twice as much as gallium, and a small amount of tin is added, keeping in mind the proportions specified above, but no attempt is made at actual measurement of these quantities.

The gallium at normal room temperature is solid but will liquefy at slightly higher temperatures such as from body temperature as when held between fingers. Pressure also tends to liquefy the gallium as when being forced into holes to hold thermocouple. In the type of action sought for holding thermocouples if too much gallium is used the mix will be excessively shiny and more copper should be added to cause the gallium to move from the more liquefied state to a more paste consistency.

Too little tin makes the mix dark. Tin acts as an inhibitor which retards initial set and thus facilitates packing.

The copper is used to give the mix body.

The setting time of mix is about one hour. The hardening time is approximately twenty-four hours.

The temperature at the points shown in Figure 18.38 closely approximates the temperature of the case immediately below the junction, which is usually inaccessible once the device is mounted to an exchanger. The point of measurement on the case should be shielded from any forced air which might cause localized cooling, and the leads should be kept out of any flow of cooling air since they can provide a heat flow path which will lower the temperature at the thermocouple junction.

Use of the foregoing procedures to produce a well-engineered cooling exchanger design for SCR's can pay big dividends in reliable operation, low material costs, and minimum space and weight requirements.

Unless carefully calibrated leads and instruments are available, a thermocouple bridge rather than a pyrometer should be employed. Care should be taken to keep the thermocouple leads out of electric fields that might induce error voltages in the leads.

As an alternative to using a thermocouple, temperature indicating waxes and paints bearing such trademarks as "Thermocolors" (manufactured by Curtiss-Wright Research Corporation) and "Tempilaq" (manufactured by Tempil Corporation, New York City) can be used to indicate whether the case exceeds a specific level of temperature. Careful attention should be given to the manufacturer's instructions for using this type of temperature indicator to prevent mis-application and errors. Temperature indicating paints and waxes are particularly useful in high electrical fields where substantial errors may occur in electrical measurement techniques or where the exchanger is inaccessible for thermocouple leads during the test, such as on the rotor of a rotating machine. Care must be taken in applying paints so their presence does not materially affect the emissivity of the surface.

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*Refer to Chapter 23 for availability and ordering information.

19 SCR RELIABILITY

19.1 INTRODUCTION

Reliability is not new as a concept, but the language and techniques relating to its treatment have continued to develop as technology has advanced and become increasingly complex. The need to define reliability as a product characteristic has expanded as the newer technologies have moved from laboratory to space to industry to home. The steel mill calculates the cost of down time in thousands of dollars per minute; the utility is sensitive to the low tolerance level of its customers to interruptions in service; the manufacturer of consumer equipment relies on a low incidence of in-warranty failures to maintain profitability and reputation.

The complexity of equipment, on the one hand, and the development of new components on the other, have forced industry to invest considerable effort in finding means for controlling and predicting reliability. The efforts, in many cases, were accelerated by the desire of the military to evaluate, and improve where necessary, the reliability of new devices, which offered the promise of improvements in size, weight, performance, and reliability in aerospace and weapons systems. One new device so favored was the SCR, the first of the thyristor family of devices to be commercially available.

The first SCR, the General Electric C35, was successfully qualified to the first SCR military specification only two years after it was made commercially available. At approximately that same time, a specification was finalized to which this same device was qualified as part of the highly publicized Minuteman missile high reliability program. These programs, and others that followed, contributed a great deal to the knowledge and understanding of the inherent reliability of semiconductors such as the SCR, and of those factors in design, rating, process control and application that effectively determine the reliability achieved. As a result the General Electric Co. has been able to develop and produce a wide variety of reliable thyristor devices tailored to the particular needs of various fields of application.

19.2 WHAT IS RELIABILITY ?

Reliability may be defined as the probability of performing a specific function under given conditions for a specific period of time. Reliability is a measure of time performance as opposed to quality, which is a measure of conformance to specified standards at a given point in time. Although system reliability is influenced by factors such as the selection and design of circuits. Discussion in this chapter is limited to the effects of component part reliability. In addition, the assumption is made that the parts are properly applied, and that they are not subject to stresses that exceed rated capability.

19.3 MEASUREMENT OF RELIABILITY

In the case of large systems, the common unit of reliability measurement is MTBF, or Mean Time Between Failures. MTBF expresses the average time in hours that the system operates between failures, providing a basis for estimating the cost of system maintenance. The MTBF measurement further contributes in the establishment of preventive maintenance scheduling and in estimating productivity as a function of availability, which is that percentage of time that the system can be expected to be productively operable.

The reliability of a system is based on the summation of the reliabilities of all the parts that make up the system. This process is made complex by factors such as the need for weighting based on the effect on total system performance of the failure of a particular component or circuit, and the assignment of correction factors to compensate for stress levels applied. If these complexities are ignored, and if a further simplification is made in the form of the assumption that the failure rates of the components are constant over time, then Failure Rate is the reciprocal of MTBF, and system MTBF is the reciprocal of the sum of the Failure Rates of the component parts.

19.3.1 Failure Rate

An individual component part, such as a semiconductor, does not lend itself to reliability measurement in the same manner as does a system. For this reason, the statistical approach to estimating device reliability is to relate the observed performance of a sample quantity of devices to the probable performance of an infinite quantity of similar devices operated under the same conditions for a like period of time. The statistical measurement is based on unit hours of operation, using a sampling procedure whose derivation takes into account the resolution with which the sample represents the population from which it was drawn and the general pattern of behaviour of the devices observed with time.

The sampling plan most commonly applied to semiconductors is given as Table C-1 of Mil-S-19500E, and is shown here as Figure 19.1. "Failure Rate" is a commonly used term, generally applied interchangeably with LTPD (Lot Tolerance Percent Defective), which is also called "Lambda" when used in connection with a one thousand hour test period. The table given permits calculation of failure rate at the ninety percent confidence level as a function of the number of devices observed and the number of failures occurring.

According to the sampling plan, satisfactory operation of 231 devices for 1000 hours is indicative that the failure rate is no greater than 1.0% per 1000 hours at a 90% confidence level. If it were desired to demonstrate a maximum failure rate of 0.1% per 1000 hours, the minimum sample would be 2,303 devices with no failures allowed. This could also be demonstrated with a sample of 3,891 samples, allowing one failure. In either case, a successful test would be the equivalent of demonstrating an MTBF of 1,000,000 hours for a system made up solely of the devices under test. Several points become evident in these observations:

(a) It would be extremely difficult to perform an accurate test demonstration to verify failure rate even 1.0% since the test equipment and instrumentation must have a still greater MTBF in order not to adversely affect the test results. The problem compounds as the failure rate being tested for is lowered. Not only is test equipment complexity increased, but its MTBF must be increased at the same time!

(b) The terminology "Failure Rate" is perhaps a poor choice of words. To the reliability engineer it relates the performance of a limited number of observations to the probable performance of an infinite population. To those not familiar with the statistics used, it unfortunately conveys the impression of actual percent defective.

19.4 SCR FAILURE RATES

Graphical presentations such as described in Section 19.7 have been found very useful to electronic device users as a guide for reliability predictions.

As an example of SCR reliability, a sample of approximately 950 pieces C35 type SCR's were subjected to full load, intermittent operation of 1000 hours duration in formal lot acceptance testing to MIL-S-19500/108 from 1962 through 1970. Of these only one device was observed to be a failure to the specification end point limits. The calculation of failure rate based on these results indicates the failure rate to be no more than 0.41% for 1000 hours at 90% confidence.

19.5 DESIGNING SCR'S FOR RELIABILITY

The design of reliable devices is concerned with the assurance that performance related characteristics remain within specified tolerances over the useful life of the devices. This relates particularly to thermal and mechanical design.

In the case of thermal design, the stability of thermal transfer characteristics are important for the reason that junction temperature is the major application limitation. The deterioration of the thermal path can lead to thermal runaway and device destruction. Interface materials scientifically selected for matched coefficients of expansion compatible with the rated range of temperatures are necessary to reduce the likelihood of metal fatigue.

Mechanical reliability requires the use of rigid assemblies of low mass, low moments of inertia, and the elimination of mechanical resonances in the normal ranges of vibration and shock excitation. Equally critical is the design of the protection of the junction surface, whether it be hermetic seal or passivation. Since degradation failures are mainly manifestations of changes at the junction surface, reliability is closely related to the integrity of the surface protection.

Lower costs and volume processing can be accomplished through new techniques without compromise of reliability. This has been exemplified by the C106 solid encapsulated SCR. Effective silicon dioxide passivation and the development of a compatible encapsulant have eliminated the need for glass to metal hermetic seals. Life test results indicate that the C106 is as reliable as hermetically sealed devices. Other examples are the C122, SC141 and SC146 which use glassivation as an effective means of passivation.

Minimum size of sample to be tested to assure, with a 90 percent confidence, a Lot Tolerance Percent Defective or λ no greater than the LTPD specified. The minimum quality (approximate AQL) required to accept (on the average) 19 of 20 lots is shown in parentheses for information only.

	Maximum Percent Defective (LTPD) or λ (1)	20	15	10	7	5	3	2	1.5	1	0.7	0.5	0.3	0.2	0.1
Rejection Number	Acceptance Number	Minimum Sample Sizes													
1	0	11 (0.46)	15 (0.34)	22 (0.23)	32 (0.16)	45 (0.11)	76 (0.07)	116 (0.04)	153 (0.03)	231 (0.02)	328 (0.02)	461 (0.01)	770 (0.007)	1152 (0.005)	2303 (0.002)
2	1	18 (2.0)	25 (1.4)	38 (.94)	55 (.65)	77 (.46)	129 (.28)	195 (.18)	258 (.14)	390 (.09)	555 (.06)	778 (.045)	1298 (.027)	1946 (.018)	3891 (.009)
3	2	25 (3.4)	34 (2.24)	52 (1.6)	75 (1.1)	105 (.78)	176 (.47)	266 (.31)	354 (.23)	533 (.15)	759 (.11)	1065 (.080)	1777 (.046)	2662 (.031)	5323 (.015)
4	3	32 (4.4)	43 (3.2)	65 (2.1)	94 (1.5)	132 (1.0)	221 (.62)	333 (.41)	444 (.31)	668 (.20)	953 (.14)	1337 (.10)	2228 (.061)	3341 (.041)	6681 (.018)
5	4	38 (5.3)	52 (3.9)	78 (2.6)	113 (1.8)	158 (1.3)	265 (.75)	398 (.50)	531 (.37)	798 (.25)	1140 (.17)	1599 (.12)	2667 (.074)	3997 (.049)	7994 (.025)
6	5	45 (6.0)	60 (4.4)	91 (2.9)	131 (2.0)	184 (1.4)	308 (.85)	462 (.57)	617 (.42)	927 (.28)	1323 (.20)	1855 (.14)	3099 (.084)	4638 (.056)	9275 (.028)
7	6	51 (6.6)	68 (4.9)	104 (3.2)	149 (2.2)	209 (1.6)	349 (.94)	528 (.62)	700 (.47)	1054 (.31)	1503 (.22)	2107 (.155)	3515 (.093)	5267 (.062)	10533 (.031)
8	7	57 (7.2)	77 (5.3)	116 (3.5)	166 (2.4)	234 (1.7)	390 (1.0)	589 (.67)	783 (.51)	1178 (.34)	1680 (.24)	2355 (.17)	3931 (.101)	5886 (.067)	11771 (.034)
9	8	63 (7.7)	85 (5.6)	128 (3.7)	184 (2.6)	258 (1.8)	431 (1.1)	648 (.72)	864 (.54)	1300 (.36)	1854 (.25)	2599 (.18)	4334 (.108)	6498 (.072)	12995 (.036)
10	9	69 (8.1)	93 (6.0)	140 (3.9)	201 (2.7)	282 (1.9)	471 (1.2)	709 (.77)	945 (.58)	1421 (.38)	2027 (.27)	2842 (.19)	4739 (.114)	7103 (.077)	14206 (.038)
11	10	75 (8.4)	100 (6.3)	152 (4.1)	218 (2.9)	306 (2.0)	511 (1.2)	770 (.80)	1025 (.60)	1541 (.40)	2199 (.28)	3082 (.20)	5147 (.120)	7704 (.08)	15407 (.04)

(1) The life test failure rate lambda (λ) shall be defined as the LTPD per 1000 hours.

FIGURE 19.1 LAMBDA SAMPLING PLAN AT 90% CONFIDENCE

19.6 FAILURE MECHANISMS

Failure mechanisms are those chemical and physical processes which result in eventual device failure. The kinds of mechanisms that have been observed in the semiconductor classification of component devices are shown in the table of Figure 19.2. Also shown in the table are those kinds of stresses to which each mechanism is likely to respond.

If more than a few such failure mechanisms are, to any significant degree prevalent in a given device type from a given process, it would not be reasonable to expect to achieve the degrees of reliability that have been demonstrated by many semiconductors. The dominant mechanisms to which a device type may be susceptible will vary according to the peculiarities of the design and fabrication process of that device.

STRESS → / FAILURE MECHANISM ↓	MECHANICAL				TEMPERATURE			ELECTRICAL				MISCELLANEOUS			
	STATIC FORCE	SHOCK	VIBRATION	PRESSURE (FLUID)	STATIC	SHOCK	CYCLING	VOLTAGE	CURRENT	POWER (CONTINUOUS)	POWER (CYCLED)	CORR-OSION	ABRASION	HUMIDITY	RADIATION
STRUCTURAL FLAWS – WEAK PARTS	•	•	•	•	•	•	•			•	•				
– WEAK CONNECTIONS	•	•	•	•	•	•	•			•	•				
– LOOSE PARTICLES		•	•				•				•				
– THERMAL FATIGUE						•	•				•				
ENCAPSULATION FLAWS				•		•	•			•		•	•	•	
INTERNAL CONTAMINANTS – ENTRAPPED FOREIGN GASES					•		•								
– OUTGASSING					•		•								
– ENTRAPPED IONIZABLE CONTAMINANTS					•			•							
– BASE MINORITY CARRIER TRAPPING					•				•						
– IONIC CONDUCTION					•		•	•	•	•					
– CORROSION					•			•	•	•					
MATERIAL ELECTRICAL FLAWS – JUNCTION IMPERFECTION								•	•	•					
METAL DIFFUSION					•					•					
SUSCEPTABILITY TO RADIATION															•

FIGURE 19.2 FAILURE MECHANISMS AND ASSOCIATED STRESSES

19.6.1 Structural Flaws

Structural flaws are generally considered to be the result of weak parts, discrepancies in fabrication, or inadequate mechanical design. Various in-process tests performed on the device, such as forward voltage drop at high current density levels and thermal resistance measurement, provide effective means for the monitoring of controls against such flaws. These tests also provide a means for the elimination of the occasional possible discrepant device.

The modes of failure generally associated with the mechanical flaw category of failure mechanism for an SCR are excessive on-voltage drop, failure to turn on when properly triggered, and open circuit between the anode and cathode terminals. Because these types of failure mechanism are relatively rare, the incidence of these modes of failure is low.

19.6.2 Encapsulation Flaws

Encapsulation flaws are deficiencies in the hermetic seal or passivation that will allow undesirable atmospheric impurities to reach the semiconductor element. Foreign atmospheres, such as oxygen and moisture, can react in such a way as to permanently alter the surface characteristics of the silicon metal.

A change in surface conductivity is evidenced by gradual increase of the forward and reverse blocking current. Because the SCR is a current actuated device, it will lose its capacity to block rated voltage if blocking current degrades beyond some critical point. This type of mechanism may eventually result in catastrophic failure. The rate of degradation is dependent mostly on the size of the flaw and the level of stress, particularly temperature, that is applied.

In the case of hermetically sealed devices a sequence of fine and gross leak testing can eliminate the occasional discrepant device. The use of radiflo and bubble testing has been found very effective for this means. Since the new plastic devices are solid encapsulated and have no internal cavity, conventional methods of leak testing obviously are no longer applicable; it has been necessary to develop new methods. One of these methods is the "pressure cooker" type test (29PSIA, 121°C) which has been found to be very effective in detecting devices with defective passivation.

19.6.3 Internal Contaminants

The inclusion of a source of ionizable material inside a hermetically sealed package, or under a passivation layer, can result in failure mechanisms. These mechanisms are similar to those resulting from encapsulation flaws if the inclusion is gross. If the inclusion is small, as compared to the junction area, the amount of electrical change that occurs is limited. Thus the increase in blocking current is not sufficient to effect the blocking capacity of the device.

The mechanism need not be a permanent change in the surface characteristics of the silicon. The apparent surface conductivity of the silicon can be altered by build-up and movement of electrical charges carried by the inclusions. The condition is often reversible, with recovery accomplished through the removal of electrical bias and the introduction of elevated temperature.

Because the SCR is a bistable, rather than a linear device, concern for this category of failure mechanism arises only if the forward blocking current can increase to the point where forward blocking capability is impared. The probability of occurrence is extremely low except for the possible case of the small junction area, highly sensitive devices. Even here, the mechanism is often negated through negative gate or resistor biasing in the circuit.

Removal of devices containing undesirable internal contaminants can effectively be accomplished by means of a blocking voltage burn-in screen. Ionization of the contaminants under these conditions takes place rapidly thus permitting a relatively short term burn-in. Detection of the discrepant devices is accomplished by both tight end-point limits and means to detect turn-on during the screen.

19.6.4 Material Electrical Flaws

This category of failure mechanism involves, basically, imperfections in junction formation. Discrepancies of this nature are not generally experienced with SCR's because of their relatively thick base widths and because the blocking junctions are formed by the diffusion process, which allows consistent control of both depth and uniformity of junction. Initial electrical classification would effectively remove any such discrepant devices.

19.6.5 Metal Diffusion

Of the possible failure mechanisms observed in semiconductors, metal diffusion is the least significant. Though diffusion will occur over a long period of time when two metals are in intimate contact at very high temperatures, the rate at which it progresses is too slow to have tangible effects during the useful life of the device or the system in which it is applied. For example, many SCR's are gold diffused at temperatures exceeding 800°C for times approaching two hours. In this fashion it is possible to obtain desired "speed" characteristics. To accomplish the equivalent gold diffusion at 150°C would require approximately 3×10^8 hours (34,000 years).

19.6.6 Nuclear Radiation

Early studies, concerning the radiation tolerance of semiconductor devices, indicated that thyristors were more susceptible to a degradation in electrical characteristics than bipolar transistors. This has more recently been shown to be an invalid conclusion. To a great extent the radiation resistance is determined by the N and P base widths in a thyristor and the base and collector widths in a transistor. The narrower the width, the less susceptible a device is to radiation. It is these same widths however that determine the devices' blocking voltage capability. Therefore, one should expect greater radiation resistance from lower voltage devices than from high voltage devices, regardless of whether they are thyristors or bipolar transistors. It must be kept in mind that when selecting radiation resistant devices, it is the designed blocking voltage that is critical, not the actual blocking voltage of the particular device.

The only true means for determining the actual tolerance of any device to the effects of nuclear radiation is through actual radiation exposure testing of that device. Approximate levels of SCR tolerance, however, have been determined through various tests performed on the General Electric C35 (2N685 series). Critical levels have been shown to be 10^{14} nvt for fast neutron bombardment and 5×10^5 R/sec for gamma radiation.

Fast neutron bombardment of the silicon results in permanent damage to the crystal lattice, reducing minority carrier lifetime. Significant effects that appear between 10^{13} nvt and 10^{14} nvt are increased gate current to trigger and, to a lesser degree, increased holding current, on voltage, and forward breakdown voltage.

Although gamma radiation may also produce permanent effects on the SCR, it is expected that failure in the typical radiation environment would result first from fast neutron bombardment. Gamma radiation, however, produces high energy electrons by photoelectric and Compton processes which create a leakage current during irradiation. High pulse levels of irradiation can have the transient effect of triggering the SCR on. At 10^6 R/sec, there is a fifty percent chance that the General Electric C35 SCR will be triggered on.

19.7 EFFECTS OF DERATING

From the above, the most probable failure mechanism is degradation of the blocking capability as a result of either encapsulation flaw (or damage) or internal contaminants. The process can be either chemical or electrochemical, and therefore variable in rate according to the degree of temperature and/or electrical stress applied.

Thus it is possible by means of derating (using the device at stress levels less than the maximum ratings of the device) to retard the process by which the failure of the occasional defective device results. This slowdown of the degradation process results in lower failure rate and increased MTBF. Suppose, for example, that a sample of 778 devices is tested under maximum rated conditions for 1000 hours with one failure observed. The calculated Lambda (λ) is 0.5 (see Table 19.1) and the MTBF is 200,000 hours. If the failed device would have remained within limits at the 1000 hour point because of lower applied stresses, the calculated Lambda becomes 0.3 and the MTBF increased to 333,000 hours.

The relationship of applied stress to General Electric SCR device failure rate is shown graphically in Figures 19.3, 19.4 and 19.5. The model that describes the relationship of these stresses as they relate to failure rate, Lambda (λ), is the Arrhenius Model. The Arrhenius Model is given by:

$$\text{Failure Rate, } \lambda = e^{A} + B/T_j$$

where λ = Failure rate expressed in % Per 1000 hours
T_j = Junction temperature in degrees Kelvin
A and B = Constants

The Arrhenius Model relationship has been successfully applied by the General Electric Company to extensive life test data involving thousands of devices and millions of test hours. The data was obtained from product design evaluations, military lot acceptance testing, and several large scale reliability contracts.

A thorough examination of the data on all General Electric silicon controlled rectifiers revealed that these three graphical presentations could describe the results of derating on failure rate for the entire family of SCR's with reasonable accuracy.

The use of these graphical presentations is quite straightforward. Suppose for example, that it is desired to obtain the estimated failure rate of a C35D under stress conditions of 200 volts peak and a junction temperature of 75°C. The circuit this device will be used in will become inoperative when the electrical characteristics of the SCR change to values outside of the specification limits. This exemplifies a degradation definition of failure and signifies that the solid lines on the

graphical presentations must be used. Since the rated junction temperature of the C35D is 125°C, Figure 19.4 must be used. Projecting a horizontal line from the intersection of the 75°C junction temperature ordinate and the applicable per cent of rated voltage surve (50% in this example) we obtain an estimated failure rate of .08% per 1000 hours at 90% confidence. If, due to a change in the design of the equipment, only devices which failed catastrophically (opens or shorts) would cause the equipment to become inoperable, the dashed curves could be used. This would result in an estimated failure rate of .008% per 1000 hours at 90% confidence.

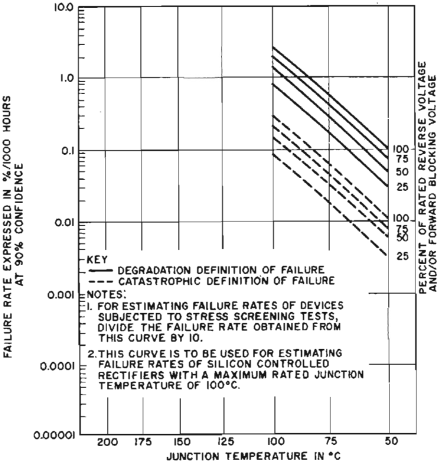


FIGURE 19.3 ESTIMATED FAILURE RATE OF A STANDARD SILICON CONTROLLED RECTIFIER AS A FUNCTION OF JUNCTION TEMPERATURE, REVERSE AND/OR FORWARD VOLTAGE, AND DEFINITION OF FAILURE FOR A MAXIMUM RATED JUNCTION TEMPERATURE OF 100°C

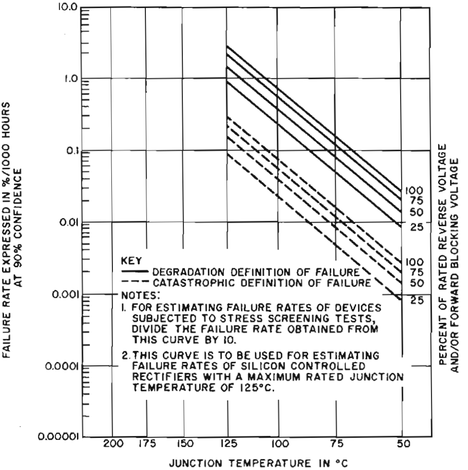


FIGURE 19.4 ESTIMATED FAILURE RATE OF A STANDARD SILICON CONTROLLED RECTIFIER AS A FUNCTION OF JUNCTION TEMPERATURE, REVERSE AND/OR FORWARD VOLTAGE, AND DEFINITION OF FAILURE FOR A MAXIMUM RATED JUNCTION TEMPERATURE OF 125°C

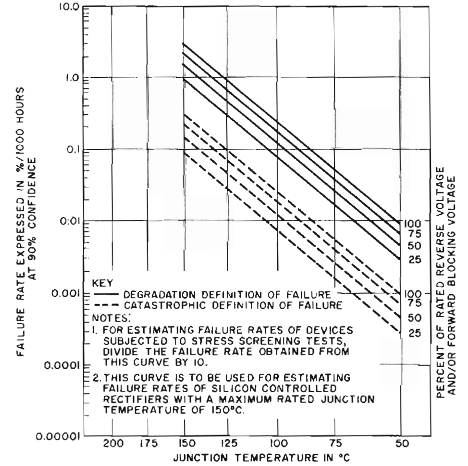


FIGURE 19.5 ESTIMATED FAILURE RATE OF A STANDARD SILICON CONTROLLED RECTIFIER AS A FUNCTION OF JUNCTION TEMPERATURE, REVERSE AND/OR FORWARD VOLTAGE, AND DEFINITION OF FAILURE FOR A MAXIMUM RATED JUNCTION TEMPERATURE OF 150°C

19.8 RELIABILITY SCREENS

An additional failure rate improvement of 10 can be obtained by subjecting the devices to stress screening tests designed to cull out potentially undesirable devices or those likely to exhibit early failure. If the devices in the example of 19.7 had received an appropriate reliability screen, the estimated failure rate would then be reduced to .0008% per 1000 hours at 90% confidence.

Reliability screens have been developed for nearly the whole General Electric SCR family. As technology advances, and more effective procedures are developed, the reliability screens are updated accordingly. Many of these reliability screens are available as published specifications (R1200 series) and devices processed to these specifications are stocked for immediate delivery. An example of one of these reliability screen specifications is shown in Figure 19.6.

Maximum allowable ratings – see General Electric brochure 160.20 dated 11/60.

Electrical characteristics – see General Electric brochure 160.20 dated 11/60.

100% Preconditioning Tests

1. High temperature bake units at 150°C for 168 hours minimum.
2. Temperature cycle per MIL-STD-202C, Method 107B, Test Condition F, except 10 cycles instead of five.
3. Thermal resistance (junction to case) = 2.0°C/w.
4. Blocking burn-in-T_A = 122°C ± 1.5°C, PRV = VBO = 400V, Time = 100 hours minimum.
5. Forward and reverse leakage – T_A = 25°C, PRV = VBO = 400V, $I_R = I_S$ = 2.0 ma maximum.
6. Gate trigger voltage – T_A = 25°C, V_{GT} = 3.0V maximum.
7. Gate trigger current – T_A = 25°C, I_{GT} = 40.0 ma maximum.
8. Forward voltage drop – T_A = 25°C, I_f (Peak) = 50 amps, V_f = 2.0V maximum.
9. Forward and reverse leakage – T_A = 125°C, PRV = VBO = 400V, $I_R = I_S$ = 5.0 ma maximum.
10. Gate trigger voltage – T_A = 125°C, V_{GT} = 1.5V maximum, .25V minimum.
11. Gate trigger current – T_A = 125°C, I_{GT} = 30 ma maximum, .50 ma minimum.
12. Monitored vibration test – "X" or "Z" orientation for 30 seconds minimum. Freq. = 60 cps, double amplitude displacement = ±0.1 inch minimum. Monitor 100V reverse voltage on oscilloscope. Reject for any discontinuity, flutter, drift or shift in trace.
13. Radiflo leak test to 1×10^{-10} cc/sec leak rate.
14. Bubble test – immerse in 90°C ± 5°C deionized water for 60 seconds minimum. Reject any unit which produces more than one bubble from the same point.

FIGURE 19.6 C35DR1200
(SIMILAR TO 2N688)

NOTES

20 TEST CIRCUITS FOR THYRISTORS

20.1 INTRODUCTION

The following circuits can be used for a number of purposes; incoming inspection of thyristor components, trouble shooting circuits in which these devices are used, preventive maintenance, comparison of different types and brands of components, and for obtaining a better understanding of thyristor operation.

In any practical circuit, some adjustment from given component values may be necessary to obtain the specified test condition due to component tolerances, distributed capacitance, inductance and resistance. In general the circuits yield test results which can be correlated with max/min values and curves published on a specific device specification sheet.

For high speed automatic testing many of these circuits are not very practical and entirely different solutions to the test circuit design have to be considered.

The JEDEC Recommended Standards for Testing Thyristors[6] have been used to prepare this chapter. From the large number of tests which can be made on thyristors, the most important have been selected and practical circuits which are in accordance with JEDEC have been shown. JEDEC numbering systems are not referenced because they are subject to change, but most of the described tests in this chapter can be found in JEDEC Part 6 Characteristics Tests.

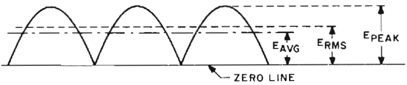
Every test circuit described in this chapter is preceded by a short description of the parameter which it will test, but for more information and better understanding of specific parameters reference to the appropriate chapter in this manual is recommended.

20.2 INSTRUMENTATION

The current waveform into, and the current and voltage waveforms out of a thyristor circuit may be distorted, due either to the nature of the circuit, e.g., a phase control circuit, or to non-linearities in the semiconductor itself, e.g., its logarithmic forward voltage drop-current relationship. The selection of proper instrumentation for use in thyristor evaluation is therefore of prime importance, if accurate measurement is to be made.

Conventional rectifier diodes and SCR's are rated in terms of *average forward current*, average current being defined as that value of unidirectional current indicated by a DC-reading ammeter placed

in series with the diode or SCR. The average value of a waveform should not be confused with its *RMS value*, which is a measure of the heating (I^2R) effect of the waveform in a linear resistance. The ratio of RMS value to average value of any waveform is called its *Form Factor* (F), and F is a function of the ripple content of the wave. For pure (rippleless) DC, F = 1, and F increases as the ripple content increases. Thus, the Form Factor of a full wave rectified sine wave is 1.11, but rises to 1.57 for a half wave rectified sine wave. For SCR's conducting less than 180° the form factor again is different. Section 9.2 gives the relationships between conduction angles and form factor.



FOR FULL WAVE RECITIFIED SINEWAVE

$E_{RMS} = E_{AVG} \cdot 1.11 = E_{PEAK} \cdot 0.707$

$E_{PEAK} = E_{AVG} \cdot 1.57 = E_{RMS} \cdot 1.41$

$E_{AVG} = E_{PEAK} \cdot 0.637 = E_{RMS} \cdot 0.9$

FIGURE 20.1 RELATIONSHIP OF E_{Peak}, E_{RMS} AND E_{AVG} FOR FULL WAVE RECTIFIED SINE WAVE

Triacs, because of their bi-directional nature, are rated in terms of RMS current.

The type of metering used in a particular thyristor circuit will depend on the input voltage to the thyristor. If the input is AC, input voltage should be measured in terms of its RMS value. Note that the commonly available types of "RMS reading" meters (VOM's, most VTVM's) only read RMS correctly when the waveform is a pure undistorted sine wave (rectifier-moving coil instruments actually *measure* average current, but are *calibrated* to read RMS as long as F = 1.11). There are three types of meter that do measure true RMS, independently of waveshape: the iron vane, dynamometer, and thermocouple type instruments. The dynamometer meter is accurate and reasonable in cost, the thermocouple meter is very accurate but delicate, while the iron vane type, although low in cost, has a limited frequency capability. A typical "chopped" sine wave, as produced by SCR phase control, contains a high percentage of harmonics which may be beyond the frequency range of an iron vane meter: The output "DC" voltage and current of an SCR circuit as well as the current through individual SCR's can be measured with conventional moving-coil instruments. RMS load current must be measured by an RMS ammeter. Ripple voltage is best measured with an oscilloscope, or with an RMS voltmeter in series with a capacitor having low impedance to the ripple compared with the voltmeter. Peak-to-peak voltage is normally read directly from an oscilloscope trace, or with a meter designed to read peak-to-peak values (See peak reading voltmeter, Figure 20.5(a)). In almost all test circuits described in this chapter, oscilloscopes are utilized to show more than one parameter simultaneously. Input impedance and frequency response can be important considerations in selecting oscilloscopes for this type of application.

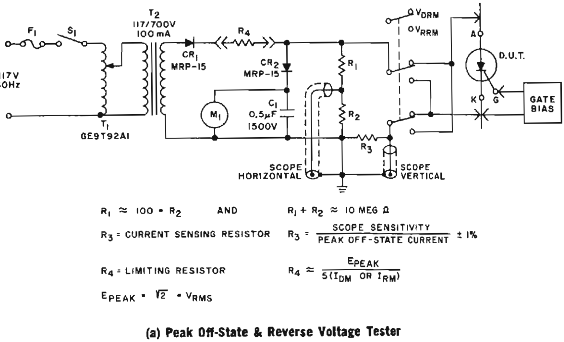
20.3 SPECIFIED PEAK OFF-STATE AND SPECIFIED REVERSE VOLTAGE

Specified Peak Reverse Voltage — V_{RRM}
Peak Reverse Blocking Current — I_{RM}
Specified Peak Off-State Voltage — V_{DRM}
Peak Off-State Current — I_{DM}

20.3.1 Specified Peak Off-State and Specified Reverse Voltage for Thyristors

Peak forward and reverse blocking tests are used to determine the voltage rating of SCR's and triacs. A blocking test is actually a measurement of the voltage withstand capability of the device, as revealed by peak off-state current flowing through it. SCR's and triacs have blocking states in both directions.

A specified peak off-state voltage or specified reverse voltage is applied to the *D*evice *U*nder *T*est (D.U.T.) and the resulting peak current flow through the device is measured. Off-state current and reverse blocking current are quite temperature sensitive and many device types are also sensitive to gate bias. If testing is done at elevated temperature, the device must be mounted on a heat sink of specified size or the test has to be sufficiently short to prevent thermal runaway.



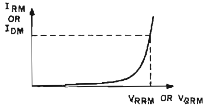
$R_1 \approx 100 \cdot R_2$ AND $R_1 + R_2 \approx 10$ MEG Ω

R_3 = CURRENT SENSING RESISTOR $\quad R_3 = \dfrac{\text{SCOPE SENSITIVITY}}{\text{PEAK OFF-STATE CURRENT}} \pm 1\%$

R_4 = LIMITING RESISTOR $\quad R_4 \approx \dfrac{E_{PEAK}}{5(I_{DM} \text{ OR } I_{RM})}$

$E_{PEAK} = \sqrt{2} \cdot V_{RMS}$

(a) Peak Off-State & Reverse Voltage Tester



(b) Typical Display on Scope for Off-State Voltage Test

FIGURE 20.2 PEAK OFF-STATE & REVERSE VOLTAGE TESTER (LEAKAGE CURRENT LARGER THAN 1ma)

An AC line is connected to the input of a variable auto transformer T_1. This transformer provides a means for adjusting the voltage level which appears across the D.U.T. Transformer T_2 provides line isolation and the voltage step-up ratio necessary to obtain the desired maximum test voltage. Diode CR_1 supplies half wave rectified DC voltage to the D.U.T. A peak reading meter circuit consisting of CR_2, C_1 and M_1 is used to measure the peak value of the voltage applied to the D.U.T. R_4 will limit the current through the device in case of short or breakdown. This resistor should be changed if devices with different I_{RM} and I_{DM} are tested. If I_{RM} or I_{DM} are not limited permanent damage of the D.U.T. may occur. Resistors R_1 and R_2 serve as a load for the supply as well as an attenuator for the horizontal input of the scope. Resistor R_3 senses the peak off-state current flowing through the D.U.T.

Variations of this basic concept are possible to increase the speed and resolution. In Figure 20.2 forward and reverse blocking measurements are made independently. By omitting CR_1, both directions can be measured simultaneously and the following display at the scope will be available.

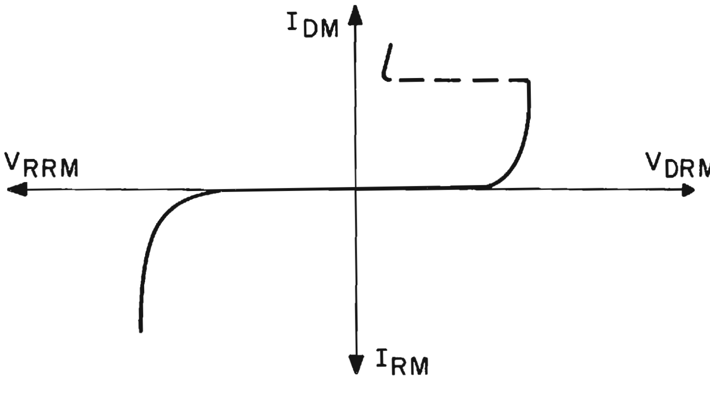
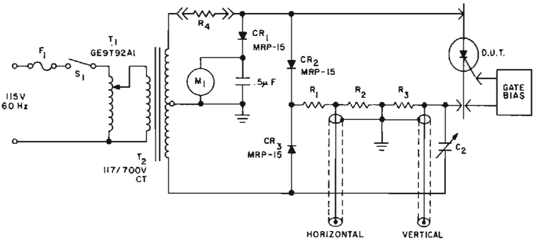


FIGURE 20.3 PEAK OFF-STATE & REVERSE BLOCKING VOLTAGE

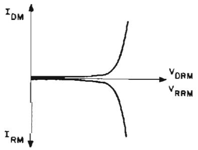
Where it is desired to measure the blocking characteristics of very low current devices, the circuit of Figure 20.4 should be used.

To increase horizontal resolution, forward and reverse blocking voltage is displayed over the whole horizontal distance by adding two diodes to the voltage divider R_1 and R_2.

To cancel the unpleasant affects of circuit and D.U.T. stray capacitance, the circuit is provided with a compensation capacitor C_2 and a 180° out-of-phase voltage source. With this feature, the circuit is eminently suited for making very low peak off-state current measurements.



(a) Peak Off-State & Reverse Voltage Tester



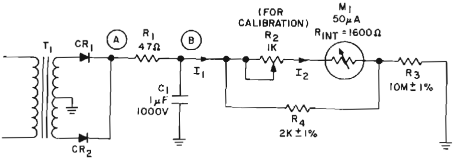
(b) Scope Display of Tester

FIGURE 20.4 PEAK OFF-STATE & REVERSE VOLTAGE TESTER (PEAK OFF-STATE CURRENT BELOW 1ma)

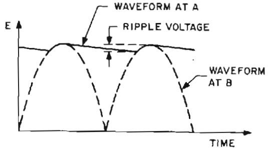
Because the peak voltage can be read very precisely by the peak reading voltmeter, R_2 could be replaced by a potentiometer and adjusted to whatever horizontal deflection is convenient for the operator. The peak reading voltmeter and R_3 could have a range switching arrangement to make the circuit more useful for a wide range of voltages and currents.

20.4 PEAK READING VOLTMETER

Figure 20.5(a) shows a peak reading voltmeter which can be used in the circuit shown in Figures 20.2 and 20.4 for measuring specified peak off-state and specified peak reverse voltage.



(a) Peak Reading Voltmeter



(b) Waveforms at A & B

FIGURE 20.5 PEAK READING VOLTMETER

Voltmeter Range 0-1000 V (E)
Assume $R_M = 10{,}000$ ohm/V, where R_M = meter resistance in ohms/volt $R_3 = R_M \cdot E = 10{,}000 \cdot 1{,}000 = 10$ Megohms

$$I_1 = \frac{E}{R_3} \quad \frac{1{,}000\ \text{V}}{10\ \text{Megohms}} = 100\ \mu\text{a}$$

$$I_2 = \frac{I_1}{2} = \frac{100}{2} = 50\ \mu\text{a (current through meter)}$$

Charging Time Constant $\approx R_1 \cdot C_1 \approx 50 \cdot 1.10^{-6} = 50\ \mu s$
Discharge Time Constant $= R_3 \cdot C_1 = 10 \cdot 10^{-6} = 10$ sec

$$R_M \approx R_3$$

$$E_{ripple} = \frac{T \cdot I_1}{C_1}$$

T = Time between charging pulses
I_1 = Discharge current
C = Capacitance in F

$$E_{ripple} = \frac{(8.3 \times 10^{-3}) \cdot (100 \times 10^{-6})}{1 \times 10^{-6}} = 0.83\ \text{V}$$

This small amount of ripple voltage would result in a very small measurement error.

20.5 DC-GATE TRIGGER CURRENT AND VOLTAGE TEST

I_{GT} = Gate Current to Trigger
V_{GT} = Gate Voltage to Trigger

Test Description

This test is used to measure the magnitude of the DC gate current and voltage signals required to trigger a thyristor or triac from the off-state to the on-state. The gate current actually performs the triggering function and the gate trigger voltage represents the drive required to achieve the triggering current.

Forward blocking voltage is applied as specified, and the gate signal voltage is slowly increased in magnitude until the SCR switches from the blocking to the on-state. Since many SCR's and triacs exhibit a change in gate impedance when they switch on, the correct test procedure is to record the highest gate voltage and current readings attained *prior* to switching even though they may not occur simultaneously.

The applied forward blocking voltage may be DC, half or fullwave DC, or trapezoidal waves of any convenient duty cycle, as long as the on-time is at least 1ms and the dv/dt of the applied anode voltage is small enough ($\approx$ 0.01 V/μs) to perform a valid gate test (so as not to assist gate triggering with dv/dt triggering).

Other important considerations are temperature, load circuit conditions and the impedance of the triggering circuit. Sufficient resistance in series with the gate voltage supply is required to ensure that the test device (especially low current devices) will not turn back off subsequent to triggering because of a gate impedance change at the instant of turn-on. (See also Chapter 4.)

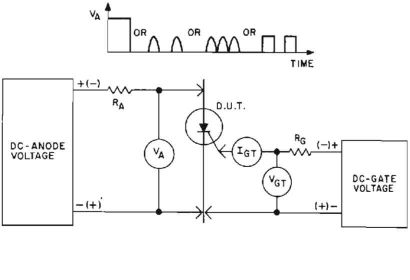


FIGURE 20.6 BLOCK DIAGRAM OF GATE TEST

20.5.1 Anode Supply For Gate Test

The blocking voltage waveform applied to the D.U.T. in the circuit of Figure 20.7 consists of a clipped half sine wave of peak magnitude of 6 or 12 volts, depending on the setting of S_2. The correct setting of S_2 is determined from the specification sheet of the thyristor under test, as is the value of the anode load resistor R_S.

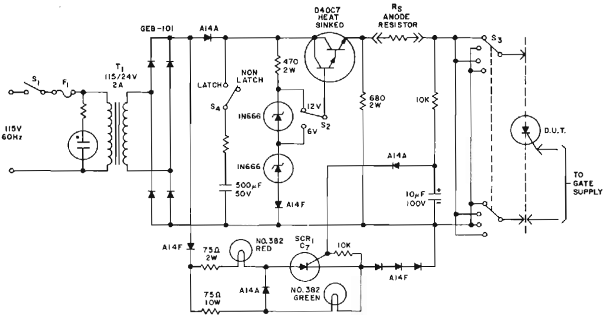


FIGURE 20.7 ANODE SUPPLY PLUS DETECTION CIRCUIT FOR GATE TEST

A detection for turn-on is also incorporated in this circuit. As long as the voltage between anode and cathode of the D.U.T. is high, SCR_1 will be turned on and the red light will be lit. As soon as the D.U.T. turns on, causing the voltage between anode and cathode to decrease below $\approx$ 3.5 volts, SCR_1 will be turned off and the green light will light. This detection circuit could be replaced by a voltmeter.

S_4 allows the circuit to test for latching capability. When S_4 is closed, the anode voltage on the device under test is changed from full wave DC to filtered DC. When a gate test is performed, the gate signal should be removed after the device has turned on and it should stay turned on.

20.5.2 DC Gate Supply For Gate Test

The gate signal can be applied as a pulse or DC. If a pulse gate trigger signal 100 μs or wider, is used measured values of current and voltage will be the same as for pure DC.

Figure 20.8 shows a gate trigger circuit where the DC gate voltage and current can be continuously adjusted and conveniently read on the appropriate meter. The gate impedance is kept constant at 100 ohms, but can be increased by inserting different values for R_X to comply to manufacturer's specifications. This gate supply is designed to work together with the anode supply in Figure 20.7. By using S_3 as shown, triacs can be tested in all four quadrants, but if SCR's only are to be tested, S_3 could be omitted.

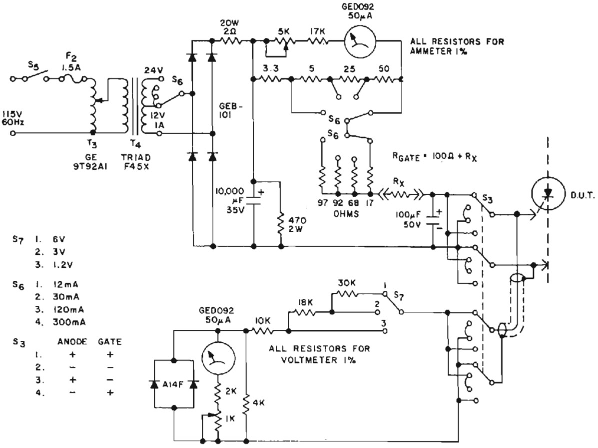


FIGURE 20.8 DC GATE SUPPLY 0-6 V, 0-300 ma

20.5.3 Pulse Gate Supply For Gate Test

Figure 20.9 shows a supply which could be used to apply square wave pulses to the D.U.T., whose magnitude can be varied from zero to 6 volts and whose pulse width is adjustable from about 5 μseconds to more than 100 μseconds. Gate voltage can be switched either positive or negative for testing triacs. Instrumentation consists of a gate current "looking" resistor R_4, an oscilloscope with separate vertical and horizontal amplification.

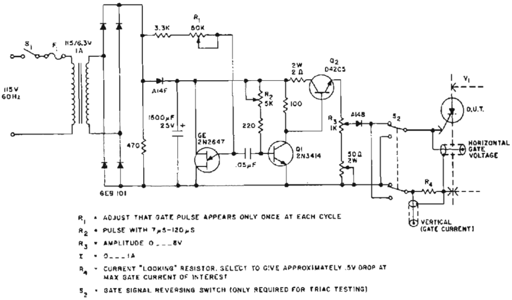


FIGURE 20.9 PULSE GATE SUPPLY (SCR & TRIACS)

Test procedure is as follows: R_1 is adjusted so that a gate pulse occurs only *once* during each half cycle of applied anode blocking voltage and the pulse should be timed (by R_1) to occur approximately 4 milliseconds after the start of the half cycle. R_2 is then adjusted to give the desired width of pulse. Note that gate pulse widths in excess of 100 μseconds result in measured values of trigger voltage and current that are equivalent to continuous DC measurements. With R_3 set initially for zero volts output, the applied gate voltage is gradually increased (via R_3) until the test thyristor triggers. Because the gate impedance may change when triggering occurs, the readings of gate voltage and current must be made just prior to triggering. Triggering is indicated by a sudden drop in the reading of V_1, or by a sudden step in the gate E-I trace observed on the oscilloscope.

In Figure 20.9 the vertical input of the scope is connected to R_4 and the horizontal input to the gate which connects the D.U.T. cathode to common. For small currents this can generate a problem because the circuit is floating above ground by the resistor R_4.

Figure 20.10 shows another arrangement, where a differential amplifier input is utilized, eliminating the problems created by noise when small gate currents have to be measured.

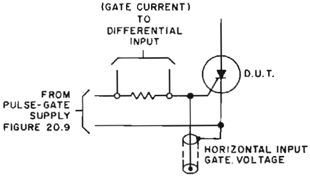


FIGURE 20.10 SCOPE CONNECTION FOR SMALL GATE CURRENT MEASUREMENTS TO ELIMINATE NOISE PROBLEMS

20.5.4 Gate Trigger Test Set for Low Current SCR's (Less Than 2 Amperes Current Rating)

The measurement of low current SCR triggering voltage and current is complicated by the fact that the gate impedance changes *drastically* when the test device switches on. In addition, the gate trigger voltage and current values are dependent on the source impedance of the test set, and the source impedance must therefore be specified when making tests. The circuit of Figure 20.11 is designed specifically for testing all present G-E low current SCR's. In this circuit a variable half sine wave of voltage is applied to the gate (from a controlled impedance source) and the gate E-I characteristic is monitored with an oscilloscope. The triggering point is detected by the sudden change in gate impedance that occurs when the device switches on.

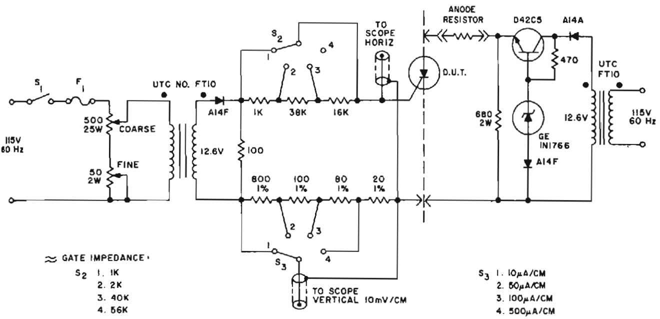


FIGURE 20.11 GATE TRIGGER TESTER FOR LOW CURRENT SCR's

Figure 20.12 shows a typical scope presentation of a gate E-I characteristic during the gate trigger current and trigger voltage test. The trace is shown dotted beyond the triggering point. In the actual case, the trace suddenly jumps at the triggering point due to the change in gate impedance. The portion of the trace beyond the triggering point becomes somewhat reduced in intensity.

The gate trigger voltage is that value of voltage which will just cause the device to switch to the on-state. As shown in Figure 20.12(a) it is read just prior to the switching point. Unlike trigger voltage, the gate trigger current value must be read at the point where it is a maximum, although this is not necessarily the actual triggering point. It must be kept in mind that in order to reach the actual triggering point, the trace must first pass through this maximum, and the firing circuit design must take this into account.

Many low current SCR's exhibit triggering with a negative value of gate current. Figure 20.12(b) shows a typical gate E-I trace for this type of device. Note that the gate trigger voltage is always positive. On this type of unit only the gate trigger voltage is of interest. A negative gate trigger current is meaningless to the circuit designer, and it is not necessary to measure it.

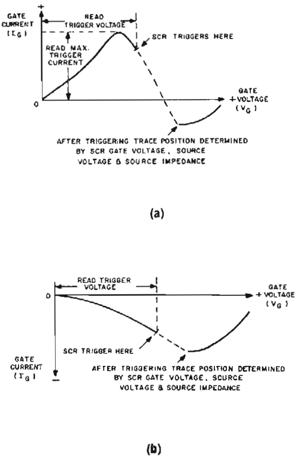


FIGURE 20.12 GATE TRIGGER MEASUREMENT POINTS FOR LOW CURRENT SCR's

If a low gate current measurements have to be made, noise can also be troublesome in this circuit and the same recommendation as for Figure 20.9 could be applied to improve circuit performance.

20.6 DC HOLDING CURRENT TEST

I_H — Holding Current

Test Description

This test is used to determine the minimum on-state current that will just sustain device conduction *following operation* at normal conduction (on-state) current levels.

It is performed by turning the device on and establishing a specified on-state current for an instant (100 μs — 10 ms) and then reducing the current until the device switches from the on-state to the off-state. The lowest on-state current thus attained is the holding current.

The initial on-state current level should be high enough to insure that the device is fully turned on and of short enough duration to insure that self-heating is negligible.

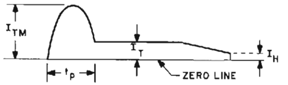


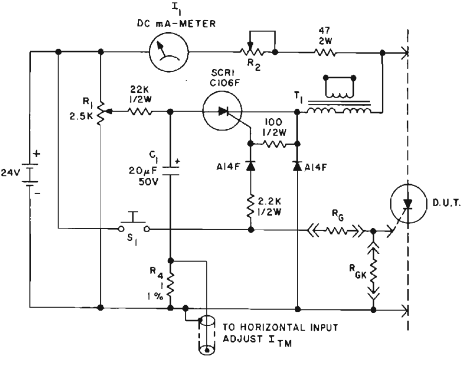
FIGURE 20.13 WAVEFORM USED FOR MEASURING HOLDING CURRENT

A fixed DC supply voltage is used and the test current is controlled by a variable resistance, but to insure proper turn-on the DC current is preceded by a half-sinusoidal current pulse.

The temperature of the D.U.T, and gate bias condition affect holding current and therefore must be specified. The gate trigger signal used to turn the test device on initially can be of any sufficient magnitude to turn the device on, but must be removed, before the actual measurement of the holding current is made.

Test Circuit

A circuit to measure holding current is shown in Figure 20.14.



I1 500 mA DC MOVEMENT
R2 10K POTENTIOMETER (OR 50K FOR LOW CURRENT SCR'S)
RG TO SUIT D.U.T.
RGK AS REQUIRED IN SPECIFICATION
T1 UTC NO. F10, OR EQUIVALENT. CONNECT SECONDARY IN SERIES AND SHORT PRIMARY WINDING

FIGURE 20.14 HOLDING CURRENT TESTER

For each time S_1 is depressed to trigger the test thyristor, SCR_1 also is triggered and SCR_1 sums an additional pulse of current through the test thyristor as it turns on. The magnitude of this initial current pulse is determined by the setting of R_1 and is specified for each thyris-

tor type. Its value is monitored by the 1 ohm "looking" resistor R_4. Pulse width is fixed by C_1 and T_1 and is satisfactory for most presently available G-E devices. To measure the holding current of a particular thyristor, S_1 is depressed to trigger the test device and then released. R_2 is then increased in value until I_1 drops suddenly zero. The reading on I_1 just prior to this point is the holding current of the test thyristor.

20.7 LATCHING CURRENT TEST

I_L = Latching Current

Test Description

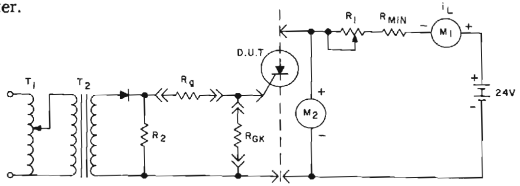
This test is used to determine the minimum on-state current, which will maintain the device in the on-state subsequent to the triggering signal removal.

It is performed by applying a specified gate pulse at a low repetition rate and then decreasing the circuit resistance until the on-state current will remain flowing following the removal of the gate signal. D.U.T. temperature, gate trigger signal and gate bias between trigger pulses, all affect the latching current level and therefore all three must be specified.

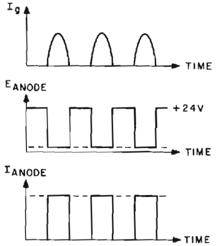
Circuit inductance must be low so that the rise time of the on-state current is short compared with the gate trigger pulse width.

Test Circuit

The circuit of Figure 20.15(a) shows a simple latching current tester.



(a) Circuit



(b) Waveforms on D.U.T. Solid lines show waveforms prior to latching; Dotted lines, after latching

FIGURE 20.15 LATCHING CURRENT TESTER

The gate signal is supplied from a half wave source, which drives the gate positive for one-half of the AC cycle. This gate signal can be adjusted to exceed the critical gate current to trigger limits for the device being tested. During the period of time when the gate is positive, the D.U.T. anode voltage will go near zero voltage regardless of the setting of R_1.

In using the circuit (Figure 20.15) R_1 is initially set to maximum resistance. This resistance must be high enough to permit the anode current to fall below the latching current level. Meter M_2 will read about 12 volts, as the D.U.T. is only conducting during the periods of positive gate signal (half cycle). Potentiometer R_1 is now gradually reduced in value, until meter M_2 suddenly drops to about 1 volt. This condition indicates that the D.U.T. is now conducting 100% of the time and the latching current value can be read from M_1.

20.8 PEAK ON-STATE VOLTAGE TEST CIRCUIT

V_{TM} = On-State Voltage

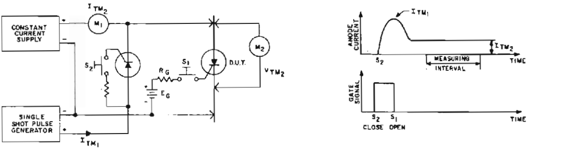
On-state voltage (formerly called the forward voltage drop in the conducting state) of a thyristor is an extremely important parameter in establishing the current vs temperature rating of a device.

Measurements of on-state voltage are usually made at two current levels.

20.8.1 On-State Voltage (Low Level) (25° C)

The low level test is made in that region of the on-state characteristic where the voltage drop is primarily determined by the effects of the junction only and as predicted by theory, generally follows a logarithmic relationship with the current.

Since thyristors may exhibit more than one state of conduction, it is necessary to establish the lowest conducting state, (lowest on-state voltage) by means of a current pulse prior to voltage measurement. A block diagram of a typical low-level on-state voltage tester is shown in Figure 20.16(a).



(a) Block Diagram On-State Voltage (low level) **(b) Waveform of Anode Current and Gate Signal**

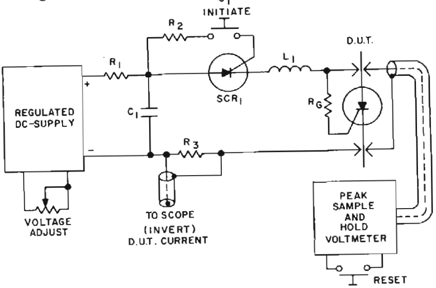
FIGURE 20.16 LOW LEVEL ON-STATE VOLTAGE TESTER

Operating sequence is as follows. Adjust constant current on pulse generator to desired current. Close S_1, close S_2, read voltage V_{TM2} on M_2.

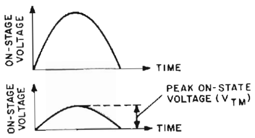
20.8.2 On-State Voltage (High Level)

The high level on-state voltage test is made in the region of the forward characteristic where the voltage drop is primarily determined by the effects of resistance of the device, including those caused by the pellet, back-up plates, solder joints, tubulation joints, terminals, etc.

To prevent excessive junction heating, a single pulse of current is used which is approximately half sine wave in shape with a specified amplitude and base width. In order to eliminate errors caused by the effect of resistance in the power supply leads, the on-state voltage measurement is made employing a four point connection. The on-state voltage measurement is made at the peak of the voltage waveform by a peak storage voltmeter.



(a) Block Diagram On-State Voltage Test (High Level)



(b) Waveform of Anode Current and On-State Voltage

FIGURE 20.17 HIGH LEVEL ON-STATE VOLTAGE TEST

Figure 20.17(a) shows a block diagram of a circuit where the high current pulse is generated by discharging a capacitor through an inductor. Operation of this circuit is as follows: A regulated dc voltage source is used to charge capacitor C_1 to a specified voltage level. When the initiate button is depressed, capacitor C_1 will discharge through SCR_1, L_1, D.U.T. and R_3. The discharge current waveform will be a half-sine wave, with the base width determined by the following formula:

$$T = \frac{1}{2 \cdot F} \qquad \begin{array}{l} T = \text{time is seconds} \\ F = \text{resonant frequency of } C_1 \text{ \& } L_1 \text{ in Hz} \end{array}$$

The resonant frequency is:

$$F = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}} \qquad \begin{array}{l} F \text{ in Hz} \\ L \text{ in Henries} \\ C \text{ in Farads} \end{array}$$

The peak current:

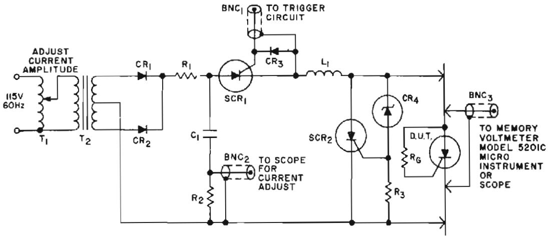
$$I_{Peak} = \frac{E_{C1}}{Z} \qquad \begin{array}{l} I_{Peak} \text{ in Amps} \\ E_{C1} \text{ volt on } C_1 \text{ in Volts} \\ Z \text{ impedance of discharge path at resonant} \\ \text{frequency in ohms} \end{array}$$

Z should be $<< V_{TM}/I_p$ or the waveform will not be sinusoidal. The peak voltage which appears at D.U.T. will be measured at peak reading storage voltmeter.

At the end of the forward current pulse the current, due to resonance attempts to reverse (the circuit being oscillatory). SCR_1 will prevent this, but the resultant reversal of the voltage across SCR_1 does insure its turn-off ($t_q < T$).

Capacitor C_1 will now slowly recharge through resistor R_1. The gate signal to fire the D.U.T. is derived from the anode voltage source. An independent gate signal is sometimes used instead where synchronization of this signal is important. SCR_2 is in the circuit only to protect the operator from high voltages which may appear on the test terminals. This could occur if SCR_1 is fired, but no D.U.T. is connected, or if D.U.T. fails to fire.

Figure 20.18 shows an actual circuit to generate pulses between 0-125A with a base width of 1 ms.



T_1	VARIABLE TRANSFORMER GE 9T92A1 (2.5 - 3.5A 0__120__140V)
T_2	STANCOR PC-8301 STANCOR PC-8301 (830V CT 200 mA)
CR_{1-2}	DIODE GE MPR 15
R_1	5K, 10W
C_1	90μF OIL-CAPACITOR GE 4 x 20μF NO. 960 1 x 10μF NO. 959
R_2	.2 OHM 1%, 5W
SCR_{1-2}	THYRISTOR GE C35N
CR_3	DIODE A14F
L_1	1.11 mH INDUCTOR MILLER 3 x .37 mH NO. 7827
CR_4	ZENER DIODE ≈ 40V 1W
R_3	RESISTOR 220Ω, 2W
R_G	RESISTOR DEPENDS ON D.U.T.

FIGURE 20.18 ON-VOLTAGE TESTER

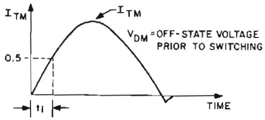
20.9 CRITICAL RATE OF RISE OF ON-STATE CURRENT TEST (DI/DT) (See JEDEC Rating Establishment and Verification Tests — Part 5)

When thyristors are switched by a gate signal from the off-state into a high on-state current, they tend to begin conducting in a limited area physically near the gate contact. (This, of course, depends on the type of gate construction employed.) This conducting area then spreads with time until the entire area of the device is conducting. If the off-state voltage is high and the on-state current rises rapidly, it is possible to dissipate a peak power of many kilowatts in a very small area, during the switching interval. This causes very high spot temperatures with resulting high switching loss. Ultimate failure by spot melting through the junction can occur in the extreme.

The di/dt test is a measure of the ability of the thyristor to withstand switching from high off-state voltages into fast rising load currents. The gate signal used is normally high in amplitude with a fast rising leading edge, to make the initial conducting spot as large as possible. Both the amplitude and rise time of the gate signal are important.

Two different non-repetitive ratings may be assigned to thyristors, one for gate triggering (which is described and most commonly used) and one for triggering by exceeding the thyristor breakover voltage.

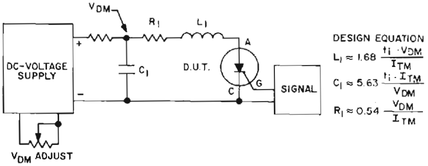
Current waveform and numerical value of di/dt are shown in Figure 20.19(a) and (b).



(a) di/dt Test Current Waveshape

$$\frac{di}{dt} = 0.5\,\frac{I_{TM}}{t_i}$$

(b) Numerical Value of di/dt



(c) Circuit for di/dt Test

FIGURE 20.19 di/dt TEST

In the circuit shown in Figure 20.19, the di/dt stress is applied, using the D.U.T. to discharge a capacitor C_1 through a series resistor R_1 and inductor L_1 to produce a damped sinusoidal current pulse.

Reverse switching transients should be suppressed as this method is intended to be a test of on-state switching capability only. R should

be one-half of the critical damping resistance in order to avoid destroying the thyristor due to reverse recovery energy after the on-state current pulse.

In the di/dt test the time, t_1, should be 1 μsecond minimum and the pulse repetition rate for establishing the repetitive rating for both unidirectional and bidirectional thyristors should be 60 p/s as recommended by JEDEC.

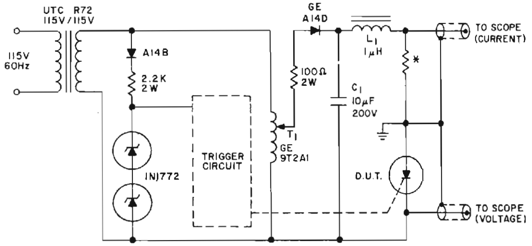
The gate trigger pulse when applicable should be specified as to pulse width, t_w, rise time, t_r, and gate source voltage and resistance. Suitable circuits for generating these pulses are described in Chapter 4 and are also shown in Figure 20.21.

20.10 TURN-ON VOLTAGE TEST

"Di/dt test" and "turn-on voltage" test can be performed with similar test circuit and should be considered together, because both gauge the ability of an SCR to switch high current loads satisfactorily.

Figure 20.20 shows a circuit which can be used to perform a turn-on voltage test, and differs from the on-voltage test only in the pulse width, which is only 10 μseconds.

By measuring the forward current and voltage simultaneously as shown in Figure 20.20(b) and (c), switching losses can be calculated.

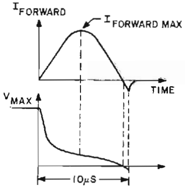


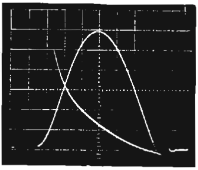
* THE CURRENT COOLING SHOULD BE A LOW INDUCTIVE TYPE SHUNT, AS MANUFACTURED BY AEG-TELEFUNFEN, OR COULD BE BUILT BY PARALLELING A LARGE NUMBER OF 2W CARBON TYPE RESISTORS.

(a) Turn-On Voltage Test

(b) Current Waveform

(c) Voltage Waveform





(d) Actual Measurement of Turn-on Voltage

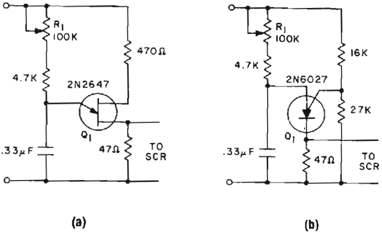
FIGURE 20.20 TURN-ON VOLTAGE TESTER

When an SCR is gate triggered, it turns on initially only in the region nearest the gate contact, and the turned-on portion then spreads laterally to encompass the entire pellet area. Until the whole pellet is in conduction, any load current through the SCR concentrates in the turned-on portion, effectively limiting the maximum current-carrying ability of the SCR for the first microsecond or so after triggering. Since the on-state voltage drop of an SCR is proportional to current density, it is possible to compare the switching characteristics of a group of devices by measuring their individual on-state voltage drops at a standard current level and time interval subsequent to triggering. In the two trigger circuits as shown in Figure 20.21 the Q_1 oscillator frequency is set by means of R_1 so that the test SCR triggers sometime after the peak of the 60 Hertz input sine wave. Transformer T_1 is then adjusted until the peak magnitude of the 10 microsecond wide half sine wave resonant discharge current pulse that ensues is 150 amperes, as measured by the current probe and oscilloscope. By taking measurements at the peak of the current pulse, voltage errors due to stray inductance in the circuit are eliminated. The SCR on-state voltage drop at the 150 ampere standard current is an indirect measure of its di/dt capability. Care is needed in the connections of the voltage and current probes to avoid errors due to stray pickup from ground loops.

Because switching losses may be reduced by using fast rising gate signals, a programmable unijunction transistor trigger circuit is shown which would generate pulses with a rise time of $\approx$50 ns. Because switching losses may increase with slow rising gate signals, it is prudent where possible to test switching losses with the trigger signal that will be used in the application.

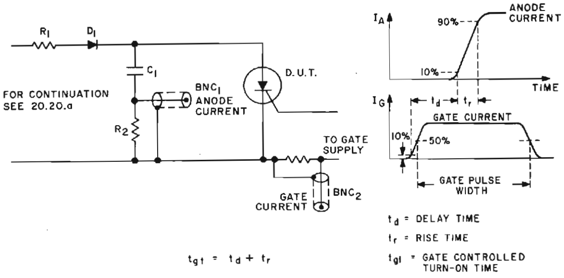
20.10.1 Gate Controlled Turn-On Time

This test method applies to all triode thyristors and for either polarity of applied voltage in the case of bidirectional devices. The circuit is similar to the circuit measuring turn-on voltage shown in Figure 20.20 except that no inductance is in the discharge path of C. Turn-on time should only be truly limited by the D.U.T.



TRIGGER CIRCUITS FOR di/dt TEST AND TURN-ON VOLTAGE TEST

FIGURE 20.21



(c) (d)

TEST CIRCUIT AND WAVEFORMS FOR MEASURING TURN-ON TIME

FIGURE 20.21

The delay time is the interval between the 10% point on the leading edge of the gate trigger pulse and the time when the resulting on-state current reaches 10% of its maximum value.

The rise time is the time interval during which the on-state current increases from 10% to 90% of its maximum value. The sum of delay time and rise time is the turn-on time (t_{gt}).

An alternate method to observe delay and rise times is to observe the voltage across the D.U.T.

The following criterion should be used in selecting the component values in the test circuit:

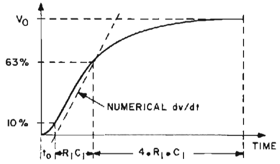
1. The rise time of the gate trigger pulse should not exceed 10% of the specified delay time.
2. The product of R_2 and C_1 should be equal or greater than ten times the specified rise time, but less than 25-30 times to minimize self heating.
3. When on-current waveform is observed, the inductance of the capacitor discharge loop including all its components should be equal to, or less than, 0.1 times the product of R_2 and the specified rise time.
4. R_1 is a surge limiting resistor to protect D_1.

20.11 DV/DT TEST — CRITICAL RATE OF RISE OF OFF-STATE VOLTAGE TEST

The off-state blocking capability of any thyristor is sensitive to the rate at which the off-state voltage is applied. If the rate of rise exceeds a critical value, breakover voltage will decrease below the static value, causing switching from the off-state to the on-state. These tests cover the cases where the device is initially unenergized and then subjected to a linearly or exponentially rising off-state voltage.

20.11.1 Exponential dv/dt Test

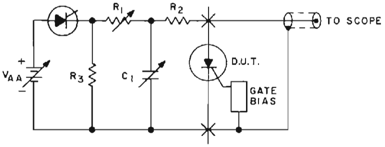
This test is performed with an exponential waveform of specified amplitude with the D.U.T. initially unenergized. The rate is increased until the device breaks over. The rate-of-rise at breakover is the critical value. Because the exponential method produces a changing rate of rise we require an arbitrary definition of numerical value. The numerical value of this rate-of-rise is calculated as shown in Figure 20.22(b).



(a) dv/dt Test Voltage Waveform (Exponential)

$$\frac{dv}{dt\,(EXP)} = 0.63\,\frac{V_0}{R_1 \cdot C_1}$$

(b) Numerical Value of dv/dt (Exponential)



S_1 = MERCURY WETTED REED RELAY OR SCR
R_1 = NONINDUCTIVE
R_2 = CURRENT LIMITING RESISTOR

(c) Circuit For Exponential dv/dt Test

FIGURE 20.22 dv/dt TEST (EXPONENTIAL)

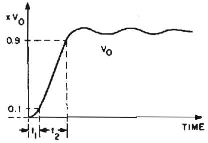
Where this parameter appears on the device specification sheet, it enables the circuit designer to design filters to prevent false triggering. Figure 20.22(c) illustrates a simple circuit to check the dv/dt capabilities of thyristor devices.

The operation of the circuit is straightforward, but a few rules have to be observed to obtain good results. The switch S_1 can be a mercury wetted relay or SCR, but its closure time (including bounce) must be less than $0.1 \cdot R_1 \cdot C_1$. Resistor R_2 is used to limit current in the event of breakover. The values of R_1, R_2 and C_1 must be selected to minimize waveform distortion due to thyristor and circuit wiring impedance. The rate of dv/dt is increased by lowering C_1 or R_1. R_3 will discharge C_1 after S_1 is opened.

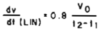
20.11.2 Linear dv/dt Test

This test is performed with a linear waveform of specified ampli-

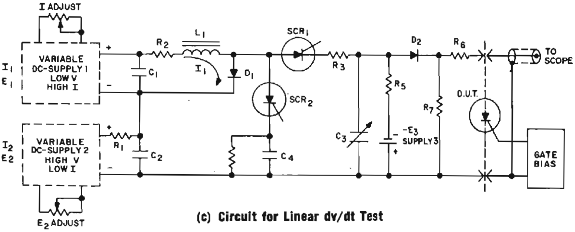
tude with the device initially unenergized. The rate is increased until the thyristor breaks over. The rate of rise at the breakover is the critical value. The test voltage waveform and numerical value of the critical rate of rise are shown in Figure 20.23



(a) dv/dt Test Voltage Waveform (Linear)



(b) Numerical Value of dv/dt (Linear)



(c) Circuit for Linear dv/dt Test

FIGURE 20.23 dv/dt TEST (LINEAR)

Figure 20.23(c) shows a basic circuit to generate a linear ramp. Initially the low voltage, high current supply is circulating a current I_1 in the loop R_2, L_1 and D_1 whose amplitude depends on the Supply 1 adjustment. Supply 3 will charge C_3 to a negative voltage through the high impedance of R_5. After I_1 has stabilized and C_3 is charged to a negative voltage, SCR_1 can be fired and constant current can flow through R_3 into C_3.

The voltage on C_3 will rise in a linear fashion from $-E_3$ to $+E_2$. The D.U.T. does not see the linear ramp until D_2 becomes forward biased, i.e., at about 2 volts above ground. The slope of the ramp can be varied by adjusting the magnitude of the constant current and/or adjusting the capacitance of C_3. The voltage amplitude to which this ramp rises is determined by E_2, where $E_1 << E_2$ and E_2 is programmable. The voltage waveform can be observed with a scope across the D.U.T.

Slow turn-on of SCR_1 and slow reverse recovery of D_1 can cause non-linearities in the lower part of the voltage waveform, which is eliminated by R_5 and D_2. The reverse voltage on D.U.T. when SCR_1 is off should not be above $0.02 \cdot (E_1 + E_2)$.

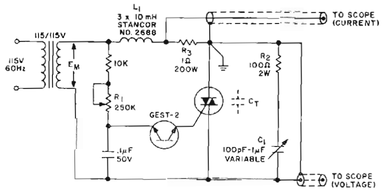
SCR_1 should be on for a minimum of 50 μseconds, R_6 is required to prevent damage to the D.U.T., but should be as small as possible to minimize waveform distortion. SCR_2 assures turn-off of SCR_1 in case the D.U.T. turns on. Lead inductance and length in the loop containing SCR_1, R_3, C_3, D_2 and R_6 should be kept to a minimum.

20.12 CRITICAL RATE OF RISE OF COMMUTATING OFF-STATE VOLTAGE FOR BIDIRECTIONAL THYRISTORS (TRIACS) TEST

The bidirectional thyristor, in its usual mode of operation, is required to switch to the opposite off-state polarity following current conduction in the on-state. In common 50, 60 and 400 Hz AC phase control applications utilizing sinusoidal voltage sources, this switching occurs each half cycle at the current zero point.

As long as voltage and current are in phase, the reapplied voltage rises relatively slowly, but operation of a triac into an inductive load requires additional design constraints that must be considered for during circuit design. The most serious of these constraints is commutation dv/dt. It is largely influenced from the last ⅓ of the decreasing current di/dt (for more details see Chapter 7).

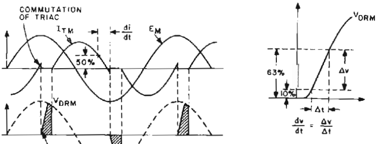
Commutation dv/dt is that rate of rise of voltage impressed across the triac by a circuit at the cessation of current flow. In an inductive AC circuit current lags voltage by a phase angle θ and as a result current goes through zero sometime after the supply voltage has reached a finite value in the opposite direction. Since the triac tries to turn off at zero current, the instantaneous line voltage at that point appears suddenly across the device at a rate limited only by circuit stray capacitance and the capacitance of the triac itself (C_T). For the triac to turn off reliably in an inductive circuit, the rate of voltage rise across the device must be kept within specified limits, and the test circuit of Figure 20.24 is intended to check this dv/dt withstand ability. In this circuit, the rate of rise of voltage across the triac is made adjustable (from 10 volts per microsecond down to less than 0.3 volts per μsecond) by deliberately adding capacitance C_1 in shunt with the test device. Resistor R_2 prevents high peak current from flowing through the triac when it turns on and discharges C_1.



(a) Commutating dv/dt Test For Triacs

(b) Supply Voltage & Load Current

(c) Rate of Rise of Voltage After Triac Commutates



(d) Expansion of Commutating dv/dt

FIGURE 20.24 COMMUTATING dv/dt TEST FOR TRIACS

Design Equation

The circuit shown in Figure 20.24 can be used to test a triac with a current rating of $I_{RMS} = 10$ amps — see Table 20.1.

$$di/dt = 6.28 \cdot f \cdot I_{TM} \cdot 10^{-3} \qquad (A/ms)$$
$$= \omega \cdot I_{RMS} \cdot \sqrt{2} = 6.28 \cdot 60 \cdot 10 \cdot 1.41 = 5.3\ A/ms$$

$$Z_L = \frac{E_M}{I_{TM}} = \frac{115 \cdot \sqrt{2}}{10 \cdot \sqrt{2}} = 11.5\ \Omega$$

$$Z_L = \sqrt{X_L^2 + R^2}$$

Choke selected as 30 mH

$$X_L = \omega \cdot L = 2 \cdot 3.14 \cdot 60 \cdot 30 \cdot 10^{-3} = 11.31\ \Omega$$

Recommended: $\frac{X_L}{R_3} \geqq 10 \qquad R_3 = 1\ \Omega$

An on-state current duration of 90% of a half cycle is recommended, which means that heat sinking is required.

Testing Procedure

Testing procedure is as follows: Set C_1 initially to 1 μf and R_1 to maximum resistance. With power applied adjust R_1 to obtain 90% on-time and 10% off-time.

If scope is connected as shown in Figure 20.24(a), you should see the current and voltage as shown in Figures 20.24(b) and (c). (Voltage is 180° inverted.)

If testing has to be done at elevated temperature provision for external heating and monitoring of case temperature (junction temperature) has to be provided. C_1 is then progressively reduced until the desired rate of voltage rise across the triac is reached or failure to commutate results as monitored by the test scope.

Numerical rate of voltage rise is defined by the waveforms of Figure 20.24(d).

Type	I Rating	di/dt 50 Hz	di/dt 60 Hz	di/dt 400 Hz	Z_L in Ohms
SC35/SC36	3	1.33	1.6		38.4
SC40/SC41 SC240/241	6	2.66	3.2	21.5	19.2
SC45/SC46 SC245/246	10	4.5	5.4	36	11.5
SC50/SC51 SC250/251	15	6.66	8	54	7.7
SC60/SC61	25	11.2	13.5	89	4.6
SC141	6	2.66	3.2		
SC146	10	4.5	5.4		

TABLE 20.1 di/dt VALUES FOR MOST COMMONLY USED TRIACS FOR 50, 60 AND 400 Hz

20.13 TURN-OFF TIME TEST

As discussed in Chapter 5, the turn-off time depends on a number of circuit parameters. Thus, a turn-off time specification inherently

must include the precise value of these circuit parameters to be meaningful. Accordingly, specifications for General Electric SCR's with guaranteed turn-off limits list the applicable circuit parameters and show the test circuit which will apply these parameters to the SCR. For this information, the reader is referred to the specification bulletin for the SCR under consideration.

For general turn-off time test work, the type of circuit shown in Figure 20.25 can be used for low, medium, and high current SCR's by proper manipualtion of the circuit constants. Forward load current is adjustbale by R_5 from approximately ½ ampere to 70 amperes and the length of time SCR_1 is reverse biased during the turn-off cycle can be adjusted by manipulating R_5 and C_1. The peak reverse current during the recovery period can be adjusted by R_7 and this current can be viewed on a scope by monitoring the voltage across a non-inductive shunt R_8. If one is interested in only one particular load current range, there is of course no necessity in providing the complete range of resistors and capacitors specified in Figure 20.25.

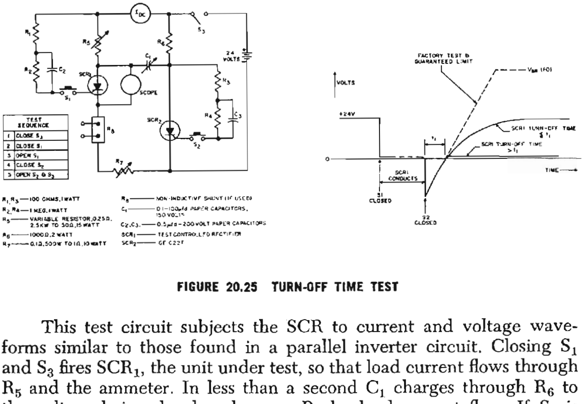


FIGURE 20.25 TURN-OFF TIME TEST

This test circuit subjects the SCR to current and voltage waveforms similar to those found in a parallel inverter circuit. Closing S_1 and S_3 fires SCR_1, the unit under test, so that load current flows through R_5 and the ammeter. In less than a second C_1 charges through R_6 to the voltage being developed across R_5 by load current flow. If S_2 is now closed, SCR_2 turns on. This applies C_1 across SCR_1 so that the current through SCR_1 is reversed. C_1 furnishes a short pulse of reverse recovery current through SCR_1 until this SCR recovers its reverse blocking ability. After this initial pulse of current, C_1 continues its discharge through SCR_2, the battery, and R_5 at the rate dependent on the time constant of R_5C_1. After a time interval, t_1, in Figure 18.7, somewhat less than the R_5C_1 time constant, the anode to cathode voltage of SCR_1 passes through zero and starts building up in the forward direction. If the turn-off time, t_{off}, of the SCR is less than t_1, it will remain turned off and the ammeter reading will return to zero. If not, the SCR will turn back on and current will continue to flow until S_3 is opened.

The turn-off interval t_1 can be measured by observing the anode to cathode voltage across SCR_1 on a high speed oscilloscope. A waveshape similar to that shown in the figure will be observed.

Satisfactory operation of this circuit requires careful attention to detail. The DC source must have good regulation if C_1 is to develop ample commutation voltage for turning off SCR_1. In order to minimize circuit inductance, power leads should be heavy copper braid when testing medium and high current SCR's and lead lengths should be held to an absolute minimum.

Turn-off time testing in the General Electric factory is performed with a fixed rate of rise of reapplied forward voltage as indicated by the dashed line in Figure 20.25. This is a more severe test on the SCR than the exponential curve and it requires considerably more elaborate test equipment than in Figure 20.25. For those who wish to test under these conditions, information on the factory test circuit will be provided upon request. (Ref. 5.)

Turn-off time is sometimes specified with an inverse diode connected in parallel with the D.U.T., which is a more severe test. Special attention should be given to reverse bias conditions when comparisons of "turn-off time" are made.

20.14 THERMAL RESISTANCE TEST

The thermal resistance of a thyristor is a measure of the ability of the thyristor package to remove heat from the silicon pellet. Therefore it is a limitation on the power handling capability of the device. Thermal resistance is measured in degrees Centigrade per watt, that is, in degrees Centigrade of temperature rise for each watt of power dissipated.

Since it is impossible to measure the junction temperature rise directly, the temperature dependence of the on-state voltage with a low-level current flowing is used to measure junction temperature rise, while a constant power is being dissipated under constant cooling conditions.

A thermal resistance test set must supply the on-state current (heating source), the reference current supply and an on-state voltage drop measuring circuit. A heat sink must be provided for the test device. A simplified version of a practical thermal resistance tester is shown in Figure 20.28 which can be used for SCR or rectifier measurements.

The measurement of thermal resistance, junction to case, consists of making measurements to satisfy the following equation:

$$R_{\theta JC} = \frac{T_J - T_C}{P_{(AVG)}} = \frac{T_{C1} - T_{C2}}{V_{T(HTG)} \cdot I_{T(HTG)} \cdot \text{Duty Factor}}$$

T_{C1} = The measured case temperature with only metering current flowing

T_{C2} = This is measured case temperature when the thyristor is mounted to a heat dissipator and operated with power applied

$I_{T(HTG)}$ = Heating current

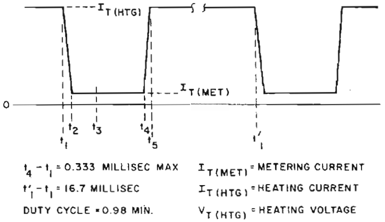
$V_{T(HTG)}$ = The measured value of on-state voltage when $I_{T(HTG)}$ is applied

When thermal resistance, junction to ambient T_{C2} should be replaced by T_A (ambient temperature).

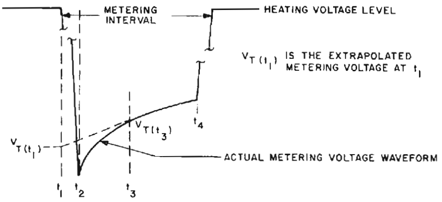
Test Procedure – Step 1

First the D.U.T. is operated with power intermittently applied, but at very high duty cycle. During the intervals between power pulses, the heating current is removed and with metering current flowing, the metering voltage is measured.

The D.U.T. current and voltage waveform are shown in Figure 20.26(a) and (b) for a 60 Hz repetition rate.



(a) Current Waveform



(b) Voltage Waveform

FIGURE 20.26 CURRENT & VOLTAGE WAVEFORMS DURING THERMAL RESISTANCE TEST

The metering current which flows continuously must be held constant. This is particularly important during the metering interval between power pulses, because the test device impedance will vary considerably during that time.

It would be desirable to arrive at the thyristor virtual junction temperature at the exact instant when the heating current removal is initiated since the virtual junction temperature will be maximum at that time. However this is not possible. First it takes a finite time for the thyristor current to decay from the heating current value to the metering current value ($t_2 - t_1$ in Figure 20.26(b). Secondly, transients will exist in the metering voltage waveform for some time after the metering current value is reached due primarily to charge storage effects in the thyristor. The time t_3 on the waveforms represents the

shortest time after removal of heating current that metering may be measured. For a particular device type the time t_3 is best found by performing the test at various power levels and noting the shortest time where the measured value of thermal resistance is essentially independent of the power dissipated. Power levels of 25% above and below the power corresponding to the specified heating current are recommended for this determination. Time t_3 should be expected to be in the range of 100 to 200 microseconds.

Since some active element cooling occurs between the time when the heating current is removed and time t_3, the thermal resistance value determined from a metering voltage measurement at t_3 will be in error, it is therefore necessary to extrapolate the metering voltage waveform back to t_1 from t_3 based on the shape of the waveform from t_3 to t_4 where the waveform is a true representation of the junction temperature cooling curve. An exponential curve is a reasonably good approximation of the true cooling curve. In the time range of interest, the exponential curve is nearly linear because the exponential time constant of the device cooling curve is relatively long. Therefore, linear extrapolation of the actual cooling curve from time t_3 back to time t_1 results in little error and is recommended. Figure 20.26(b) illustrates the extrapolation.

Step 2 — Determination of Junction Temperature

The power application test (Step 1) produced a value of on-state voltage at the metering current level which corresponded to the maximum virtual junction temperature attained. Step 2 consists of operating the test device with no significant power dissipation so that for all practical purposes the thyristor virtual junction temperature and case temperature will be equal. The thyristor is operated at the same value of metering current as in Step 1. The on-state voltage is monitored and the thyristor is externally heated on a temperature controlled block or in an oven until the measured value of on-state voltage equals the extrapolated value $V_{T(t1)}$ obtained previously. When the on-state voltage has stabilized, the thyristor case temperature is recorded. This value is T_{C1}.

When the metering current is initiated for Step 2 of the test, it should momentarily be increased to the value of $I_{T(HTG)}$ used in Step 1. This is to assure that the device is fully turned-on. The duration of the $I_{T(HTG)}$ pulse should be at least one millisecond but not longer than five seconds to avoid unnecessary heating of the test device.

If a continuous gate current value is used as a test condition for Step 1, it must also be used in Step 2.

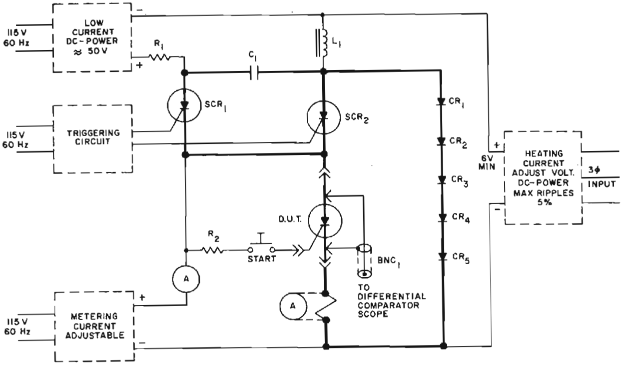


FIGURE 20.27 THERMAL RESISTANCE TEST CIRCUIT

Test Circuit

A basic circuit which may be used for testing the thyristor in Step 1 with high level (heating) current present is shown in Figure 20.27. The active element of the D.U.T. is heated by direct current having an rms ripple content of 5 percent or less which is passed continuously through the D.U.T. except for a 0.333 millisecond maximum interval every 16.7 milliseconds. During this 0.333 millisecond period, the junction temperature is indicated by reducing the on-state current to the metering current value and measuring the on-state voltage. This circuit will produce the current and on-state voltage waveshapes shown in Figures 20.26(a) and (b).

Control of the heating current through the D.U.T. is accomplished by SCR1 and SCR2 (see Figure 20.27) which functions as a dc flip-flop switching at a 60 Hertz repetition rate to facilitate oscillographic observations. Current is carried by SCR1 only during the on-state voltage metering interval so this SCR may be considerably smaller than SCR2. C_1, which is charged by the low current dc power supply has the function of turning off SCR2 when SCR1 is triggered.

Unavoidable inductance in the heating current power supply and associated circuit wiring make it impossible to turn off the heating current abruptly without creating transient voltages which would interfere with the measurement of on-state voltage. To overcome this, a diverter circuit consisting of rectifier diodes RD1 through RD5 is included so that heating current is not interrupted by SCR2, but is simply switched to a different path. The inductor L may be included to make certain that the heating current does not vary while it is being switched from one path to the other. This inductor also serves to reduce to a negligible amount undesired flow of current from C_1 through the D.U.T. and the heating current power supply. The inductance in the diverter circuit should be kept low so that 10 μs after SCR_1 begins to

contact, all heating current will have been diverted away from the D.U.T. In Figure 20.27 the portion of the circuit in which inductance must be carefully controlled is indicated by heavy lines.

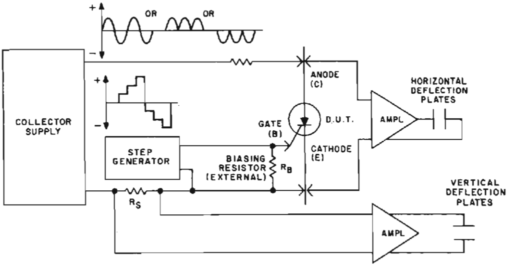
In order to observe the on-state voltage of the D.U.T. during the metering current interval, the use of a differential comparator pre-amplifier is recommended.

20.14.1 Thermal Resistance of Press Pak Rectifier Diodes & Thyristors

The Press-Pak configuration makes possible a very simple technique for measuring thermal resistance of either rectifier diodes or thyristors without the complications and inaccuracies associated with the junction temperature measurement. Since there are approximately two equal heat flow paths from junction to ambient, heat can be passed through the device from an external source to a heat sink. The heat flow can be measured and the heat flow divided into the temperature drop across the device giving the thermal resistance of its two heat flow paths in series. This method is explained in detail in Reference 1 at the end of the chapter.

20.15 TESTING THYRISTORS ON CURVE TRACERS

Curve tracers, like the Tektronix 575 and 576, are well known instruments for measuring diodes and transistors. They are also very useful to measure thyristor characteristics.



DATA FOR A 576 CURVE TRACER:

COLLECTOR SUPPLY 0 — 1500V
OR 0.1A — 10A
PULSED 20

STEP GENERATOR 5mA — 2A
OR 5mV — 40V

PULSED MODE FOR COLLECTOR SUPPLY AND STEP GENERATOR ARE POSSIBLE

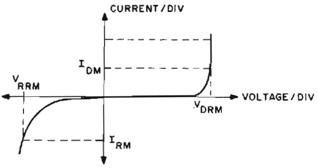
HORIZONTAL DEFLECTION
0.05V/CM — 200V/CM

VERTICAL DEFLECTION
1mA/CM — 2A/CM

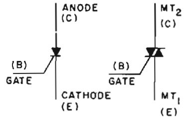
FIGURE 20.28 BLOCK DIAGRAM OF CURVE TRACER CONNECTED TO THYRISTOR

The block diagram and typical data for a Tektronix 576 in Figure 20.28 shows the suitability for testing some of the characteristics of thyristors.

20.15.1 Off-State & Reverse Voltage



(a) Scope Display of Off-State & Reverse Voltage Test



(b) Connection of Thyristors to Curve Tracer

FIGURE 20.29 DISPLAY ON CURVE-TRACER AND THYRISTOR CONNECTIONS

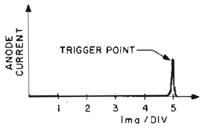
The device is connected as shown above, the gate terminal is returned to the cathode through a resistor if specified in the specification sheet. Then the voltage between anode and cathode is increased and the leakage current can be seen as the vertical deflection.

Figure 20.29 shows a scope display where an AC voltage was used to measure simultaneously the off-state and reverse directions.

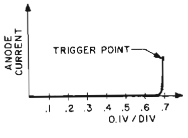
20.15.2 Gate Voltage, Gate Current Measurement

After the thyristor is connected as shown in Figure 20.29(b), the collector supply is adjusted to 12 volts (or whatever anode voltage required, but keep in mind that gate voltage and current to trigger are functions of anode voltage and junction temperature). The proper anode resistor can be selected (dissipation limiting resistor) and the *proper gate-cathode resistor* could be connected externally if necessary.

The step selector should be set to minimum current per step. Now the D.U.T. is connected to the test circuitry of the curve tracer. The horizontal amplifier will display the anode voltage (12 volts). This amplifier can then be switched to a position which will connect it to the step-generator. Depending on the position of the step generator (voltage or current) either parameter could be displayed as a horizontal deflection.



(a) Curve Tracer Display of Gate Current to Trigger



(b) Curve Tracer Display of Gate Voltage to Trigger Series Resistor = 0

FIGURE 20.30 GATE VOLTAGE & GATE CURRENT DISPLAY AT CURVE TRACER

Figure 20.30(a) and (b) show gate current and gate voltage measurement. The sensitivity at every step depends on the setting of step selector switch. By using steps/family and step zero adjustment reasonably accurate measurements can be made.

Another possibility is to display gate current and gate voltage simultaneously.

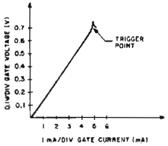


FIGURE 20.31 GATE VOLTAGE AND GATE CURRENT TO TRIGGER FOR THYRISTOR, DISPLAYED ON CURVE TRACER

The horizontal amplifier has to be switched to display base current. Sensitivity can be selected by the step selector switch (ma/step) and the vertical amplifier is switched to "base volts" position, which connects this amplifier to the D.U.T.'s gate cathode terminals. The series gate resistor no longer influences the gate voltage measurement.

20.15.3 Forward Current & On-State Voltage Measurement

The Tektronix 575 and 576 can be used to measure the on-state voltage of power thyristors and triacs up to 10 amps and in a pulsed mode up to 20 amperes. (The 576 pulsed high current fixture increases the step generator and collector supply by a factor of 10.) This is sufficient for low and medium current thyristors. After the D.U.T. is connected as shown in Figure 20.29(b), a low voltage and an appropriate series resistor on the collector supply is selected. The horizontal amplifier will display the anode current and the vertical amplifier will display the on-state voltage of the device. The device is triggered into conduction by increasing the gate current on the step selector switch. Anode current can now be increased by increasing the collector supply voltage or decreasing the dissipation limiting resistor. The horizontal deflection will allow a convenient reading of the on-state voltage of the device at the appropriate current.

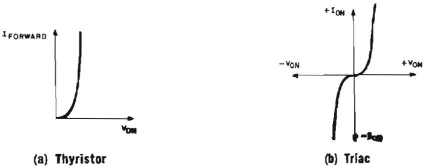


FIGURE 20.32 DISPLAY ON CURVE-TRACER OF ON-STATE VOLTAGE MEASUREMENT

More measurements like holding and latching current measurements can be done. For more information see references 2, 3, and 4.

20.16 ELEVATED TEMPERATURE TESTING

In Chapter 12, Zero Voltage Switching, there is a wealth of information on temperature controllers which would be very suitable for heating the test devices wherever elevated temperature testing is necessary.

20.17 COMMERCIAL THYRISTOR TEST EQUIPMENT

Several manufacturers offer ready-made thyristor test equipment, or design and build it to customer specifications. Some are listed below and should be contacted directly for details.

Cyberex Inc.
4399 Industrial Parkway
Willoughby, Ohio 44094

Utah Research & Development Co., Inc.
1820 South Industrial Road
Salt Lake City, Utah 84104

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97005

Mastech Inc.
478 East Brighton Ave.
Syracuse, New York 13210

REFERENCES

1. "Pressure Contact Semiconductor Devices," W. Warburton, W. F. Lootens, T. Staviski, IEEE IGA Conference Record 1966.
2. Semiconductors Device Measurements, First Edition, Tektronix, 1968.
3. Tektronix Instruction Manual, Type 575 Curve Tracer.
4. Tektronix Instruction Manual, Type 576 Curve Tracer.
5. "Turn-Off Time Characterization and Measurement of Silicon Controlled Rectifiers," R. F. Dyer and G. K. Houghton, AIEE CP 61-301. (Available as General Electric Application Note 200.15*)
6. JEDEC Recommended Standard for Thyristors, available from Electronic Industries Association, 2001 Eye Street, N.W., Washington, D.C. 20006.

*See Chapter 23 for ordering information.

21 SELECTING THE PROPER THYRISTOR AND CHECKING THE COMPLETED CIRCUIT DESIGN

21.1 SELECTING THE PROPER THYRISTOR

A glance at the device specification section in Chapter 22 shows that the equipment designer has available to him a wide range of thyristor components from which to choose. Basic SCR types are offered with current ratings extending from 0.8 amp to 1400 amps RMS, and with voltage ratings spanning the range 15 volts through 2600 volts peak. In many instances, within this range, economy/light industrial SCR's exist side by side with similarly rated industrial military types. Many *specialized* SCR types also are listed, including high speed inverter SCR's with guaranteed dynamic characteristics, SCR's for use over very wide temperature ranges, SCS's, PUT's light-activated SCR's, very high voltage SCR's, and SCR's tested to very rigid quality levels for high reliability applications. Bidirectional thyristors (triacs), intended primarily for use on 120 volt and 240 volt AC power lines, are presently available in 3, 6, 10, 15 and 25 amp sizes. Diacs and UJT's, while not strictly speaking thyristors, are included because of their wide usage as thyristor trigger components. Packaged assemblies ("stacks") of individual thyristors and/or rectifier diodes—both with and without suitable control circuitry—complete the range. For the equipment designer understandably confused by this profusion of types, the following selection criteria are offered.

21.1.1 Semiconductor Design Trade-Offs

Within the present state of the power semiconductor art, it is true to say that there is no such thing as a "universal thyristor." An SCR optimized for use in a high speed inverter or chopper circuit for instance, may be a bad choice for use in a 50 or 60 Hz phase control application. By the same token, a thyristor designed for use in very high voltage applications is by nature unsuited for use in high frequency circuits. These various incompatibilities stem from the fact that most device design approaches leading to good high power handling capabilities (voltage or current) are diametrically opposite to those leading to good high frequency performance. As a result *state of the art* high frequency devices tend to have limited power handling capabilities, while the highest power devices are relatively slow. Between these two extremes there are naturally many general-purpose devices that combine medium speed performance with medium power handling capabilities. Figure 21.1 summarizes some of the design factors that affect practical thyristor electrical performance at this writing.

Design Variable (increase)	EFFECT ON				
	Current Rating	Voltage Rating	Turn Off Time	dv/dt Withstand Ability	Ability to Switch High Currents Rapidly (di/dt)
Pellet Area (emitter)	⬆				
Base Width	↓	⬆			↓
Resistivity	↓	⬆			↓
Lifetime	⬆	⬆	↑	↓	⬆
Thermal Resistance	↓	↓	↑	↑	↓
Surface Contouring	↓	⬆			
Emitter Shorts	↓	⬆	⬇	⬆	↓
Optimized Gate Structure	(See Chapter 1 for Discussion)				

Key: Beneficial Effects—
Increase ⬆
Decrease ⬇

Undesirable Effects—
Increase ↑
Decrease ↓

FIGURE 21.1 THYRISTOR DESIGN TRADE-OFFS

Chapter 1 contains more information on these different design trade-offs. One critical item is the gate structure. The simple point gate is satisfactory for low di/dt applications but more intricate gate designs are required as di/dt stress increases. These latter designs sacrifice emitter area so that the current rating decreases for a given silicon pellet size.

There are also several design compromises discussed in Chapter 1 that can be made in the *mechanical construction* of a thyristor. For example, when a thyristor is designed specifically for use in the light industrial and consumer markets—environments characterized by limited temperature excursions and absence of wide range cyclical loading—simple low cost fabrication techniques are usually employed in its construction. Such techniques, while completely adequate for their intended purpose, would be completely unacceptable if applied to the design of a 500 amp SCR destined for use in a steel mill drive. Here, a premium thermal-fatigue resistant and high voltage structure would be a "must."

21.1.2 Selection Check List

To select and apply *any* thyristor successfully, none of its published ratings should be exceeded. Equally evident, it would be uneconomical to apply the device too conservatively. To make a proper device selection then, the equipment designer should first of all prepare a check-list outlining all the limiting conditions of his particular application. Section 21.4 contains all of the component specifications that have to be considered. Since thyristor ratings are usually specified as maximum or minimum values (worst case), the designer subsequently can determine which device best fits the needs of the application. The following is a check list of the steps that should be taken or considered in selecting the proper thyristor for a given application.

Step 1. Determine Circuit Requirements on Thyristor

Voltage across and current through the thyristor must be determined in terms of circuit input voltage and output power requirements. Figure 9.4 shows these relationships for some common SCR circuits.

Note. Check voltage transients (Chapter 16).

Check current carrying capability required of the thyristor if the *current waveform* is irregular (Chapter 3) or has a high starting component.

Determine temperature range over which the circuit must operate. Is a high-reliability or "MIL-Spec" device desirable or mandatory?

Step 2. Select Proper Thyristor

Refer to Section 22.1 and then to the more detailed specifications in Chapter 22. For final check, consider individual device specification sheets with more detailed information.

Step 3. Determine Proper Heatsink

(a) Check maximum allowable ambient temperature if a lead mounted device was selected.

(b) Select proper size heatsink from fin curves given on the specification sheet for stud mounted types. OR determine the power dissipation of the device in order to design an air or liquid cooled heat exchanger following Chapter 18. OR select suitable pre-assembled thyristor stack assembly from the many types available as indicated in Chapter 22.

Step 4. Design Triggering Circuit

See Chapter 4 for thyristor triggering requirements and design criteria. Commercially packaged triggering circuits are also available using magnetic, light sensitive or semiconductor components.

Step 5. Design Suitable Overload Protection, if Required

Protect the thyristors and associated semiconductors against short circuit and other fault conditions.[1] In some applications, economic factors and industry practice may preclude or not require protective circuitry coordination. *Do not overlook "normal overloads"* such as cold inrush to incandescent light bulbs[2] or starting current of induction motors, etc.

Beyond these elementary steps, there are often other considerations meriting special attention:

1. Series or parallel operation of individual thyristors–Chapter 6.
2. Radio interference suppression–Chapter 17.
3. Frequency response–Chapter 3 and Chapter 5.

21.2 CHECKING CIRCUIT DESIGN

The purpose of this section is to aid the designer in diagnosing and curing poor performance in his completed circuit. It also provides a step-by-step procedure for checking the design to ensure long life and reliable operation of the thyristors.

21.2.1 Thyristor Ratings and Characteristics

Thyristors must be operated within their ratings as given in the specification sheet. Do not design around samples; the sample may well be much better than the type number would indicate. If production quantities are later involved, some thyristors may be received which are, for example, of lower voltage capability than the sample or they may have longer turn-off times, lower dv/dt's, etc. *Use specification sheet limit values not data* gleaned from samples.

Voltage and current measurements must be made on all thyristors in the prototype. For this purpose an oscilloscope is essential. It should have a rise time of less than 100 nanoseconds in order that the waveforms may be reliably scanned for steep wave fronts.

Measurements should be made under extreme as well as normal load conditions. Include open-circuit operation, momentary overloads, and the first starting cycle.

21.2.2 Voltage Measurement (See also Chapter 20)

Make sure that the probe is adjusted to give a flat response. Make sure too that no ground-current loops are present; the rule is that only one ground lead should run from the circuit to the oscilloscope.

21.2.3 Current Measurement (See also Chapter 20)

Current measurements are more difficult to make accurately than voltage measurements. No universal instrument is available but satisfactory results are obtained using a combination of the following types.

Current Probe. This is a clamp-on type of current transformer with the secondary connected to an oscilloscope. An example is the Tektronix Type P6016 current probe, Figure 21.2. When used with an amplifier this probe can handle 15 amperes peak to peak and has a frequency response extending from 50 Hz to 20 mHz. It is especially useful for measuring gate-current pulses because the readings are free from external pick up.

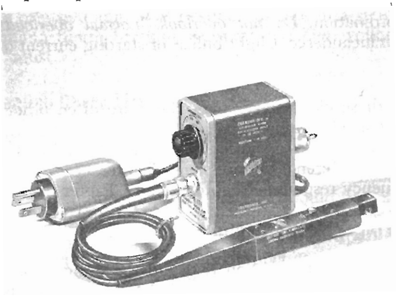


FIGURE 21.2 CURRENT PROBE AND AMPLIFIER

This type of instrument cannot measure DC and is liable to saturate if the DC component exceeds 0.5 ampere. The current range of the current probe of Figure 21.2 may be extended by winding a current transformer as shown in Figure 21.3.

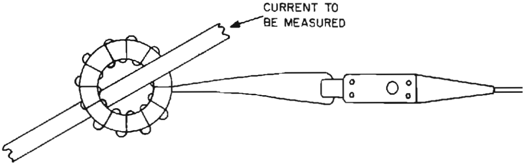


FIGURE 21.3 METHOD FOR EXTENDING CURRENT RANGE OF OSCILLOSCOPE CURRENT PROBE

The core may be of ferrite, powdered iron or powdered molybdenum (typically Arnold Mfg. Co. Cat. #106073-2). The number of turns = current ratio, thus Figure 21.3 shows a 10:1 arrangement.

Tektronix now has another clamp-on current probe that can measure both AC and DC. The Tektronix P6042 current probe is designed for use with oscilloscope systems having either 50 ohm or high-impedance inputs. The maximum currents it can measure depends upon frequency and varies from 20 A P-P at 0.1 Hz to 2 A P-P at 50 MHz.

Current Shunt. The current shunt must be a non-inductive resistor which is inserted in the circuit. The voltage across this resistor is then observed on an oscilloscope. An inexpensive form of a current shunt is described in Chapter 20 along with construction details.

A much more elegant design is shown in Figure 21.4. This shunt, made by T & M Research Products, 129 Rhode Island, N.E., Albuquerque, New Mexico 87108, has a frequency response from DC to 150 MHz and can carry 60 amperes rms continuously. The only limitations of this form of current measurement lie in the practical difficulty of inserting the shunt in the circuit and in avoiding false readings due to stray pick up from ground loops.

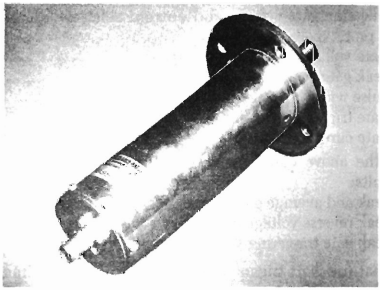


FIGURE 21.4 A COMMERCIAL NON-INDUCTIVE CURRENT SHUNT

21.2.4 The Power Circuit

The following anode voltage and current relations should be measured on all thyristors in the circuit:

Peak forward blocking voltage
Peak reverse voltage
dv/dt
Turn-off time (t_q) (if required, as in an inverter or chopper)
Rate of change of turn-on current (initial di/dt)
Forward current before turn-off (if required)
Peak reverse current (if required)
Initial start-up current, e.g., inrush or latching, and holding currents (if required)
Fault currents (if required)

These items are generally detailed in the specification sheet. If the thyristor is running outside of specifications, either choose another device with an improved rating or modify the circuit so as to run the device within ratings.

21.2.5 Modifications to Soften dv/dt

Add a series RC network across the thyristor. Note that this may, with low values of R, increase the di/dt. The effectiveness of the network may be increased by shunting a fast recovery diode across the resistor. This increases softening of the dv/dt without worsening the initial di/dt (see Chapter 6).

21.2.6 Modifications to Soften Initial di/dt

The initial di/dt may be limited by means of a reactor or saturating reactor connected in series with the thyristor. The design of the saturating reactor is discussed in Chapter 5.

21.2.7 Gate Circuit

The following gate voltage and current relations should be measured in the prototype:

Gate voltage before triggering
Peak gate triggering voltage
Pulse width of triggering gate voltage
Gate triggering current
Gate current rise time

From the above data check that the following are within the specified limits:

Peak and average gate power
Peak reverse voltage on gate
Peak gate triggering voltage

Note that for short trigger pulses the peak gate voltage that will trigger all thyristors has to be increased as the pulse width decreases (Chapter 4).

Remember that a slowly rising gate pulse that will only just trigger a thyristor is liable to increase local junction heating if fast rising anode currents exist. Always trigger an SCR used in inverters with as steep a rise time as possible (preferably shorter than 500 ns) and with as high an amplitude as is permitted. Although this "hard" drive is not always a condition of specification for some of the newer amplifying gate SCR's, it never hurts to trigger hard (within rating) as the turn-on is considerably better yet with hard drive.

Negative gate bias voltage may be applied to some SCR's that do not have emitter shorting in the off-state to improve dv/dt and turn-off time. This also eliminates random triggering due to noise. As always, the data sheet must be checked to make sure that negative gate voltage does not increase off-state blocking losses excessively (Section 4.3.5) or worse yet, trigger on the SCR.

Where the anode current of an SCR is liable to oscillate due to resonance in the load, it will be necessary to trigger the SCR with a broad pulse. A gate pulse which did not extend to time t_2 in Figure 21.5 would result in only the shaded part of the anode current flowing. By continuing the gate pulse to time t_2, the SCR will be retriggered when the circuit again causes anode current to flow. Extended gate pulse duration is also necessary when triggering is initiated before current zero in phase control applications with lagging power factor load as discussed in Section 9.6.

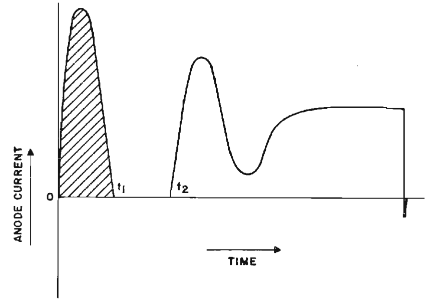


FIGURE 21.5 TYPICAL OSCILLATORY ANODE CURRENT WAVEFORM

Alternatively, the gate may be triggered by a train of pulses such as shown in Figure 21.6.

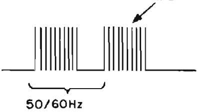


FIGURE 21.6 PULSE TRAIN FOR GATE TRIGGERING

Check the gate current for spurious signals. The clamp-on current probe described previously is ideal for this purpose.

21.2.8 Temperature Measurement

The case and junction temperatures of a thyristor have a strong influence on its characteristics. It is therefore necessary in checking thyristors in a circuit to measure the case temperature of each and, if the specification sheets do not supply adequate data, to estimate the junction temperature.

The power dissipation and consequently case temperature, depend upon the on-state voltage and switching losses. Since the thyristor being tested most likely will not be a limit sample, the following procedure should be followed in making a heat run:

1. Refer to the specification sheets to find the maximum power dissipation under worst case load current.
2. Disable the rest of the circuit and pump DC current through the device.
3. Measure the on-state voltage with a digital voltmeter or other highly accurate voltmeter.
4. Increase the current until the worst case power dissipation limit is attained and measure the case temperature at the highest expected ambient temperature.

The estimated junction temperature should then be used in prescribing the required thyristor characteristics. Methods of calculating the junction temperature are discussed in Chapter 3.

21.2.9 Magnetic Saturation

Iron core inductors and transformers can saturate and can cause of some thyristor circuits to malfunction. There are two cases where unexpected saturation can commonly be encountered.

1. In phase control circuits with a transformer load. Asymmetrical triggering, whether gate or anode type triggering, will cause a DC component of current to flow through the transformer, thus tending to saturate it.

2. When an inverter is initially triggered, the voltage applied to the iron core transformer may be in the same polarity as the half cycle before it was previously turned off. The additional magnetomotive force may cause saturation of the core.

Corrective methods include:

(a) Designing the core for operation at reduced flux density.
(b) Controlling the trigger pulses so that the magnetization polarity is symmetrical and is always automatically reversed.
(c) Starting at a frequency which is momentarily higher than normal.
(d) Introduction of current limiting impedance.

21.2.10 Supply Impedance

Check the power supply impedance. Remember that in an inverter the supply has to carry output-frequency current. Electrolytic capacitors are not always suitable for carrying AC superimposed on DC owing to their relatively high loss factor. Oil impregnated paper capacitors are much better.

Avoid having mechanical switches in the line from the supply to the thyristor whenever possible. Contact bounce is a common cause of transients and high values of dv/dt.

21.3 SCR SELECTION EXAMPLES

One of the more critical factors involved in selecting the proper SCR is the current carrying capability of the device. Too large an SCR will needlessly raise the cost of the design while too small a one will compromise the reliability, since, like all solid state devices, SCR's are very sensitive to over temperature.

21.3.1 Current Conversion Factors

Quite frequently it is required to compute the RMS and/or average current from peak currents, pulse widths, phase angles, etc., in order to choose the proper thyristor. Therefore, this section contains many different formulae and graphs to facilitate these conversions.

21.3.2 Definitions of Terms

For the sake of completeness, the following definitions have been grouped together. From Figure 21.7:

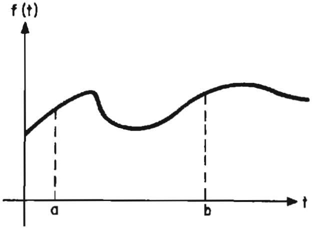


FIGURE 21.7 DEFINITION OF TERMS

1) The average value of the function f(t) over the interval $a \leqq t \leqq b$ is:

$$AVG = \frac{1}{b-a}\int_a^b f(t)\,dt \tag{21.1}$$

2) The RMS value is:

$$RMS = \left[\frac{1}{b-a}\int_a^b f(t)^2\,dt\right]^{1/2} \tag{21.2}$$

3) Form factor (F) is defined as:

$$F = \frac{RMS}{AVG} \tag{21.3}$$

The following special cases, which are significant in thyristor circuits, can be derived from the above formulas:

1) Half-wave phase control:

$$I_{AVG} = \frac{I_{PK}}{2\pi}\left[1 + \cos\alpha\right] \tag{21.4}$$

$$I_{RMS} = \frac{I_{PK}}{2}\left[1 - \frac{\alpha}{\pi} + \frac{\sin 2\alpha}{2\pi}\right]^{1/2} \tag{21.5}$$

$$F = \frac{\pi\left[1 - \frac{\alpha}{\pi} + \frac{\sin 2\alpha}{2\pi}\right]^{1/2}}{1 + \cos\alpha} \tag{21.6}$$

Where α is the phase angle of triggering. Figure 9.2 has plotted the ratio of I_{AVG}/I_{PK}, I_{RMS}/I_{PK} and F vs α is shown in Figure 9.7.

2) Full-wave phase control (see Figures 9.3 and 9.7):

$$I_{AVG} = \frac{I_{PK}}{\pi}\left[1 + \cos\alpha\right] \tag{21.7}$$

$$I_{RMS} = \frac{I_{PK}}{\sqrt{2}}\left[1 - \frac{\alpha}{\pi} + \frac{\sin 2\alpha}{2\pi}\right]^{1/2} \tag{21.8}$$

$$F = \frac{\pi}{\sqrt{2}}\,\frac{\left[1 - \frac{\alpha}{\pi} + \frac{\sin 2\alpha}{2\pi}\right]^{1/2}}{1 + \cos\alpha} \tag{21.9}$$

Note that values from Figure 9.7 must be divided by $\sqrt{2}$.

3) Variable frequency sine wave inverter (see Figure 21.8 for definition of terms):

$$I_{AVG} = \frac{2 \cdot I_{PK}}{\pi}\left(\frac{\tau}{T}\right) \tag{21.10}$$

$$I_{RMS} = I_{PK}\left[\frac{\tau}{2T}\right]^{1/2} \tag{21.11}$$

$$F = \frac{\pi}{2}\left[\frac{T}{2\tau}\right]^{1/2} \tag{21.12}$$

4) Rectangular waveshapes:

$$I_{AVG} = I_{PK}\left(\frac{\tau}{T}\right) \tag{21.13}$$

$$I_{RMS} = I_{PK}\left[\frac{\tau}{T}\right]^{1/2} \tag{21.14}$$

$$F = \left[\frac{T}{\tau}\right]^{1/2} \tag{21.15}$$

Equations 21.10 through 21.15 have been plotted on Figures 21.8 and 21.9.

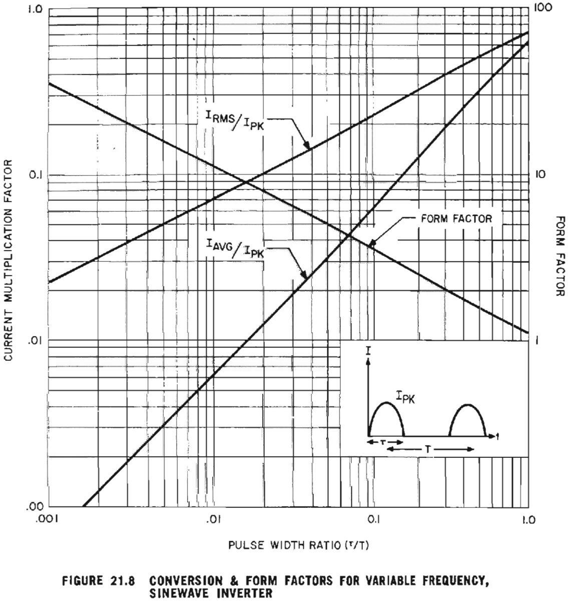


FIGURE 21.8 CONVERSION & FORM FACTORS FOR VARIABLE FREQUENCY, SINEWAVE INVERTER

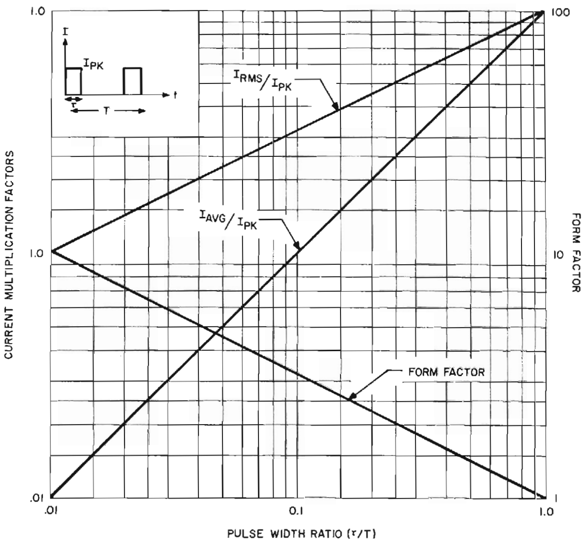


FIGURE 21.9 CONVERSION & FORM FACTORS FOR VARIABLE WIDTH RECTANGULAR WAVE INVERTERS

21.3.3 SCR Bridge

The basic three phase SCR bridge as shown in Figure 21.10, is being used to control a 75 HP, 500 V DC motor. The motor is rated at 126 A full load and can withstand a 200% overload condition for one minute.

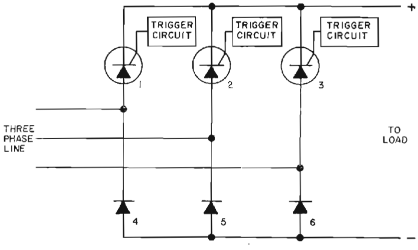


FIGURE 21.10 THREE PHASE BRIDGE CIRCUIT WITH THREE CONTROLLED LEGS

Since the thermal time constants of SCR's are so small in comparison to a motor, a one minute overload for them puts them practically into thermal equilibrium. Therefore the SCR and heatsink are designed around the overload limit. Under this condition:

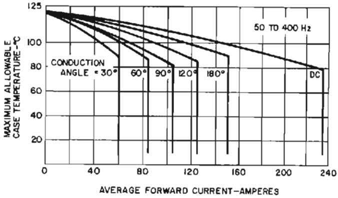
I_{AVG} (SCR) = 252/3 = 84 A (120° conduction)

I_{RMS} (SCR) = (252) (0.578) = 145 A (RMS)

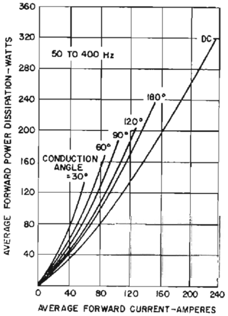
Therefore, step 1 is to find all phase control SCR's that can carry this current at "reasonable" case temperatures.

The units selected from Chapter 22 based on the RMS limit that should be considered would be: C180, C185, C280, C350, C354 and C358. But the C354, C358 and C185 are inverter types and since their good dynamic characteristics are not needed here, they can be deleted from the list. The C280 is really too large so it too can be eliminated.

Before proceeding, the data sheets on these devices must be consulted. Figures 21.11 and 21.12 show the current derating with temperature and power dissipation of these two devices.

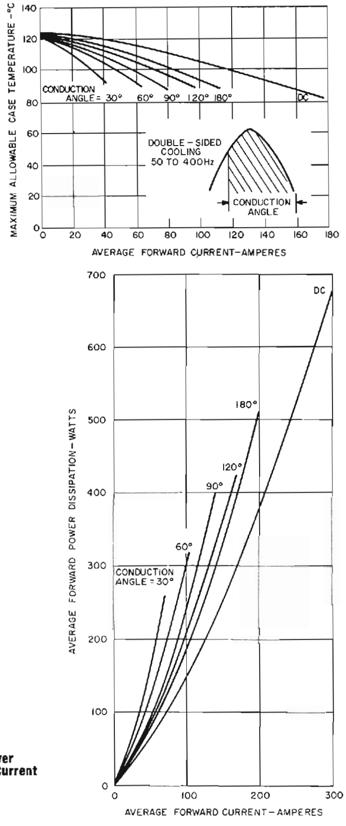


a. Maximum Allowable Case Temperature For Sinusoidal Current Waveform



b. Average Forward Power Dissipation For Sinusoidal Current Waveform

FIGURE 21.11 ALLOWABLE CURRENT AND POWER DISSIPATION CURVES FOR THE C180 SCR



a. Maximum Allowable Case Temperature For Sinusoidal Current Waveform

b. Average Forward Power Dissipation For Sinusoidal Current Waveform

FIGURE 21.12 ALLOWABLE CURRENT AND POWER DISSIPATION CURVES FOR THE C350 SCR

At 120° conduction 84 A average, the maximum case temperatures allowed for these two devices are:

T_C (C350) = 93°C (double side cooling)

T_C (C180) = 100°C

The respective power dissipations are:

P (C350) = 160 watts

P (C180) = 115 watts

Determine the maximum permissible heatsink temperature under the overload condition assuming that the C350 has a thermal contact resistance of .03°C/watt while that of the C180 is .08°C/watt when coated

with a thin layer of silicone grease.

$$T_{H.S.}\ (C350) = 93 - (.03 \times 160) \approx 88°C$$
$$T_{H.S.}\ (C180) = 100 - (.08 \times 115) \approx 91°C$$

The final step is the heatsink design. The required thermal resistance of the heatsink to allow the SCR to operate in a 40°C ambient is:

$$R_{\Theta SA}\ (C350) = \frac{T_S - T_A}{P_{D(M)}}$$
$$= \frac{88 - 40}{160} \approx .30°C/W$$
$$R_{\Theta SA}\ (C180) = \frac{91 - 40}{115} \approx .44°C/W$$

Both SCR's would be reasonable choices. The final selection will be economic since now the lower cost of the C350 is going to be traded off against a larger and more expensive heatsink. Furthermore, protection for the C180 will be easier because of its larger I^2t, almost four times larger than that of the C350. There are also several intangible factors such as ease of SCR replacement in the field and slightly better reliability of the larger device since it will run slightly cooler under normal operating conditions.

21.3.4 Inverter SCR Selection

The current waveshapes of a 1 kHz sinewave inverter can be seen in Figure 21.13. The SCR must block 900 volts.

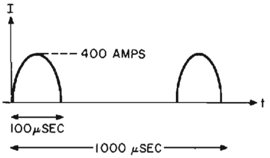


FIGURE 21.13 EXAMPLE SINEWAVE INVERTER WAVEFORMS

From Figure 21.8, $I_{(RMS)} = 89$ A. The following 110 $A_{(RMS)}$ SCR's have been chosen from Chapter 22 for closer scrutiny — C52, C150, C154 and C158.

Since the C52 and C150 are phase control devices, the dynamic stresses imposed by the circuit, such as turn-off time, dv/dt and di/dt, will cause these SCR's to malfunction. The upper blocking voltage of the C154, moreover, is 600 volts, which is 300 volts short of the required 900 volts.

Figure 3.19 in Chapter 3 shows the maximum, allowable sinewave current pulses for the C158. At 1 kHz, 100 μsec pulse, the peak current is 450 A. Since this device is also available in voltage grades up to 1200 volts, it is the natural choice for this application. The commutation circuit is designed to exceed its maximum turn-off time by a suitable safety margin.

21.4 CHECK LIST

Measure and check the following against the component specifications.

Max. Load	Min. Load	Starting Load	
☐	☐	☐	Peak forward blocking voltage
☐	☐	☐	Peak reverse voltage
☐	☐	☐	Rate of change of turn-on current at operating frequency
☐	☐	☐	Forward current before turn-off
☐	☐	☐	Average forward current
☐	☐	☐	RMS forward current
☐	☐	☐	Peak reverse current
☐	☐	☐	Surge currents
☐	☐	☐	Maximum gate voltage before triggering
☐	☐	☐	Maximum gate reverse voltage before triggering
☐	☐	☐	Peak gate triggering voltage
☐	☐	☐	Peak gate triggering current
☐	☐	☐	Peak gate power
☐	☐	☐	Average gate power
☐	☐	☐	Gate voltage rise time
☐	☐	☐	No spurious signals on gates
☐	☐	☐	Gate pulse width suitable for the circuit
☐	☐	☐	No undesired saturation in magnetic core reactors
☐	☐	☐	No undesired saturation in magnetic core transformers
☐	☐	☐	Power supply impedance
☐	☐	☐	No contact bounce effects from mechanical switches
☐	☐	☐	Electrolytic capacitors checked for high AC current
☐	☐	☐	Case temperature
☐	☐	☐	Operation satisfactory at maximum ambient temperature
☐	☐	☐	Operation satisfactory at minimum ambient temperature

REFERENCES

1. "Take the Guesswork Out of Fuse Selection," F. B. Golden, The Electronic Engineer, July 1969.
2. "Solid State Incandescent Lighting Control," R. W. Fox, Application Note 200.53,* General Electric Company, Syracuse, N. Y.

*Refer to Chapter 22 for availability and ordering information.

22 GENERAL ELECTRIC THYRISTOR AND DIODE CONDENSED SPECIFICATIONS

This chapter is primarily devoted to condensed specifications of General Electric's thyristors, thyristor assemblies, trigger devices, and diodes. These specifications are intended for reference only. For full information the designer should rely on the complete specifications indicated for each type.

The Selector Guides for Phase Control and Inverter SCR's are laid out to provide quick recognition of the four major selecting parameters — current, voltage, speed (for Inverter SCR's) and package. Other important parameters such as surge current and dv/dt capability are also included. Comments highlighting unique characteristics, package types, etc., are included to aid you in your SCR selection.

Unabridged specifications should be consulted for detail design parameters.

The initial selection of an SCR starts with identifying the current requirements, since this offers a measure of SCR pellet and/or package size. SCR's are generally categorized by maximum allowable RMS current, $I_{T(RMS)}$. The designer is cautioned that actual SCR current capability is influenced by the

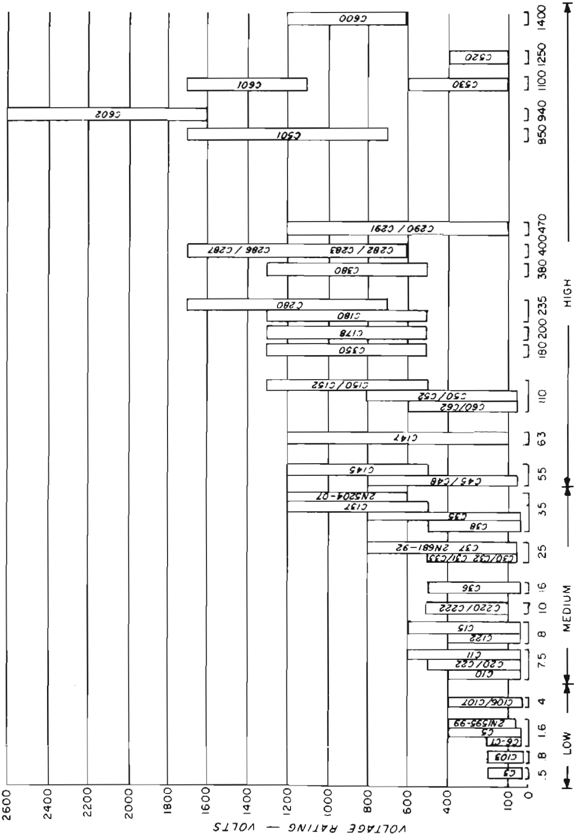
- cooling system
- switching frequency (more prevalent with inverter applications)
- ambient temperature
- coordination of SCR surge current capability with system current limiting (fusing)

It's prudent to check the detailed current rating information provided on the full specification insuring that the SCR's maximum current rating exceeds the worst case use conditions.

"Phase Control" is a term used to describe SCR's where fast turn-off time is not a prime requirement. The trade-offs in SCR design are such that turn-off time has an unfavorable relationship to current and voltage capability for any given junction size. Primary application for a device with relatively slow turn-off are AC phase control — hence the name "Phase Control." This type of device is also used for zero voltage switching and select pulse applications.

Inverter SCR's are characterized for turn-off time (commutation speed) capability and other speed characteristics. When designing for speed, the parameter trade offs must be carefully weighed. Thus the large matrix of speed, current and voltage capability for inverter SCR's. As the name implies, major applications for these devices are DC/AC inverters. Additionally, they are used in cycloconverters and other pulse applications requiring high speed capability.

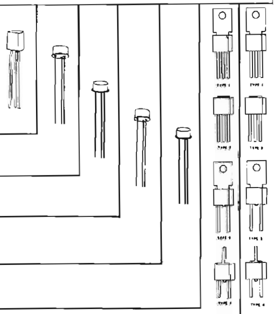
22.1 PHASE CONTROL SCR's



SELECTOR GUIDE PHASE CONTROL SCR's

ᴾHASE CONTROL SCR's .8 TO 4.0 AMPERES

GE TYPE		C103	C8	C7	C5	—	C106	C107
JEDEC		—	—	2N2344-48	2N2322-29 *	2N1595-99	—	—
SPECIFICATIONS								
VOLTAGE RANGE		30-200	25-200	25-200	25-400	50-400	15-400	15-400
CONDUCTION								
$I_{T(RMS)}$	Max. RMS on-state current (A)	0.80	1.60	1.60	1.60	1.60	4.00	4.00
$I_{T(AV)}$	Max. average on-state current @ 180° conduction (A) @ T_C	0.50 @ 25°C	1.0 @ 85°C	1.0 @ 55°C	1.0 @ 85°C	1.0 @ 110°C	2.5 @ 30°C	2.5 @ 20°C
I_{TSM}	Max. peak one cycle, non-repetitive surge current (A)	8.0	—	15	15	15	20	15
I^2t	Max. I^2t for fusing for <1.5 msec (A^2 sec)	—	0.5	—	0.5	0.5	0.5	0.5
V_{TM}	Max. peak on-state voltage @ 25°C, I_{TM} (V)	1.5	1.4	2.0	2.2	2.0	2.2	2.5
$R_{\theta JC}$	Max. internal thermal resistance, dc, junction-to-case (°C/W)	125	18	18	18	18	10	10
I_H	Max. holding current @ 25°C (mA)	5.0	5.0	1.0	2.0	0.5	3.0	6.0
t_q	Typical turn-off time (μsec)	15 —	40 —	20 —	40 —	40 —	40 100 [1]	40 100 [1]
$t_d + t_r$	Typical turn-on time (μsec)	—	1.4	1.4	1.4	1.2	1.2	1.2
di/dt	Max. rate-of-rise of on-state current (A/μsec)	—	—	—	50	—	50	50
T_J	Junction operating temperature range (°C)	−65 to 125	−40 to 125	−65 to 100	−65 to 125	−65 to 150	−40 to 110	−40 to 110
OFF-STATE								
dv/dt	Typical critical rate-of-rise of off-state voltage, exponential to rated V_{DRM} @ max. rated T_J (V/μsec)	20	5	1	5	5	8	8
SPECIFICATION SHEET NO.		150.7	150.8	150.11	150.10	150.15	150.9	150.13



PLANAR PASSIVATED. EPOXY ENCAPSULATED. LOW CURRENT. FOR COST CONSCIENCE VOLUME APPLICATIONS.

GENERAL PURPOSE. LOW CURRENT. HERMETIC PACKAGE.

LOW T_J VERSION OF C8.

GENERAL PURPOSE LOW CURRENT. JAN & JANTX TYPES.

SIMILAR TO C5 SERIES. EXCEPT HIGHER 150°C T_J RATING.

THE ORIGINAL SILICONE ENCAPSULATED, PLANAR PASSIVATED SCR. FOR COST CONSCIENCE VOLUME APPLICATIONS.

SIMILAR TO C106 EXCEPT 15A SURGE RATING. LOWER COST THAN C106.

PHASE CONTROL SCR's 7.4 TO 25 AMPERES

GE TYPE		C10	C11	C15	C122	C20-22	C220, 222		C30,31,32,33	C37
JEDEC		2N1770A-77A*	2N1770-78	—	—	—	—	2N1842-50	—	—
SPECIFICATIONS										
VOLTAGE RANGE		25-400	25-800	25-600	50-500	25-500	25-500	25-800	25-500	25-600
CONDUCTION										
$I_{T(RMS)}$	Max. RMS on-state current (A)	7.40	7.40	8.0	8.0	7.40	10	16.0	25.0	25.0
$I_{T(AV)}$	Max. average on-state current @ 180° conduction (A) @ Tc	4.7 @ 105°C	4.7 @ 80°C	5.1 @ 50°C	5.1 @ 75°C	4.8 @ 87°C	6.3 @ 67°C	10.0 @ 35°C	16.0 @ 70°C	16.0 @ 35°C
I_{TSM}	Max. peak one cycle, non-repetitive surge current (A)	60	60	60	90	80	80	125	250	125
I^2t	Max. I^2t for fusing for >1.5 msec (A^2 sec)	5	5	5	25	27	27	—	260	40
$t_d + t_r$	Typical turn-on time (μsec)	1.0	1.0	1.0	—	2.5	40	3	3	3
di/dt	Max. rate-of-rise of on-state current (A/μsec)	30	30	30	50	—	50	15	—	15
T_J	Junction operating temperature range (°C)	−65 to 150	−65 to 125	−65 to 105	−40 to 100	−40 to 100	−40 to 100	−40 to 100	−40 to 100	−40 to 105
OFF-STATE										
dv/dt	Typical critical rate-of-rise of off-state voltage, exponential to rated V_{DRM} @ max. rated T_J (V/μsec)	40	50	60	40	40	40	40	40	40
SPECIFICATION SHEET NO.		150.20	150.21	150.22	150.35	150.30	150.36	160.19	160.27	160.23

GENERAL PURPOSE 150°C T_J RATING.
JAN & JANTX & HI REL TYPES.

GENERAL PURPOSE. FOR INDUSTRIAL APPLICATIONS.

GENERAL PURPOSE.

SILICONE ENCAPSULATED WITH POWER GLAS PASSIVATED PELLET.
FOR COST CONSCIENCE VOLUME APPLICATIONS.

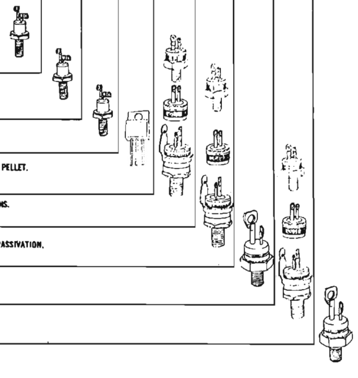
GENERAL PURPOSE. FOR VOLUME INDUSTRIAL APPLICATIONS.
3 PACKAGE CONFIGURATIONS.

MEDIUM CURRENT SCR FEATURING POWER GLAS PELLET PASSIVATION.
3 PACKAGE CONFIGURATIONS.

GENERAL PURPOSE CHASIS MOUNT SCR.

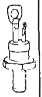
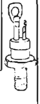
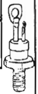
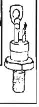
SIMILAR TO C20 EXCEPT HIGHER CURRENT RATINGS.

GENERAL PURPOSE.



PHASE CONTROL SCR's 25 TO 35 AMPERES

GE TYPE		—	C35	C38	C137	—
JEDEC		2N681-92	—	—	—	2N5204-07
SPECIFICATIONS						
VOLTAGE RANGE		25-800	25-800	25-800	500-1200	800-1200
CONDUCTION						
$I_{T(RMS)}$	Max. RMS on-state current (A)	25.0	35.0	35.0	35	35
$I_{T(AV)}$	Max. average on-state current @ 180° conduction (A) @ T_C(°C)	16.0 @ 65°C	22.3 @ 40°C	22.5 @ 70°C	22.3 @ 67°C	22.3 @ 40°C
I_{TSM}	Max. peak one cycle, non-repetitive surge current (A)	150	225	225	380	300
I^2t	Max. I^2t for fusing for 5 to 8.3 msec (A^2 sec)	100	100	100	460	370
di/dt	Max. rate-of-rise of on-state current (A/μsec)	10	20	—	150	100
T_J	Junction operating temperature range (°C)	−65 to 125	−65 to 125	−65 to 150	−65 to 125	−40 to 125
OFF-STATE						
dv/dt	Min. critical rate-of-rise of off-state voltage, exponential @ max. rated T_J (V/μsec)	20 Typ.	10	20	100	100
SPECIFICATION SHEET NO.		160.22	160.20	160.30	160.45	160.45

POPULAR GENERAL PURPOSE CHASSIS MOUNT SCR. JAN & JANTX TYPES.

THE ORIGINAL SCR. FOR GENERAL PURPOSE APPLICATIONS. HI REL TYPES AVAILABLE.

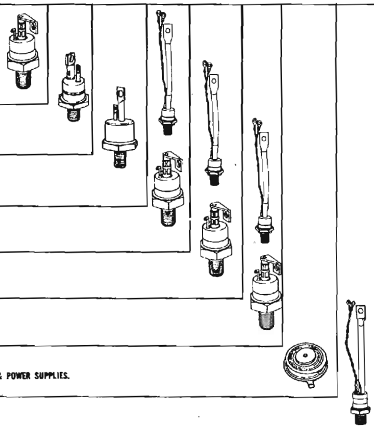
SIMILAR TO C35 SERIES EXCEPT 150°C T_J RATING.

HIGH VOLTAGE, HIGH PERFORMANCE FOR DEMANDING INDUSTRIAL APPLICATIONS. HI REL TYPES AVAILABLE.

SIMILAR TO C137.

PHASE CONTROL SCR's 55 TO 200 AMPERES

GE TYPE		C45, 46	C145	C147	C50, 52	C150, 152	C60, 62	C350	C178
JEDEC					2N1909-16 2N1792-98		2N2023-30		CONTACT FACTORY
SPECIFICATIONS									
VOLTAGE RANGE		25-800	500-1200	100-1200	25-800	500-1300	25-400	500-1300	500-1300
CONDUCTION									
$I_{T(RMS)}$	Max. RMS on-state current (A)	55	55	63	110	110	110	180	200
$I_{T(AV)}$	Max. average on-state current @ 180° conduction (A) @ T_C	35 @ 87°C	35 @ 90°C	35 @ 90°C	70 @ 62°C	70 @ 80°C	70 @ 88°C	125 @ 80°C	127 @ 80°C
$I_{T(AV)}$	Max. average on-state current @ 120° conduction (A) @ T_C	29 @ 90°C	29 @ 93°C	29 @ 93°C	60 @ 64°C	59 @ 87°C	59 @ 90°C	110 @ 80°C	100 @ 80°C
I_{TSM}	Max. peak one cycle, non-repetitive surge current (A)	700	700	1000	1000	1500	1000	1500	2500
I^2t	Max. I^2t for fusing for 5 to 8.3 msec (A^2 sec)	2000	2000	4000	4000	7000	4000	10,000	25,000
di/dt	Rate-of-rise of on-state current (A/μsec)	30	100-200	100-200	30	50-75	30	50-100	50-100
T_J	Junction operating temperature range (°C)	−40 to 125°C	−40 to 125°C	−40 to 125°C	−40 to 125°C	−40 to 125°C	−65 to 150°C	−40 to 125°C	−40 to 125°C
OFF-STATE									
dv/dt	Min. critical rate-of-rise of off-state voltage, exponential @ max. rated T_J (V/μsec)	30 TYP.	200	200 TYP.	30 TYP.	200	30 TYP.	200	200
SPECIFICATION SHEET NO.		170.17	170.18	170.19	170.20	170.23	170.26	170.54	170.51



LOW CONDUCTOR LOSSES.
FOR GENERAL PURPOSE APPLICATIONS.

EXCELLENT dv/dt & di/dt RATINGS.
LOW POWER GATE REQUIREMENTS.

RUGGED HERMETIC PACKAGE.
¼-28 STUD. MIN DV/DT = 200 V/μSEC

VERY LOW FORWARD CONDUCTION LOSSES
& GATE POWER REQUIREMENTS.

HIGH dv/dt.
FOR MOTOR CONTROLS & POWER SUPPLIES.

150°C T_J RATING
FOR NATURAL CONVECTION APPLICATIONS.

PRESS PAK FOR Θ_{J-C}
HIGH dv/dt. EXCELLENT FOR MOTOR CONTROLS & POWER SUPPLIES.

HIGH dv/dt FOR 200A CURRENT REQUIREMENTS.

PHASE CONTROL SCR's 235 TO 470 AMPERES

GE TYPE		C180	C280	C380	C282, 283	C286, 287	C290, 291
SPECIFICATIONS							
VOLTAGE RANGE		500-1300	700-1700	500 - 1300	600 - 1700	600 - 1700	100 - 1200
CONDUCTION							
$I_{T(RMS)}$	Max. RMS on-state current (A)	235	235	380	400	400	470
$I_{T(AV)}$	Max. average on-state current @ 180° conduction (A) @ T_C	150 @ 88°C	150 @ 90°C	235 @ 80°C	200 @ 80°C	225 @ 80°C	300 @ 76°C
$I_{T(AV)}$	Max. average on-state current @ 120° conduction (A) @ T_C	122 @ 83°C	125 @ 90°C	180 @ 80°C	175 @ 80°C	200 @ 80°C	250 @ 80°C
I_{TSM}	Max. peak one cycle, non-repetitive surge current (A)	3500	3500	3500	4500	5000	5500
I^2t	Max. I^2t for fusing for 5 to 8.3 msec (A^2 sec)	50,000	50,000	50,000	65,000	100,000	120,000
di/dt	Rate-of-rise of on-state current (A/μsec)	50-100	50	50-100	50	50	≤50
T_J	Junction operating temperature range (°C)	−40 to 125°C	−40 to 125°C	−40 to 125°C	−40 to 120°C	−40 to 125°C	−40 to 125°C
OFF-STATE							
dv/dt	Min. critical rate-of-rise of off-state voltage, exponential @ max. rated T_J (V/μsec)	200	100	200	100	100	100
SPECIFICATION SHEET NO.		170.52	170.58	170.56	170.59	170.58	170.60

HIGH dv/dt MEDIUM VOLTAGE.
FOR DC & AC MOTOR CONTROL & POWER SUPPLIES.

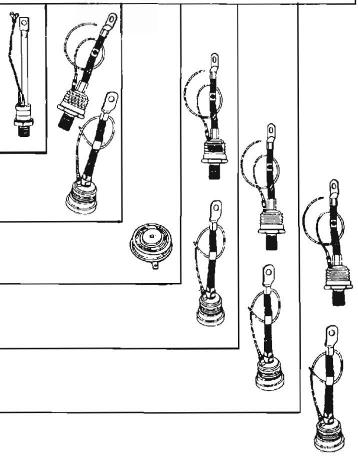
HIGH VOLTAGE. STUD PACKAGE.
FOR TAP CHANGING, AC CONTACTORS.

PRESS PAK VERSION OF C180.

HIGH VOLTAGE. 400A CURRENT RATINGS.

HIGHEST POWER STUD PACKAGED SCR.
FOR MOTOR STARTING & AC CONTACTORS.

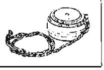
HIGHEST CURRENT STUD PACKAGED SCR.
FOR MOTOR CONTROLS & POWER SUPPLIES.



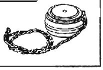
PHASE CONTROL SCR's 850 TO 1400 AMPERES

GE TYPE		C501	C530	C520	C600	C601	C602
SPECIFICATIONS							
VOLTAGE RANGE		700 - 1700	100 - 600	100 - 400	500 - 1200	1100 - 1700	1600 - 2600
CONDUCTION							
$I_{T(RMS)}$	Max. RMS on-state current (A)	850	1100	1250	1400	1100	940
$I_{T(AV)}$	Max. average on-state current @ 180° conduction (A) @ T_C	550 @ 67°C	700 @ 80°C	800 @ 75°C	900 @ 72°C	750 @ 72°C	600 @ 78°C
$I_{T(AV)}$	Max. average on-state current @ 120° conduction (A) @ T_C	400 @ 80°C	600 @ 80°C	700 @ 75°C	720 @ 80°C	600 @ 80°C	500 @ 80°C
I_{TSM}	Max. peak one cycle, non-repetitive surge current (A)	7000	10,000	10,000	13,000	10.500	6500
I^2t	Max. I^2t for fusing for 5 to 8.3 msec (A^2 sec)	200,000	415,000	415,000	700,000	516,000	176,000
di/dt	Rate-of-rise of on-state current (A/μsec)	30 - 75	75	75	30 - 75	30 - 75	30 - 75
T_J	Junction operating temperature range (°C)	−40 to 125°C	−40 to 125°C	−40 to 150°C	−40 to 125°C	−40 to 125°C	−40 to 125°C
OFF-STATE							
dv/dt	Min. critical rate-of-rise of off-state voltage, exponential @ rated T_J (V/μsec)	100	50 TYP	50 TYP	100	100	100
SPECIFICATION SHEET NO.		170.70	170.82	170.81	170.84	170.85	170.86

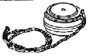
GENERAL PURPOSE HIGH POWER SCR.



LOW CONDUCTIVE LOSSES. LOW VOLTAGE. HIGH CURRENT.
AVAILABLE IN WATER COOLED CONFIGURATION.



130°C T_J.
AVAILABLE IN LIQUID COOLED HEAT EXCHANGERS.

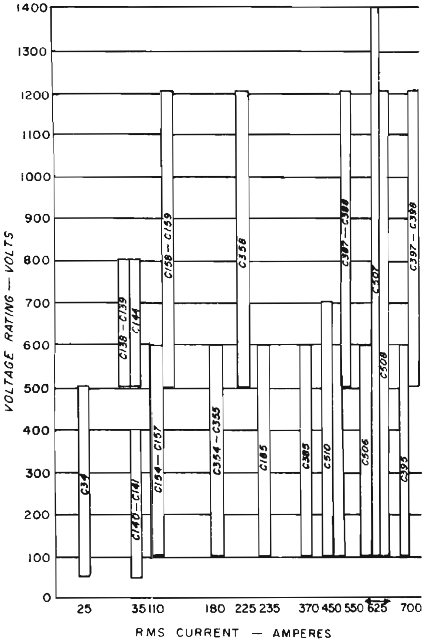


HIGH OPERATING & SURGE CURRENT RATINGS.

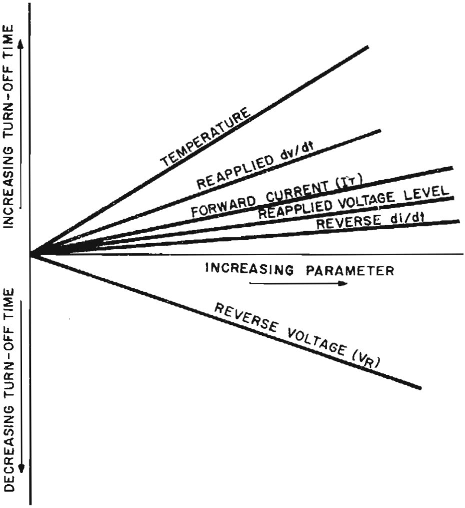
HIGH CURRENT. HIGH VOLTAGE.
FOR WELDING, HEATING & MOTOR CONTROL.

THE INDUSTRIES' HIGHEST VOLTAGE RATED SCR.
FOR CONTACTOR & MOTOR STARTING APPLICATIONS.

22.2 INVERTER SCR's



SELECTOR GUIDE
INVERTER SCR's

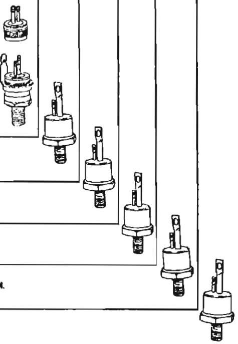


Although each type of High Speed SCR is affected to different degrees by various conditions, the directions of change remain the same. Additionally, the relative effect of each is roughly as shown above for a "generalized" High Speed SCR.

Should you determine that your conditions are more severe than those for which the turn-off time is specified, you are invited to contact General Electric to have turn-off time specified at the different conditions.

INVERTER SCR's 25 TO 35 AMPERES

GE TYPE		C34	C140	C141	C138	C139	C144
JEDEC		—	2N3649-53	2N3654-58	—	—	—
SPECIFICATIONS							
VOLTAGE RANGE		50-500	50-400	50-400	300-600	300-800	500-800
CONDUCTION							
$I_{T(RMS)}$	Max. RMS on-state current @ $T_C=65°C$, 50% duty, (A)	25	35	35	35	35	35
	1KHz	25	26	26	26	26	32
	5KHz	—	26	26	22	22	32
	10KHz	—	20	20	18	18	30
I_{TSM}	Max. peak one cycle, non-repetitive surge current (A)	250	200	200	200	200	200
I^2t	Max. I^2t for fusing @ time (ms)	220 @ 1.0	165 @ 1.0	165 @ 1.0	165 @ 0.5	165 @ 0.5	165 @ 0.5
t_q	Max. turn-off time @ rated voltage and T_J (μsec) 20V/μsec reapplied	20	—	—	—	—	—
	@ 200V/μsec reapplied	—	15	10	10-20	10-20	15-30
di/dt	Critical rate-of-rise of on-state current (A/μsec)	—	400	400	100	100	100
T_J	Junction operating temperature range (°C)	−40 to 100	−65 to 120	−65 to 120	−65 to 125	−65 to 125	−65 to 125
OFF-STATE							
dv/dt	Min. critical rate-of-rise of off-state voltage exponential to rated V_{DRM} @ Max. rated T_J (V/μsec)	20	200	200	200	200	200
SPECIFICATION SHEET NO.		160.28	160.35	160.35	160.47	160.47	160.49



FOR COST SENSITIVE VOLUME APPLICATIONS.

CHARACTERIZED TO 25 KHz.
FOR PULSE MODULATOR & NON CRITICAL tq APPLICATIONS.

CHARACTERIZED TO 25 KHz.
FOR ULTRASONIC & CRITICAL tq APPLICATIONS.

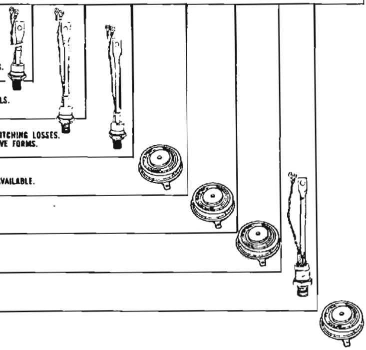
OPTIMIZED FOR VOLTAGE & TURN-OFF.
FOR OPERATION WITH FEEDBACK DIODE.

SIMILAR TO C139, DESIGNED FOR REVERSE VOLTAGE OPERATION.
CHARACTERIZED TO 25 KHz.

OPTIMIZED FOR VOLTAGE & TURN OFF.
CHARACTERIZED TO 10 KHz.

INVERTER SCR's 100-380 AMPERES

GE TYPE		C154, 156	C155, 157	C158, 159	C354	C355	C358	C185	C385
CONSTRUCTION		ALL DIFFUSED	ALL DIFFUSED	AMPLIFYING GATE	ALL DIFFUSED	ALL DIFFUSED	AMPLIFYING GATE	ALL DIFFUSED	ALL DIFFUSED
SPECIFICATIONS									
VOLTAGE RANGE		100-600	100-800	500-1200	100-600	100-800	500-1200	100-800	100-800
CONDUCTION									
$I_{T(RMS)}$	Max. forward conduction sinusoidal @ $T_C = 85°C$, 50% duty (A)								
	@ 60 Hz	110	110	110	180	180	225	235	380
	@ 600 Hz	105	105	110	170	170	225	235	320
	@ 1200 Hz	102	102	110	160	160	225	210	275
	@ 2500 Hz	85	85	100	140	140	190	180	215
	@ 5000 Hz	65	65	90	120	120	125	115	170
I_{TSM}	Max. peak one cycle, non-repetitive surge current (A)	1200	1200	1600	1200	1200	1600	3500	3500
I^2t	Max. I^2t for fusing for 8.3 msec (A^2sec)	6000	6000	10,500	6000	6000	10,500	50,000	50,000
t_q	Turn-off time @ rated voltage & T_J, V_R = 50 volts min (μsec) @ 20V/μsec reapplied	10	20	30	10	20	30	20	20
	@ 100V/μsec reapplied	15	25	35	15	25	35	25	25
	@ 200V/μsec reapplied	20		40	20		40		
di/dt	Critical rate-of-rise of on-state current (A/μsec)	100	100	800	100	100	800	100	100
T_J	Junction operating temperature range (°C)	←			−40 to 125°C				→
OFF-STATE									
dv/dt	Min. critical rate-of-rise off-state voltage exponential to rated V_{DRM} @ Max. T_J (V/μsec)	200	100	200-500	200	200	200-500	200	200
SPECIFICATION SHEET NO.		170.35	170.35	170.36	170.37	170.37	170.38	170.53	170.57



FASTEST TURN-OFF TIME AVAILABLE.
MEDIUM TO LOW FREQUENCY. LOW SWITCHING LOSSES.

FOR BATTERY VEHICLES, CHOPPERS & MOTOR CONTROLS.

FEATURES AMPLIFYING GATE. HIGH VOLTAGE. LOW SWITCHING LOSSES.
CHARACTERIZED FOR SINUSOIDAL & RECTANGULAR WAVE FORMS.

PRESS PAK, LOW SWITCHING LOSSES.
LOW THERMAL IMPEDANCE. FASTEST TURN-OFF TIME AVAILABLE.

PRESS PAK VERSION OF C155.

PRESS PAK VERSION OF C158.

LOW SWITCHING LOSSES. FAST TURN-OFF.
FOR BATTERY VEHICLE & INVERTER MOTOR DRIVE.

PRESS PAK VERSION OF C185.

INVERTER SCR's 550-625 AMPERES

GE TYPE		C392	C393	C387	C388	C506	C507	C508
CONSTRUCTION		AMPLIFYING GATE	AMPLIFYING GATE	AMPLIFYING GATE	AMPLIFYING GATE	F-I GATE	F-I GATE	F-I GATE
SPECIFICATIONS								
VOLTAGE RANGE		100-800	100-800	500-1200	500-1200	100-800	100-1400	100-1200
CONDUCTION								
$I_{T(RMS)}$	Max. forward conduction sinusoidal @ $T_C = 65°C$, 50% duty (A)							
	@ 60 Hz	550	550	550	550	625	625	625
	@ 500 Hz	450	450	530	530	625	625	625
	@ 1200 Hz	370	370	455	455	430	—	—
	@ 2500 Hz	210	210	225	225	250	—	—
	@ 5000 Hz	130	130	120	120	—	—	—
I_{TSM}	Max. peak one cycle, non-repetitive surge current (A)	5500	5500	5500	5500	8000	6500	9000
I^2t	Max. I^2t for fusing for 5 to 8.3 msec (A^2sec)	120,000	120,000	120,000	120,000	265,000	175,000	335,000
t_q	Turn-off time @ rated voltage & T_J, V_R = 50 V min. (μsec) @ 20V/μsec reapplied	10	15	30	20	35	100	60
	@ 100V/μsec reapplied	15	18	35	25	40	—	—
	@ 200V/μsec reapplied	20	20	40	30	—	—	—
di/dt	Critical rate-of-rise of on-state current (A/μsec)	800	800	800	800	100	50-75	50-75
T_J	Junction operating temperature range (°C)	←			−40 to 125°C			→
OFF-STATE								
dv/dt	Min. critical rate-of-rise off-state voltage exponential to rated V_{DRM} @ Max. T_J (V/μsec)	200	200	200-500	200-500	200	200	200
SPECIFICATION SHEET NO.		170.42	170.42	170.44	170.44	170.76	170.77	170.78

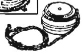
LOW SWITCHING LOSSES. FAST TURN-OFF.
FOR BATTERY VEHICLE & INVERTER MOTOR DRIVE.

LOW SWITCHING LOSSES. FAST TURN-OFF.
FOR BATTERY VEHICLE & INVERTER MOTOR DRIVE.

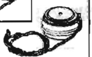
HIGH VOLTAGE.
FOR LOW-MEDIUM FREQUENCY APPLICATIONS.

HIGH VOLTAGE. FAST TURN-OFF.
FOR MEDIUM FREQUENCY APPLICATIONS.

LOW VOLTAGE.
FOR MEDIUM FREQUENCY APPLICATIONS.



HIGH VOLTAGE.
FOR LOW FREQUENCY APPLICATIONS.



HIGH I^2t. LOW LOSS
FOR LOW FREQUENCY APPLICATIONS.

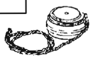
INVERTER SCR's 625-700 AMPERES

GE TYPE		C397	C398	C510	C394	C395
CONSTRUCTION		AMPLIFYING GATE	AMPLIFYING GATE	F-I GATE	AMPLIFYING GATE	AMPLIFYING GATE
SPECIFICATIONS						
VOLTAGE RANGE		500-1200	500-1200	100-700	100-600	100-600
CONDUCTION						
$I_{T(RMS)}$	Max. forward conduction sinusoidal @ $T_C = 65°C$, 50% duty (A)					
	@ 60 Hz	700	700	625	700	700
	@ 600 Hz	650	650	625	700	650
	@ 1200 Hz	550	550	300	600	550
	@ 2500 Hz	275	275	190	425	275
	@ 5000 Hz	150	150	130	290	150
I_{TSM}	Max. peak one cycle, non-repetitive surge current (A)	7500	7500	4000	8000	8000
I^2t	Max. I^2t for fusing for 8.3 msec (A^2sec)	230,000	230,000	65,000	250,000	250,000
t_q	Turn-off time @ rated voltage & T_J, V_R = 50 V min. (μsec) @ 20V/μsec reapplied	40	30	12	15	15
	@ 100V/μsec reapplied	50	35	15	18	18
	@ 200V/μsec reapplied	60	40	--	20	20
di/dt	Critical rate-of-rise of on-state current (A/μsec)	800	800	400	800	800
T_J	Junction operating temperature range (°C)	← −40 to 125°C →				
OFF-STATE						
dv/dt	Min. critical rate-of-rise off-state voltage exponential to rated V_{DRM} @ Max. T_J (V/μsec)	200-500	200-500	200	200	200
SPECIFICATION SHEET NO.		170.45	170.45	170.80	170.42	170.42

HIGH POWER.
FOR LOW FREQUENCY APPLICATIONS.

FULL CONCURRENT CHARACTERIZATION OPTIMIZED
FOR 1KHz SWITCHING.

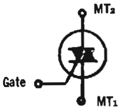
MEDIUM VOLTAGE. FAST TURN-OFF.
FOR HIGH FREQUENCY APPLICATIONS.



LOW SWITCHING LOSSES. FAST TURN-OFF.
FOR BATTERY VEHICLE & INVERTER MOTOR DRIVE.

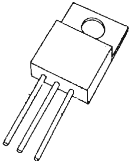
LOW VOLTAGE. MEDIUM SPEED
FOR VERY HIGH POWER CHOPPERS, INVERTER MOTOR CONTROLS.

22.3 TRIACS 6 AMPERES

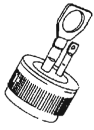


GE Type	SC240	SC240*2	SC241	SC241
Voltage Range	200-500	200-500	200-500	200-500
Current Rating (Amps RMS)	6	6	6	6
I_{TSM}, Max Peak One Cycle, Non. Rep. Surge Current (A)	80	80	80	80
I_{DRM}, Blocking Current @ 25°C, Max (mA)	.1	.1	.1	.1
dv/dt Static, @ 100°C Rated V_{DRM} Gate Open Typical (V/μsec)	50	50	50	50
dv/dt Commutating, @ 75°C Rated V_{DRM} and I_T, Gate Open Min (V/μsec)	4	4	4	4
FIRING				
I_{GT} Max DC Gate Trigger Current @ 12 V, 25°C (mA)**	50	50	50	50
V_{GT} Max DC Gate Trigger Voltage @ 12 V, 25°C (V)**	2.5	2.5	2.5	2.5
Package Type	Stud	Isolated Stud	Press Fit	Power Pac
Specification Sheet No.	←	175.16	→	175.15

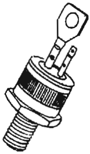
*Voltage Grade
**MT_2+ Gate+
MT_2+ Gate−
MT_2− Gate−



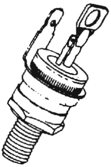
Power Pac



Press Fit



Isolated Stud

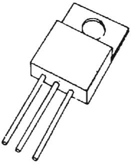


Stud

10 Ampere Triacs

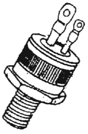
GE Type	SC245	SC245*2	SC246	SC146
Voltage Range	200-500	200-500	200-500	200-500
Current Rating (Amps RMS)	10	10	10	10
I_{TSM}, Max Peak One Cycle, Non. Rep. Surge Current (A)	100	100	100	100
I_{DRM}, Blocking Current @ 25° C, Max (mA)	.1	.1	.1	.1
dv/ dt Static, @ 100°C Rated V_{DRM} Gate Open Typical (V/μsec)	50	50	50	50
dv/dt Commutating, @ 75°C Rated V_{DRM} and I_T. Gate Open Min (V/μsec)	4	4	4	4
FIRING				
I_{GT} Max DC Gate Trigger Current @ 12 V, 25°C (mA)**	50	50	50	50
V_{GT} Max DC Gate Trigger Voltage @ 12 V, 25°C (V)**	2.5	2.5	2.5	2.5
Package Type	Stud	Isolated Stud	Press Fit	Power Pac
Specification Sheet No.	←	175.17	→	175.15

*Voltage Grade
**MT_2+ Gate+
MT_2+ Gate—
MT_2— Gate—

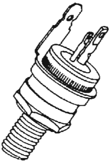


Power Pac

Press Fit



Stud

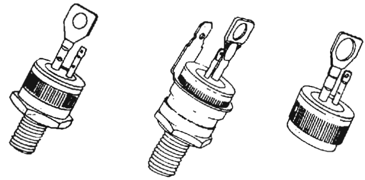


Isolated Stud

15 Ampere Triacs

GE Type	SC250	SC250*2	SC251
Voltage Range	200-500	200-500	200-500
Current Rating (Amps RMS)	15	15	15
I_{TSM}, Max Peak One Cycle, Non. Rep. Surge Current (A)	100	100	100
I_{DRM}, Blocking Current @ 25° C, Max (mA)	.1	.1	.1
dv/ dt Static, @ 100°C Rated V_{DRM} Gate Open Typical (V/μsec)	50	50	50
dv/dt Commutating, @ 75°C Rated V_{DRM} and I_T. Gate Open Min (V/μsec)	4	4	4
FIRING			
I_{GT} Max DC Gate Trigger Current @ 12 V, 25°C (mA)**	50	50	50
V_{GT} Max DC Gate Trigger Voltage @ 12 V, 25°C (V)**	2.5	2.5	2.5
Package Type	Stud	Isolated Stud	Press Fit
Specification Sheet No.	← 175.18 →		

*Voltage Grade
**MT_2+ Gate+
MT_2+ Gate−
MT_2− Gate−

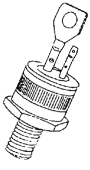


Stud Isolated Stud Press Fit

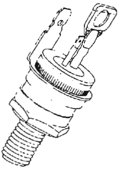
25 Ampere Triacs

GE Type	SC60	SC60*2	SC61
Voltage Range	200-500	200-500	200-500
Current Rating (Amps RMS)	25	25	25
I_{TSM}, Max Peak One Cycle, Non. Rep. Surge Current (A)	250	250	250
I_{DRM}, Blocking Current @ 25° C, Max (mA)	.5	.5	.5
dv/ dt Static, @ 100°C Rated V_{DRM} Gate Open Typical (V/μsec)	100	100	100
dv/dt Commutating, @ 75°C Rated V_{DRM} and I_T. Gate Open Min (V/μsec)	5	5	5
FIRING			
I_{GT} Max DC Gate Trigger Current @ 12 V, 25°C (mA)**	50	50	50
V_{GT} Max DC Gate Trigger Voltage @ 12 V, 25°C (V)**	2.5	2.5	2.5
Package Type	Stud	Isolated Stud	Press Fit
Specification Sheet No.	175.28	175.28	175.28

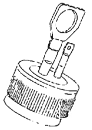
*Voltage Grade
**MT_2+ Gate+
MT_2+ Gate—
MT_2— Gate—



Stud



Isolated Stud



Press Fit

22.4 TRIAC TRIGGER DEVICES

TRIAC TRIGGER DEVICES

Because of its bilateral nature, the Triac requires its own unique trigger element, distinct from SCR's. GE offers a full line of suitable Triac triggers. The total power system is easily assembled consisting of a suitable sensor, IC, Triac and a few other passive components. The Triac may also be triggered by an SCR trigger element by using a pulse transformer.

APPLICATIONS

DEVICE	UJT PUT	SBS 2N4991-93	ST2	ST4
USE				
HEAT CONTROL	E	F	F	N
LIGHT CONTROL	F	F	F	E
MOTOR SPEED CONTROL	P	F	F	N
POWER REGULATION	E	F	F	N
SOLID STATE CONTRACTORS & RELAYS	F	F	F	N

E = EXCELLENT F = FAIR P = POOR

N = NOT APPLICABLE

TYPES

CONVENTIONAL UNIJUNCTION (UJT) AND PROGRAMMABLE UNIJUNCTION TRANSISTORS (PUT)

- Unilateral triggers requiring pulse transformers.
- See unijunctions, switches, & triggers selector guide. Specification No. 60.53

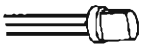
DIAC (ST2)

- Diffused silicon bi-directional trigger diode.
- Specification sheet No. 175.30

SILICON ASSYMMETRICAL SWITCH (ST4)

- Assymmetrical trigger device for hysteresis free lamp dimming circuits.
- Specification sheet No. 175.32

SILICON BILATERAL SWITCH (SBS)



- Low voltage triac trigger, two silicon unilateral switches connected in inverse parallel.
- Specification sheet No. 65.25

UNIJUNCTIONS, TRIGGERS AND SWITCHES

Since the introduction of the commercial silicon unijunction transistor in 1956, General Electric has continued developing an extensive line of negative resistance threshold and four-layer switch devices. Each of these devices can be used as a power thyristor trigger, and each offers a special advantage for a particular trigger function. In addition, each can be used for various non-trigger applications.

The features—both in design and characteristics—which you receive with these products are concisely defined for each series:

TYPES

CONVENTIONAL UNIJUNCTIONS 2N489-494—proved reliability, MIL spec version.
2N2646-47—low cost, proved hermetic sealed device.

PROGRAMMABLE UNIJUNCTION TRANSISTOR (PUT)—variable threshold, low cost, fast switching speed, and circuit adjustable electrical characteristics.

COMPLEMENTARY UNIJUNCTION TRANSISTOR—ultimate in temperature stability for timing and oscillator applications.

SILICON ASYMMETRICAL SWITCH (SAS)— asymmetrical voltage threshold, gate triggered

SILICON UNILATERAL SWITCH (SUS)—a stable fixed low voltage threshold, low cost, high performance "4-layer diode."

SILICON BILATERAL SWITCH (SBS)—low voltage triac trigger, two silicon unilateral switches connected back to back.

SILICON CONTROLLED SWITCH (SCS)—high triggering sensitivity, 4-lead capability for multiple loads or dv/dt suppression.

APPLICATIONS

Use	Device	Unijunctions: Conventional		Unijunctions: Complementary	Unijunctions: Programmable	Triggers		
		2N489-94, 2N2417-22 2N1671, 2N2160	2N2646 2N2647	DSK1 DSK2	2N6027 2N6028	SUS 2N4983-90	SBS 2N4991-93	SAS D13H
Trigger for SCR's	DC, Lo Cost	P	F	P	E	E	E	E
	DC, Hi Perf.	F	F	F	E	F	F	F
	DC, Volt Regulator	P	P	F	F	E	E	E
	DC, Inverter	F	F	E	E	F	F	F
	DC, Hi $\Delta I/\Delta T$	P	P	P	E[1]	P	P	P
	AC, φ, Hi Perf.	F	F	E	E[1]	F	F	F
	AC, φ, Hi I	F	F	F	E	P	P	P
	AC, Lo RFI	P	P	F	F	E	E	E
	AC, φ, Lo Cost	P	F	P	E	E	E	E
Timers	>1 hr.	F[1]	P	F[1]	E[1]	N	N	N
	>1 min, Lo Cost	P	F	P	E	N	N	N
	>1 min, Stable	F	P	E	P	N	N	N
	<1 min, Lo Cost	P	F	P	E	F	F	F
	<1 min, Stable	F	P	E	P	F	N	N
	<10V	P	P	F	E	N	N	N
	10V-25V	E	E	E	E	F	F	F
	>25V	P	P	P	E	F	F	F
Oscillators	Stability	F	F	E	F	N	N	N
	Cost	P	F	P	E	N	N	N
	Adjust, Range	E	E	F	F[1]	N	N	N
Markets	Military	E	P	F	F[2]	P	P	P
	Hi-Rel	E	P	E	F[2]	F	F	P
	Economy	P	F	P	E	E	E	E

E = Excellent, F = Fair, P = Poor, N = Not Applicable
[1] With additional circuitry
[2] Hermetic version 2N6116-18

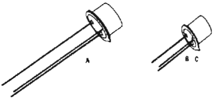
CONVENTIONAL UNIJUNCTIONS

General Electric produces a very broad line of standard UJT's. The TO-5 ceramic disc bar structure device has been the workhorse of the unijunction industry for over 10 years. MIL versions are available on the 2N489-494 series. Equivalent types are available in TO-18 packages where small size is required.

The cube structure TO-18 series offers excellent value for those requiring proved, low cost units.

Applications

Oscillators	SCR Triggers
Timers	Frequency Divider
Sawtooth Generators	Stable Voltage Sensing



	GE Type	R_{BBO} Interbase Resistance @ V_{BB} = 3V I_E = 0 (KΩ)	η Intrinsic Standoff Ratio @ V_{BB} = 10V	I_V Valley Current Min. (mA)	I_P Peak Point Emitter Current Max. (μA)	I_{EO} Emitter Reverse Current Max. (μA)	I_{EO} T_J = 25°C @ V_{B2E}	V_{OB1} Base One Peak Pulse Voltage Min. (V)	Comments	Package	Specification No.
TO-5 Bar Structure	2N489	4.7- 6.8	.51-.62	8	12	2	60	—		A	60.10
	2N489A *				12	2	60	3			
	2N489B				6	0.2	30	3			
	2N490	6.2- 9.1	.51-.62	8	12	2	60	—			60.10
	2N490A *				12	2	60	3			
	2N490B				6	0.2	30	3			
	2N490C				2	.02	30	3	"A" versions are guaranteed in recommended circuit to trigger GE SCR's over range T_A = −55°C to 125°C.		60.11
	2N491	4.7- 6.8	.56-.68	8	12	2	60	—		A	60.10
	2N491A *				12	2	60	3			
	2N491B				6	0.2	30	3			
	2N492	6.2- 9.1	.56-.68	8	12	2	60	—		A	60.10
	2N492A *				12	2	60	3			
	2N492B				6	0.2	30	3			
	2N492C				2	.02	30	3	"B" versions in addition to SCR triggering guarantees lower I_{EO} and I_P for long timing periods with a smaller capacitor.		60.11
	2N493	4.7- 6.8	.62-.75	8	12	2	60	—		A	60.10
	2N493A *				12	2	60	3			
	2N493B				6	0.2	30	3			
	2N494	6.2- 9.1	.62-.75	8	12	2	60	—		A	60.10
	2N494A *				12	2	60	3			
	2N494B				6	0.2	30	3			
	2N494C				2	.02	30	3			60.11
	2N1671	4.7- 9.1	.47-.62	8	25	12	30	—	Industrial types.	A	60.50
	2N1671A				25	12	30	3			
	2N1671B				6	0.2	30	3			
	2N1671C				2	.02	30	3			
	2N2160	4.0-12.0	.47-.80	8	25	12	30	3	General purpose—low cost.	A	60.53
TO-18 Bar Structure	2N2417	4.7- 6.8	.51-.62	8	12	2	60	—		B	60.10
	2N2417A				12	2	60	3			
	2N2417B				6	0.2	30	3			
	2N2418	6.2- 9.1	.51-.62	8	12	2	60	—		B	60.10
	2N2418A				12	2	60	3			
	2N2418B				6	0.2	30	3	"A" versions are guaranteed in recommended circuit to trigger GE SCR's over range T_A = −55°C to 125°C.		
	2N2419	4.7- 6.8	.56-.68	8	12	2	60	—		B	60.10
	2N2419A				12	2	60	3			
	2N2419B				6	0.2	30	3			
	2N2420	6.2- 9.1	.56-.68	8	12	2	60	—		B	60.10
	2N2420A				12	2	60	3			
	2N2420B				6	0.2	30	3	"B" versions in addition to SCR triggering guarantees lower I_{EO} and I_P for long timing periods with a smaller capacitor.		
	2N2421	4.7- 6.8	.62-.75	8	12	2	60	—		B	60.10
	2N2421A				12	2	60	3			
	2N2421B				6	0.2	30	3			
	2N2422	6.2- 9.1	.62-.75	8	12	2	60	—		B	60.10
	2N2422A				12	2	60	3			
	2N2422B				6	0.2	30	3			
	D5E514	4.7- 9.1	.47-.62	8	25	12	30	—	TO-18 versions of 2N1671 industrial series.	B	—
	D5E515				25	12	30	3			
	D5E516				6	0.2	30	3			
	—				2	.02	30	3			
TO-18 Cube Structure	2N2646	4.7- 9.1	.56-.75	4	5	12	30	3	General purpose.	C	60.62
	2N2647	4.7- 9.1	.68-.82	8	2	0.2	30	6	For long timing periods and triggering high current SCR's.	C	60.62
	D5E-43	4.7- 9.1	.68-.82	5	2	1	30	5	General purpose.	C	60.17
	D5E-44	4.7- 9.1	.68-.82	4	5	12	30	4	General purpose—low cost.	C	60.13
	2N2840	4.7- 9.1 [1]	.62 Typical	.2	10	1	30	—	For 1.5 volt applications.	C	60.56

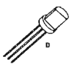
* JAN & JANTX types available
[1] V_{BB}=1.5V

PROGRAMMABLE UNIJUNCTIONS (PUT—D13T SERIES)

The 2N6028 is specifically characterized for long interval timers and other applications requiring low leakage and low peak point current. The 2N6027 has been characterized for general use where the low peak point current of the 2N6028 is not essential.

Applications:

- SCR Trigger
- Pulse & Timing Circuits
- Oscillators
- Sensing Circuits
- Sweep Circuits



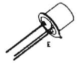
Outstanding Features of the PUT:

- Low Cost
- Low Leakage Current
- Low Peak Point Current
- Low Forward Voltage
- Fast, High Energy Trigger Pulse
- Programmable η
- Programmable R_{BB}
- Programmable I_p
- Programmable I_v
- Planar Passivated Structure

JEDEC Types	Gate to Anode Reverse Voltage Max. (V)	DC Anode Current Max. (mA)	Peak Anode Current 20 μsec. 1% D.C. Max. (A)	I_{GAO} Leakage Current @ 40V Max. (nA)	Pk. Point Current Max. @ R_G = 10 k (μA)	Pk. Point Current Max. @ R_G = 1 Meg. (μA)	I_V Valley Current Min. @ R_G = 10 k (μA)	V_O Output Voltage Min. (V)	t_r Pulse Rate of Rise Max. (nsec.)	Package	Specification No.
2N6027	40	150	2	10	5	2	70	6	80	D [1]	60.27
2N6028	40	150	2	10	1	.15	25	6	80	D [2]	60.27

[1] Hermetic version of 2N6027: 2N6116
[2] Hermetic version of 2N6028: 2N6118

COMPLEMENTARY UNIJUNCTIONS (D5K SERIES)

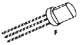


The D5K offers the ultimate in unijunction stability and uniformity. Low frequency oscillators and timers can be built using the D5K with better than 1.0% accuracy over extended temperature ranges. The D5K has characteristics like those of a standard unijunction except the currents and voltages applied to it are of opposite polarity than those of the standard devices.

GE Type	R_{BO} Interbase Resistance @ I_E = 0.1mA k Ω	η Intrinsic Standoff Ratio	I_V Valley Current Min. (mA)	I_P Peak Point Emitter Current Max. (μA)	I_{EO} Emitter Reverse Current Max. (nA)	V_O Peak Pulse Voltage Min. (V)	Operating Temp. Range Top (°C)	Frequency Stability from 25°C —55 to +150°C %	Package	Specification No.
D5K1	5.5-8.2	.58-.62	1	5	10	3.5	—55 to +150	1.0	E	60.15
D5K2	5-15	.58-.62	1	15	10	3.5	—55 to +100	2.0	E	60.16

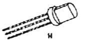
SILICON ASYMMETRICAL SWITCH (SAS)

A Monolithic Integrated Switch for Bistable Application Where Stability of Switching Voltage is Required.

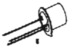


GE Type	V_{S2} Switching Voltage Min. (V)	V_{S2} Switching Voltage Max. (V)	V_{S1} Switching Voltage Min. (V)	V_{S1} Switching Voltage Max. (V)	I_{S2}, I_{S1} Switching Current Max. (μA)	V_{F2} Forward Voltage Drop @ 100 mA Max. (V)	V_{F1} Forward Voltage Drop @ 100 mA Min. (V)	V_{F1} Forward Voltage Drop @ 100 mA Max. (V)	Temperature Coefficient of V_S —55 to +125°C Typical	Package	Specification No.
D13H1	7	9	14	18	80	1.6	7	10	.03%/°C	F	65.34

SILICON UNILATERAL AND BILATERAL SWITCHES (SUS, SBS)



H



G

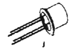
The General Electric SUS is a silicon, planar monolithic integrated circuit having thyristor electrical characteristics closely approximating those of an "ideal" four-layer diode. The device is designed to switch at 8 volts with a typical temperature coefficient of 0.02%/°C. A gate lead is provided to eliminate rate effect, obtain triggering at lower voltages, and to obtain transient-free waveforms.

The SBS is a bilateral version of the forward characteristics of the SUS. It provides excellently matched characteristics in both directions with the same low temperature coefficient.

	GE Type	V_{ACR} Reverse Voltage Max. (V)	I_F Continuous Forward Current Max. (mA)	I_f Peak Recurrent Forward Current @ 100°C, 10 µs, 1% duty cycle (A)	P_T Dissipation (mW)	T_C Temperature Coefficient of Switching Voltage (%/°C)	V_S Switching Voltage Min. (V)	V_S Switching Voltage Max. (V)	I_S Switching Current Max. (µA)	I_B Forward Blocking Current @ 5V (µA)	V_F Forward Voltage @ 200mA (V)	I_H Holding Current (mA)	V_O Peak Pulse Voltage Min. (V)	Package	Specification No.
Unilateral	2N4987	30	175	1.0	300	—	6	10	500	1.0	1.5	1.5	3.5	G	65.25
	2N4988	30	200	1.0	350	±.05	7.5	9	150	0.1	1.5	.5	3.5		65.25
	2N4989	30	200	1.0	350	±.02	7.5	8.2	300	0.01	1.5	1.0	3.5		65.25
	2N4990	30	175	1.0	300	—	7	9	200	0.1	1.5	.75	3.5		65.25
	2N4983	30	175	1.0	300	—	6	10	500	1.0	1.5	1.5	3.5	H	65.26
	2N4984	30	200	1.0	350	±.05	7.5	9	150	0.1	1.5	.5	3.5		65.26
	2N4985	30	200	1.0	350	±.02	7.5	8.2	300	0.01	1.5	1.0	3.5		65.26
	2N4986	30	175	1.0	300	—	7	9	200	0.1	1.5	.75	3.5		65.26
Bilateral	2N4991	—	175	1.0	300	—	6	10	500	1.0	1.7	1.5	3.5	H	65.31
	2N4992	—	200	1.0	350	±.05	7.5	9	120	0.1	1.7	.5	3.5		65.32
	2N4993	—	175	1.0	300	—	6	10	500	1.0	1.7	1.5	3.5	G	65.30

SILICON CONTROL SWITCHES (SCS)

High triggering sensitivity. 4 lead capability for multiple load or dv/dt suppression.



J

GE Type	V_{AK} Anode Voltage Blocking (V)	I_F Continuous DC Forward Current (mA)	Peak Recurrent Forward Current @ 100µsec (A)	Cathode Gate Peak Current (mA)	P_T (mW)	Cutoff Characteristics: I_R @ V_{AK} R_{GK}=10KΩ 150°C (µA)	Conducting Characteristics: I_H R_{GK}=10KΩ (mA)	Max. Gate Ratings: V_{GK} I_{GK}=20µA (V)	Max. Gate Ratings: V_{GA} I_{GA}=1µA (V)	Gate Triggering Characteristics: I_{GTK} @ V_{AK}=40V, R_L=800Ω, R_{GA}=∞ (µA)	Gate Triggering Characteristics: V_{GTK} (V)	Gate Triggering Characteristics: I_{GTA} @ V_{AK}=40V, R_L=800Ω, R_{GK}=10K (mA)	Gate Triggering Characteristics: V_{GTA} (V)	Package	Specification No.
3N81	65	200	1.0	500	400	20	1.5	5	65	1.0	.4 to .65	1.5	−.4 to −.8	J	65.16
3N82	100	200	1.0	500	400	20	1.5	5	100	1.0	.4 to .65	1.5	−.4 to −.8	J	65.16
3N83	70	50	0.1	50	200	20*	4.0 †	5	70	150 †	.4 to .80	—	—	J	65.17
3N84	40	175	0.5	100	320	20*	2.0	5	40	10	.4 to .65	—	—	J	65.18
3N85	100	175	0.5	100	320	20*	2.0	5	100	10	.4 to .65	—	—	J	65.18
3N86	65	200	1.0	500	400	20	0.2	5	65	1.0	.4 to .65	0.1	−.4 to −.8	J	65.19

* Measured @125°C. † Measured in special test circuit (See specification sheet).

ADDITIONAL REFERENCE PUBLICATIONS

ORDER BY PUBLICATION NUMBER

- 90.10 The Unijunction Transistor Characteristics and Applications
- 90.12 Unijunction Temperature Compensation
- 90.19 Unijunction Frequency Divider
- 90.70 The D13T—A Programmable Unijunction Transistor
- 90.72 Complementary Unijunction Transistors

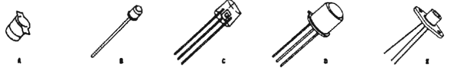
22.5 DETECTORS

General Electric has a full line of Solid State Optoelectronic Products and is interested in assisting you choose products to perform your function with maximum effectiveness and minimum cost.

This Selection Guide contains information on products which have been formally introduced prior to its printing. General Electric has a continuing development program and will be introducing other products throughout the year. Information on these products will be published as they are introduced.

PACKAGES

Package must have a small enough diameter to fit on the proper centers in the case of arrays.
Package must be small enough to offer proper pellet (sensitive area) placement when a small aperture is being used.



SPEED

The device must have a sufficiently fast rise and fall time to see the signal in the case of a moving aperture or a signal from a pulsed source.

SENSITIVITY

Sensitivity is important to generate a signal sufficient to drive a logic gate or other following functions.

SATURATION VOLTAGE

The saturation is very important when the device is being used to drive a logic gate directly.

TYPES

Recommended stocking items in bold

	d	Package Outline	Speed (μs) t_r	t_f	Sensitivity (mA/mW/cm²)	Saturation Voltage	Specification Sheet
L14A800	.060"	A	3	3	.3	.4	55.58
L15E	.087"	B	3	3	0.4	.4	55.56
L14T8	.208"	C			Switches (100 mA)	1.6	55.54
L14E	.208"	C	15	10	.05	.2	55.47
L14G (2N5777)	.208"	C	75	45	2.0	.7	55.46
L14A802	.230"	D	5	5	.7	.4	55.45
L14F	.230"	D	100	100	150	1.0	55.49
L1V	.230"	D	15	25	Switches (175 mA)	2.0	56.41
L8/L9	.370"	E	0.8		Switches (1.6 A Rms)	1.2	190.10

PHOTON COUPLED ISOLATORS

ISOLATION

The device must have sufficient isolation to prevent destruction of the device.

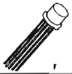
SPEED

The device must be fast enough to pass the signal without distortion.

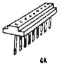
TRANSFER RATIO

Transfer ratio is important in that it can save you an additional stage of amplification.

PACKAGES


F

G


GA

TYPES

Recommended stocking items in bold

	Package	Isolation Voltage (V)	Speed (μs)	Current Transfer Ratio (%)	Specification Sheet
H10A	F	1000	3	50	55.61
H10B	F	1000	100	500	55.62
H10C	F	1000	.6	Switches 1.0 Amp Rms Max.	55.63
PC15-26	G	2500	3	35	3-0159R
PC 4-73	G	2500	100	125	3-0190R

ARRAYS

CENTER TO CENTER SPACING

Element must have proper spacing to be compatible with format to be read.

SPEED

Element must be fast enough to see the moving aperture.

MATCHING FACTOR

Most data formats (i.e. punched papertape, and punched cards) transmit some light when a hole is not present, hence we have two signal levels (an on-signal, and an off-signal). It is important to determine both levels. Once these levels are measured, the required matching factor for the devices in an array can be set, to insure an on-signal from the least sensitive device in the on-state, and an off-signal from the most sensitive device in the off-state.

SENSITIVITY

It is desirable to generate a sufficient signal to drive a logic gate or following functions directly.

SATURATION VOLTAGE

It is necessary that the photo-transistor have a low saturation voltage when it is being used to drive logic directly.

TYPES

Package GA	Number of Elements and Center to Center Spacing No.	Spacing	Speed (μs) t_r	t_f	Matching Factor %	Sensitivity mA/mW/cm²	Saturation Voltage Volts	Specification Sheet
J300	9	.100"	3	3	50	1.0	.4	55.60
J300A	9	.100"	3	3	75	1.0	.4	55.60

Special—Please contact your local GE Electronic Components Sales Office with your requirements on all special arrays.

VISIBLE SOLID STATE LAMPS & DISPLAYS (EMITTERS)

PEAK EMISSION

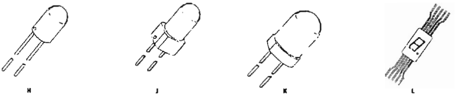
To insure that the film (in film annotation applications) or the eye (in visual applications) are sensitive to the emitted wavelength.

VISIBLE OUTPUT

Millicandella is a measure of the time rate of flow, of visible radiation, out of the device.

PACKAGE

Package is important for proper center to center spacing in linear and matrix arrays.
Package size is also important since the apparent size of the light source is the diameter of the package.



H J K L

VISIBLE TYPES

Recommended stocking items in bold

	Peak Emission Wavelength A	Visible Output Millicandella	Package d	Package l	Outline	Comments	Specification Sheet
SSL212	7000	1.0	.080″	.125″	H		
SSL12	7000	1.0	.095″	.187″	J	Square Base for Linear and Matrix Arrays	
SSL22L	7000	1.5	.230″	.230″	K	Longer Barrell for Panel Mounting (Panel Mount Clip Available)	**
SSL3	5390/9200	80′ Lamberts @ 5390 A 1.0 mW @ 9000 A	.230″	.230″	K		

DISPLAYS

	Peak Emission Wavelength A	Package l	Package w	Outline	Character h	Specification Sheet
SSL140	7000	.400	.220	L	.140″	**
SSL190	7000	.400	.220	L	.190″	

**For Technical Information Contact: General Electric
Miniature Lamp Dept. Inquiry Bureau #482
Nela Park, Cleveland, Ohio 44112

INFRARED SOLID STATE LAMPS (EMITTERS)

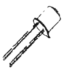
POWER OUTPUT

Infrared Solid State Lamps are used to irradiate silicon photo-detectors. The output from the detector is proportional to the radiant flux density incident upon its active area, hence power output is the most important parameter of the Infrared SSL.

PACKAGE

The package must have a small diameter for proper center to center spacing in arrays.

M



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SPEED

The speed of the device is important in pulsed operation, primarily for signal coupling over large distances. In most applications the speed of the detector will be the limiting parameter rather than that of the SSL.

INFRARED TYPES

Recommended stocking items in bold

	Power Output (mW)	Package d	Package Outline	Speed (μs) t_r	Speed (μs) t_f	Specification Sheet
SSL15	0.5	.097"	M	.7	.5	
SSL315	1.0	.097"	M	.7	.7	
SSL4	0.4	.230"	N	.005	.005	
SSL34	0.9	.230"	N	.010	.010	
SSL54	1.0	.230"	N	.010	.010	
SSL5A	1.5	.230"	N	.3	.2	**
SSL5B	2.3	.230"	N	.3	.2	
SSL5C	2.9	.230"	N	.3	.2	
SSL55B	4.8	.230"	N	.3	.2	
SSL35	5.5	.230"	N	.5	.5	
SSL55L	6.0	.230"	N	.3	.2	

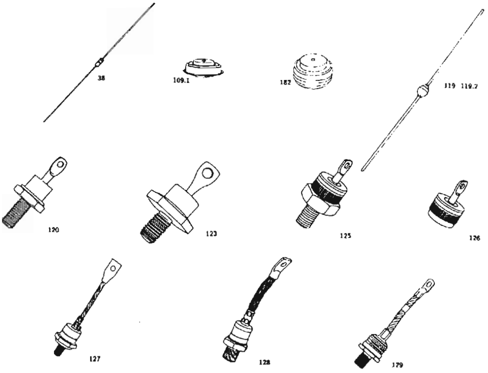
**For Technical Information Contact: General Electric
Miniature Lamp Dept. Inquiry Bureau #482
Nela Park, Cleveland, Ohio 44112

22.6 SILICON RECTIFIERS

THE INDUSTRY'S BROADEST LINE OF POWER RECTIFIERS—.250 TO 1500 AMPERES, UP TO 3000 VOLTS

- CURRENT/VOLTAGE RATINGS
- PACKAGING
- MOUNTING AND COOLING
- HIGH-SPEED FAST RECOVERY
- TRANSIENT SELF-PROTECTION
- GENERAL PURPOSE

PACKAGES



SILICON RECTIFIERS .25 TO 3 AMPERES

JEDEC		—	—	—	—	1N5059-62	1N4245-49	—	—	1N5624-27	—	—
GE TYPE		DT230	MPR10-15	A14PD	A114PD2	A14A-P	—	GER4001-7	A114A-M	—	A15A-M	A115A-M
SPECIFICATIONS												
$I_{F(AV)}$	(A)	.25	.5	1	1	1	1	1	1	3	3	3
	@ T_A(°C)	50	100	75	75	100	55	75	55	70	70	55
$V_{RM(rep)}$ — Max. repetitive peak reverse voltage (V)												
	50	DT230F	—	—	—	A14F	—	GER4001	A114F	—	A15F	A115F
	100	DT230A	—	—	—	A14A	—	GER4002	A114A	—	A15A	A115A
	150	DT230G	—	—	—	—	—	—	—	—	—	—
	200	DT230B	—	—	—	1N5059	1N4245 [2]	GER1003	A114B	1N5624	A15B	A115B
	250	DT230H	—	—	—	—	—	...	—	—	...	—
	300	—	—	—	—	A14C		—	A114C	—	A15C	A115C
	400	—	—	—	—	1N5060	1N4246 [2]	GER4004	A114D	1N5625	A15D	A115D
	500	—	—	—	—	A14E	—	—	A114E	—	A15E	A115E
	600	—	—	—	—	1N5061	1N4247 [2]	GER4005	A114M	1N5626	A15M	A115M
	800	—	—	—	—	1N5062	1N4248 [2]	GER4006	A114N	1N5627	A15N	—
	1000	...	MPR10	—	—	A14P [1]	1N4249	GER4007	—	—	...	—
	1200	—	MPR12	—	—	—	—	—	—	—	—	—
	1400	—	—	A14PD	A114PD2	—	—	—	—	—	—	—
	1500	—	MPR15	—	—	—	—	—	—	—	—	—
$I_{FM(surge)}$	Max. peak one cycle, non-recurrent surge current (60 Hz sine wave, 1 phase operation) @ max. rated load conditions (A)	5	25	40	40	50	25	30	40	125	125	110
I^2t	Max. non-repetitive for 8.3 msec. (A^2sec)	—	3	3.5	3.5	4	4	—	3.5	25	25	20
T_J	Operating junction temperature range (°C)	−65 to 150	−55 to 175	−65 to 150	−65 to 150	−65 to 175 [1]	−65 to 160	−65 to 175	−65 to 125	−65 to 175	−65 to 175	−65 to 150
T_{stg}	Storage temperature range (°C)	65 to 200	−65 to 175	−65 to 175	−65 to 175	−65 to 175	−65 to 200	−65 to 175	−65 to 175	−65 to 200	−65 to 175	−65 to 175
V_{FM}	Max. peak forward voltage drop @ rated $I_{F(AV)}$ (1 phase operation)	1.1	1.8	1.1	1.1	1.0	1.2@ +55°C	1.1	1.1	1.0	1.0	1.0
t_{rr}	Max. reverse recovery time (μsec)	0.3	5	—	20	6	5	—	0.2	5	5	0.2
PACKAGE OUTLINE NO.		38	119	119	119	119	119	119	119	119 2	119.2	119 2
SPECIFICATION SHEET NO.		130.25	130.53	130.55	130.69	130.55	130.56	130.66	130.54	130.59	130.58	130.67

NOTE:
[1] Average forward current 1 amp. @ T_A=90°C. Junction, operating and storage temperature range −65 to +185°C.
[2] JAN & JANTX types available

SILICON RECTIFIERS 5 TO 12 AMPERES

JEDEC		1N1612-16	1N1341A-48A	1N3987-90	1N3879-83	1N1199A-1206A 1N3670A-73A 1N5331	1N3889-93			1N4510-11
GE TYPES		—	—	—	—	—	—	A28F-D	A129E-PB	—
SPECIFICATIONS										
$I_{F(AV)}$	(A)	5	6	6	6	12	12	12	12	12
	@ T_C = (°C)	150	150	150	100	150	100	135	65	135
V_{RRM} — Max. repetitive peak reverse voltage (V)		—	—	—	—	—	—	—	—	—
	50	1N1612	1N1341A	—	1N3879	1N1199A	1N3889	A28F	—	--
	100	1N1613	1N1342A	—	1N3880*	1N1200A	1N3890*	A28A	—	—
	150	—	1N1343A	—	—	1N1201A	—		—	—
	200	1N1614*	1N1344A		1N3881*	1N1202A*	1N3891*	A28B	—	—
	300	—	1N1345A	—	1N3882	1N1203A	1N3892	A28C	—	—
	400	1N1615*	1N1346A	—	1N3883*	1N1204A*	1N3893*	A28D	—	
	500	—	1N1347A	—	—	1N1205A	—	—	A129E	—
	600	1N1616*	1N1348A	—	—	1N1206A*	—	—	A129M	—
	700	—	—	1N3987	—	1N3670A	—	—	—	—
	800	—		1N3988	—	1N3671A	—	—	A129N	—
	900	—	—	1N3989	—	1N3672A	—	—	—	—
	1000	—	—	1N3990	—	1N3673A*	—	—	A129P	1N4510
	1200	—	—	—	—	1N5331	—	—	A129PB	1N4511
$I_{FM\,(surge)}$	Max. peak one cycle, non-recurrent surge current (60 Hz sine wave, 1 phase operation) @ max. rated load conditions (A)	150	150	150	75	240	150	240	150	240
I^2t	Max. non-repetitive for 1.0 msec (A^2sec.)	25	25	25	—	60	—	67	60	67
T_J	Operating junction temperature range (°C)	−65 to +190	−65 to +200	−65 to +200	−65 to +150	−65 to +200	−65 to +150	−65 to +175	−40 to +125	−65 to +175
T_{stg}	Storage temperature range (°C)	−65 to +200	−65 to +200	−65 to +200	−65 to +175	−65 to +200	−65 to +175	−65 to +175	−40 to +125	−65 to +200
$R_{\theta JC}$	Max. thermal resistance, junction-to-case (°C/W)	7.0	4.25	4.25	2.5	2.5	2.0	2.0	3.25	2.0
V_{FM}	Max. peak forward voltage drop @ rated $I_{F(AV)}$ (1 phase operation) (V)	1.3	1.4	1.4	1.4	1.1	1.4	1.5	1.5	1.4
	@ T_C = (°C)	25	25	25	25	150	25	135	64	135
t_{rr}	Max. reverse recovery time (nsec)	—	—	—	200	—	200	300	500	--
PACKAGE OUTLINE NO.		120	120	120	120	120	120	120	120	120
SPECIFICATION SHEET NO.		140.15	140.10	--	140.12	140.20	140.22	140.23	140.25	140.24

*JAN & JANTX types available

SILICON RECTIFIERS 20 TO 40 AMPERES

JEDEC		1N248B-250B	1N1195A-98A	1N2154-60	1N1183-90 1N3765-68 1N5332	1N1183A-90A	1N3899-3903	1N3909-13	1N4529-30	1N3208-14		
GE TYPE										A40F-M	A44F-M	A139
SPECIFICATIONS												
$I_{F(AV)}$	Max. average forward current (1 phase operation) (A)	20	20	25	35	40	20	30	35	20	20	25
	@ T_C = (°C)	150	150	145	140	150	100	100	115	110	110	75
$V_{RM(rep)}$	—Max. repetitive peak reverse voltage (V)											
	50	1N248B	—	1N2154	1N1183	1N1183A	1N3899	1N3909*	—	1N3208 A40F	A44F	—
	100	1N249B*	—	1N2155	1N1184*	1N1184A	1N3900	1N3910*	—	1N3209 A40A	A44A	—
	150	—	—	—	1N1185	1N1185A	—	—	—	—	—	—
	200	1N250B*	—	1N2156	1N1186*	1N1186A	1N3901	1N3911*	—	1N3210 A40B	A44B	—
	300	—	1N1195A	1N2157	1N1187	1N1187A	1N3902	1N3912*		1N3211 A40C	A44C	—
	400	—	1N1196A	1N2158	1N1188*	1N1188A	1N3903	1N3913*	—	1N3212 A40D	A44D	—
	500	—	1N1197A	1N2159	1N1189	1N1189A	—	—	—	1N3213 A40E	A44E	A139E
	600	—	1N1198A	1N2160	1N1190	1N1190A	—	—	—	1N3214 A40M	A44M	A139M
	700	—	—	—	1N3765	—	—	—	—	—	—	—
	800	—	—	—	1N3766	—	—	—	—	—	—	A139N
	900	—	—	—	1N3767	—	—		—	—	—	—
	1000	—	—	—	1N3768	—	—	—	1N4529	—	—	A139
	1200	—	—	—	1N5332	—	—	—	1N4530	—	—	A139PB
$I_{FM(surge)}$	Max. peak one cycle, non-recurrent surge current (60 Hz sine wave, 1 phase operation) @ max. rated load conditions (A)	350	350	400	500	800	275	300	500	300	300	400
I^2t	Max. I^2t rating (non-repetitive for 8.3 msec.) A^2 sec	—	—	250	500	...	—	—	500	100	100	500
T_J	Operating junction temperature range (°C)	−65 to +175	−65 to +175	−65 to +200	−65 to +200	−65 to +200	−65 to +150	−65 to +150	−65 to +175	−65 to +175	−65 to +175	−40 to +125
T_{stg}	Storage temperature range (°C)	−65 to +175	−65 to +175	−65 to +200	−65 to +200	65 to +200	−65 to +175	−65 to +175	−65 to +200	65 to +175	−65 to +175	−40 to +200
θ_{J-C}	Max. thermal resistance, junction-to-case (°C/W)	1.2	1.2	1.4	1.0	1.0	1.5	1.0	1.0	1.5 Typical	1.5 Typical	1.0
V_{FM}	Max. peak forward voltage drop @ rated $I_{F(AV)}$ (1 phase operation) (V)	—	—	—	1.7	1.3	1.4	1.4	1.4	1.35 Typical	1.35 Typical	1.85
	@ T_{CM}(°C)	150	150	145	140	25	25	25	115	25	25	75
T_{rr}	Max. reverse recovery time (nsec)	—	—	—	—	—	200	200	—	—	—	500
PACKAGE OUTLINE NO.		123	123	123	123	123	123	123	123	125	126	124
SPECIFICATION SHEET NO.		140.28	140.30	140.40	140.50	140.50	140.47	140.48	140.37	140.32	140.33	140.26

* JAN & JANTX types available

SILICON RECTIFIERS 100-275 AMPERES

JEDEC TYPE		1N3289-96	1N3260-73	1N3735-42				1N4044-56
GE TYPE		A70B-PB		A90A-PB	A96A-P	A396A-P	A291PC-PM	
SPECIFICATIONS								
$I_{F(AV)}$	Max. average forward current (1 phase operation)	100	160	250	250	250	250	275
	@ T_C = (°C)	130	125	130	70	70	135	120
$V_{RRM(rep)}$ — Max. repetitive peak reverse voltage (V)		—	—	—	—	—	—	—
	50	—	1N3260	—	—	—	—	1N4044
	100	—	1N3261	A90A, 1N3735	A96A	A396A	—	1N4045
	150	—	1N3262	—	—	—	—	1N4046
	200	A70B, 1N3289	1N3263	A90B, 1N3736	A96B	A396B	—	1N4047
	250	—	1N3264	—	—	—	—	1N4048
	300	A70C, 1N3290	1N3265	A90C, 1N3737	A96C	A396C	—	1N4049
	350	—	1N3266	—	—	—	—	—
	400	A70D, 1N3291	1N3267	A90D, 1N3738	A96D	A396D	—	1N4050
	500	A70E, 1N3292	1N3268	A90E, 1N3739	A96E	A396E	—	1N4051
	600	A70M, 1N3293	1N3269	A90M, 1N3740	A96S	A396M	—	1N4052
	700	A70S	1N3270	A90S	A96M	A396S	—	1N4053
	800	A70N, 1N3294	1N3271	A90N, 1N3741	A96N	A396N	—	1N4054
	900	A70T,	1N3272	A90T	A96T	A396T	—	1N4055
	1000	A70P, 1N3295	1N3273	A90P, 1N3742	A96P	A396P	—	1N4056
	1100	—	—	A90PA	—	—	—	—
	1200	A70PB, 1N3296	—	A90PB	—	—	—	—
	1300	—	—	—	—	—	A291PC	—
	1400	-	—	—	—	—	A291PD	—
	1500	—	—	—	—	—	A291PE	—
	1600	—	—	—	—	—	A291PM	—
$I_{FM(surge)}$	Max. peak one cycle, non-recurrent surge current (60 Hz sine wave, 1 phase operation) @ max. rated load conditions (A)	1600	2000	4500	3300	3300	4500	5000
I^2t	Max. non-repetitive for 8.3 msec. (A^2sec)	10,000	16,000	84,000	43,000	43,000	84,000	100,000
T_J	Operating junction temperature range (°C)	−40 to +200	−55 to +190	−40 to +200	−40 to +125	−40 to +125	−40 to +200	−65 to +190
T_{stg}	Storage temperature range (°C)	−40 to +200	55 to +190	−40 to +200	−40 to +125	−40 to +125	−40 to +200	−65 to +190
θ_{J-C}	Max. thermal resistance, junction-to-case (°C/W)	.4	.3	.18	.18	.18	.15	.18
V_{FM}	Max. peak forward voltage drop @ rated $I_{F(AV)}$ (1 phase operation)	1.15	1.6	1.3	1.25	1.25	1.0	1.35
	@ T_C = (°C)	25	125	130	25	25	25	120
Q_{RR}	Max. reverse recovered charge (μC)	—	—	—	19	19	—	—
PACKAGE OUTLINE NO.		127	128	128	128	109.1	129	128
SPECIFICATION SHEET NO.		145.15	145.28	145.30	145.55	145.71	145.58	145.32

SILICON RECTIFIERS 400-1500 AMPERES

GE TYPE		A390A-PB	A295A-PN	A500P-LP	A540A-L	A570A-P
SPECIFICATIONS						
$I_{FM(AV)}$	Max. average forward current (1 phase operation) (A)	400	500	740	1000	1500
	@ T_C=(°C)	145	130	100	100	80
$V_{RM(rep)}$ — Max. repetitive peak reverse voltage (V)						
	100	A390A	—	—	A540A	A570A
	200	A390B	A295B	—	A540B	A570B
	300	A390C	A295C	—	A540C	A570C
	400	A390D	A295D	—	A540D	A570D
	500	A390E	A295E	—	A540E	A570E
	600	A390M	A295M	—	A540M	A570M
	700	A390S	A295S	—	A540S	A570S
	800	A390N	A295N	—	A540N	A570N
	900	A390T	A295T	—	A540T	A570T
	1000	A390P	A295P	A500P	A540P	A570P
	1100	A390PA	A295PA	A500PA	A540PA	—
	1200	A390PB	A295PB	A500PB	A540PB	—
	1300	—	A295PC	A500PC	A540PC	—
	1400	—	A295PD	A500PD	A540PD	—
	1500	—	A295PE	A500PE	A540PE	—
	1600	—	A295PM	A500PM	A540PM	—
	1700	—	A295PS	A500PS	A540PS	—
	1800	—	A295PN	A500PN	A540PN	—
	1900	—	—	A500PT	A540PT	—
	2000	—	—	A500L	A540L	—
	2100	—	—	A500LA	—	—
	2200	—	—	A500LB	—	—
	2300	—	—	A500LC	—	—
	2400	—	—	A500LD	—	—
	2500	—	—	A500LE	—	—
	2600	—	—	A500LM	—	—
	2700	—	—	A500LS	—	—
	2800	—	—	A500LN	—	—
	2900	—	—	A500LT	—	—
	3000	—	—	A500LP	—	—
$I_{FM(surge)}$	Max. peak one cycle, non-recurrent surge current (60 Hz sine wave, 1 phase operation) @ max. rated load conditions (A)	4500	7000	8400	10,000	15,000
I^2t	Max. non-repetitive for 8.3 msec (A^2sec)	84,000	200,000	270,000	400,000	920,000
T_J	Operating junction temperature range (°C)	−40 TO +200	−40 TO +200	−40 TO +200	−40 TO +200	−40 TO +200
T_{stg}	Storage temperature range (°C)	−40 TO +200	−40 TO +200	−40 TO +200	−40 TO +200	−40 TO +200
θ_{J-C}	Max. thermal resistance, junction-to-case (°C/W)	.15	.12	.06	.06	.053
V_{FM}	Max. peak forward voltage drop @ rated $I_{F(AV)}$ (1 phase operation)	1.15	1.1	1.25	1.15	1.0
	@ T_{CM}(°C)	25	25	25	150	25
PACKAGE NO.		109.1	129	182	182	182
SPECIFICATION SHEET NO.		145.70	145.60	145.78	145.80	145.85

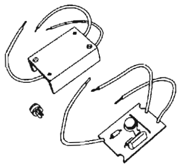
22.7 CIRCUIT ASSEMBLIES

SPECIFY GE SOLID-STATE SUB-ASSEMBLIES FOR A WIDE VARIETY OF CUSTOMER APPLICATIONS

- variable voltage AC controls
- AC motor speed controls
- static switching
- zero-voltage switching AC power controls
- temperature controls
- thyratron and high voltage rectifier tube replacements

"S100"—STANDARD TRIAC CIRCUIT SUB-ASSEMBLIES

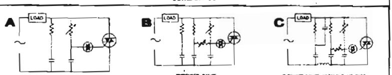
- Available in ratings of 6, 10 and 15 amperes (RMS) at 120 or 240 volts (RMS), the seven circuit configurations offer 42 different sub-assemblies in one "family" package type (1 x 2 x 3 inches).
- As circuit diagram titles imply, the variations allow usage in a wide variety of applications where the ability to vary applied voltage is desired. Such usage includes a simple voltage control, shaded-pole or permanent split-capacitor type motor speed control, resistance heating control, and many others.



NOMENCLATURE

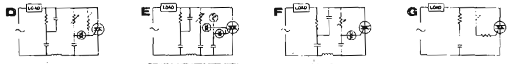
S100	—	—

SCHEMATICS



A: BASIC VARIABLE VOLTAGE ASSEMBLY
B: EXTENDED RANGE VARIABLE VOLTAGE ASSEMBLY
C: EXTENDED RANGE VARIABLE VOLTAGE ASSEMBLY WITH RFI SUPPRESSION

SUFFIX	CURRENT	VOLTAGE
1	6A	120V
2	6A	240V
3	10A	120V
4	10A	240V
5	15A	120V
6	15A	240V



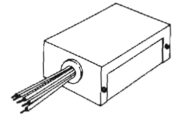
D: COMBINATION STATIC SWITCH AND VARIABLE VOLTAGE CONTROL WITH RFI SUPPRESSION
E: FURNACE BLOWER MOTOR SPEED CONTROL WITH LOW SPEED LIMIT (RFI SUPPRESSED)
F: BASIC VARIABLE VOLTAGE ASSEMBLY WITH RFI SUPPRESSION
G: A-C STATIC SWITCH ASSEMBLY

SPECIFICATION SHEET NOS. 155.20 AND 155.26

"S200"—AC POWER CONTROLLERS

Features:

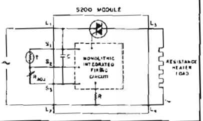
- Available ratings of 10 and 15 amperes (RMS) at 120, 240 and 277 volts (RMS) for controlling resistive loads from 500 to 4150 watts.
- "Zero-Voltage Switching" provides much lower RFI levels than are possible with mechanical contacts.
- All solid-state control for long life and high reliability.
- Capable of operating with a variety of variable resistance sensors such as thermistors, photo-resistors, humidity sensitive devices, etc.
- High input impedance allows use of sensors operating at any point from 5K to 100K ohms.
- Control point repeatability better than ±5.0% of sensor resistance.



NOMENCLATURE

S200A	—

SCHEMATIC



SUFFIX	CURRENT	VOLTAGE
1	10A	120V
2	10A	240V
21	10A	277V
3	15A	120V
4	15A	240V
41	15A	277V

Contact factory for special types

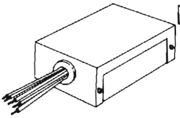
SPECIFICATION SHEET NO. 155.40

"S300"—PHASE CONTROL POWER MODULES WITH FEEDBACK

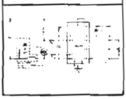
- Available in ratings of 6, 10 and 15 amperes (RMS) at 120 or 240 volts (RMS), for controlling resistive or inductive motor loads up to 3600 watts.
- All solid-state control for long life and high reliability.
- Capable of operating with a variety of variable resistance sensors (thermistors, photo-resistors, humidity sensitive resistors, etc.) as well as DC tachometer signals.
- High input impedance allows use of sensors operating at any point from 5K or 100K ohms.
- High gain trigger circuitry allows wide range of controlled output with small changes in input signal.
- Adjustable gain allows module usage in a variety of AC motor speed control applications.
- Voltage-regulated (zener) control circuit provides stability in supply voltage variations.
- Ambient compensated for stability during temperature fluctuations.
- Inductive load logic allows use with any resistive or lagging power factor motor loads. Minimizes DC components commonly found in phase-controlled inductive load circuits.
- Radio frequency interference suppression network minimizes conducted and radiated RFI.

NOMENCLATURE

S300A	—



SCHEMATIC

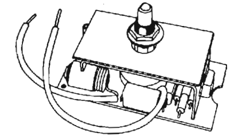


SUFFIX	CURRENT	VOLTAGE
1	6A	120V
2	6A	240V
3	10A	120V
4	10A	240V
5	15A	120V
6	15A	240V

SPECIFICATION SHEET NO. 155.50

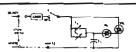
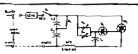
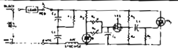
"S400"—FAN MOTOR SPEED CONTROLS

- All models rated at 4.0 amperes, 120 volts (RMS).
- Optimized circuit for primary use as fan motor speed control.
- All solid-state control for long life and high reliability.
- Line voltage compensation feature automatically compensates for input variations of ±12 volts, from 108 to 132 volts. Output variation limited to ±3 volts.
- Capable of operating in a wide variety of applications, within its rating, such as; room air conditioners, window fans, fan and coil air conditioners, exhaust fans, unit heaters and coolers, centrifugal pumps, air curtains, dehumidifiers and vacuum cleaners.
- All units include; a main control potentiometer, a trimmer potentiometer for adjusting minimum output voltage, a self-contained copper heatsink, and UL approved printed circuit board and line switch.



NOMENCLATURE

S400A | —

SCHEMATICS	SUFFIX	FUNCTION
	A1	Basic Power Control
	A1S	Basic Power Control with RFI Suppression
	A1SC	Basic Power Control with RFI Suppression and Line Voltage Compensation

SPECIFICATION SHEET NO. 155.60

TUBE REPLACEMENTS

Solid-state tube replacements are available for high-voltage rectifier tubes, thyratrons, and other special purpose tubes. Since most replacements are for retrofit purposes, it is absolutely essential that they be direct mechanical and electrical replacements. For multi-purpose tubes, such as thyratrons, special care is taken to insure that the solid-state replacement is in fact a true replacement for the particular customer application. Close liaison is maintained between customer engineers and our own to assure proper design.

Standard solid-state thyratron replacements available are:

G-E Type Number	Peak Anode Voltage	Cathode Current	Max. Temp. T_A	May Replace
S26	200V	1.0A RMS @ 30°C	125°C	2D21
S27	200V	1.0A RMS @ 30°C	125°C	2050

SPECIFICATION SHEET NO. 155.10

CUSTOMIZED ASSEMBLIES

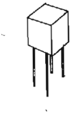
Complete semiconductor circuit assemblies using discrete components are available in a variety of mechanical configurations, including printed circuit boards, potted modules, standard tube shells and many special packages to meet individual customer needs.

SCR and TRIAC motor speed controls. Solid state replacements for thyratron tubes. Static switching. High voltage rectifier stacks. Molded multiple diode modules for computer logic circuits. Molded SCR and transistor modules for computer and other uses. Temperature controllers. Automatic exposure lamp controls for copying machines, etc. Light activated controls.

22.8 RECTIFIER & SCR MODULES

- Most Standard Rectifier Diodes and SCR's, or Combinations of Both, Available with Heatsinks.
- A Wide Variety of Standard Circuit Configurations.
- Special Circuit Configurations Available Upon Request.
- Only Mounting Bolts and Electrical Connections for Power (Trigger Signal also, if SCR's are used) are Required.
- Proven Construction—GE's Long Years of Experience in Designing and Supplying Thousands of Industrial Stacks form the Basis for this Rugged Construction.

2 AMP BRIDGES—UP TO 1000V



- Single phase full wave performance
- 4 hermetically sealed avalanche protected A14 rectifiers
- ½" cube package
- −65°C to +150°C operating temperature range
- 2 amps @ 25°C; 1.6 amps @ 50°C
- 7 standard types:

GEB100	50V
GEB101	100V
GEB102	200V
GEB104	400V
GEB106	600V
GEB108	800V
GEB110	1000V

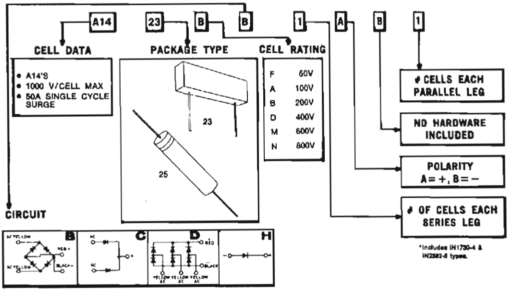
- Other customer package configurations and electrical ratings available

SPECIFICATION SHEET NO. 130.86

SILICON RECTIFIER MODULES—UP TO 3A, 12,000V

Standard modules are offered in single-phase, fullwave bridges, 3-phase bridges, center tap or voltage-doublers, and half-wave series strings, in addition any other circuit configuration desired may be built upon special order.

A1423BB1AB1 is a 200V, 1.5A, Single Phase Full Wave Bridge in a .5 x .25 x 6" Potted Block.



SPECIFICATION SHEET NO. 130.85

Medium & High Current Rectifier Modules

NOMENCLATURE

A2011BC1AD1 is a 200V, single phase center tap, using A20 cells on type 11 Fins, capable of conducting 6.3A ave. per cell at 180º C conduction angle in free air or 9.8A per cell in 2000 linear feet per minute forced air.

A20	11	B	C	1	A	D	1

A20 → CELL DATA; 11 → FIN DATA; B → CELL PEAK REVERSE VOLTAGE RATING; C → CIRCUIT DESIGNATOR

1 → NUMBER OF CELLS IN SERIES EACH LEG

A → POLARITY
A. POSITIVE B. NEGATIVE

D → MECHANICAL FEATURES
A. NO BRACKETS OR MOUNTING FEET.
D. STANDARD
OTHERS AVAILABLE ON SPECIAL ORDER.

1 → NUMBER OF CELLS IN PARALLEL EACH LEG.

CELL DATA / FIN DATA

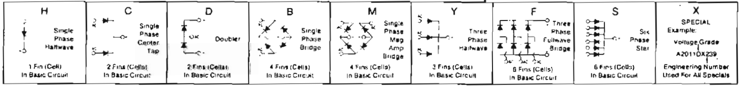
CELL NUMBER	MAX VOLT PER CELL	SINGLE ∿ SURGE-AMPS	Fin 11 FREE CONVECT	Fin 11 2000 LFPM	Fin 12 FREE CONVECT	Fin 12 2000 LFPM	Fin 13 FREE CONVECT	Fin 13 2000 LFPM	Fin 14 FREE CONVECT	Fin 14 2000 LFPM	Fin 15 FREE CONVECT	Fin 15 2000 LFPM
A20	600	150	6.3	9.8								
A25	600	240	9.4	15.5								
A28	400	150			6.3	9.8						
A27	1200	240			12.5	18.4						
A35	600	400	12.5	25.0	20.0	29.0						
A38	1200	500	12.5	25.0	20.0	29.0						
A70	1000	1600	60.4*	99.4*	44.2	80.6	64.4	99.4	78.2	96.9		
A90	1000	4500					83.7	220			160	250

* 3¼" X 3¼" extrusion

CELL PEAK REVERSE VOLTAGE RATING

25V - U	200V - B	500V - E	800V - N	2000V - L	NOTE: FOR PRV RATINGS NOT LISTED
50V - F	300V - C	600V - M	900V - T		USE MULTIPLE LETTERS
100V - A	400V - D	700V - S	1000V - P		FOR i.e. - PB = 1200V

CIRCUIT DESIGNATOR



SCR Medium & High Current Modules

NOMENCLATURE

C10 12BA1AD1 is a 200V, full wave (back to back) bridge connected C10 cells on type 12 Fins, capable of controlling 4.7 amp average per SCR in free air or 6.2 amp average per cell with 1000 linear feet per minute forced air.

C10	12	B	A	1	A	D	1
Cell data	Fin data	Cell peak reverse voltage rating	Circuit designator	Number of cells in series each leg	Polarity & minor electrical modifications	Mechanical features	Number of cells in parallel each leg

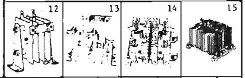
NUMBER OF CELLS IN PARALLEL EACH LEG.

MECHANICAL FEATURES
A. NO BRACKETS OR MOUNTING FEET.
D. STANDARD
OTHERS AVAILABLE ON SPECIAL ORDER.

POLARITY & MINOR ELECTRICAL MODIFICATIONS
A. POSITIVE OR STANDARD
B. NEGATIVE
C.} D.} OTHER DEPENDING ON CIRCUIT

NUMBER OF CELLS IN SERIES EACH LEG

CELL DATA / FIN DATA



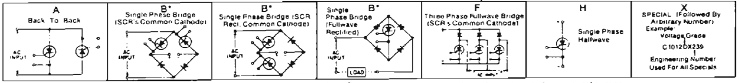
CELL NUMBER	MAX VOLT PER CELL	SINGLE ∿ SURGE-AMPS	COMPATIBLE RECTIFIER	12 FREE CONVECT	12 1000 LFPM	13 FREE CONVECT	13 1000 LFPM	14 FREE CONVECT	14 1000 LFPM	15 FREE CONVECT	15 1000 LFPM
C10	400	60	1N13414-46A	4.7	6.2	4.7	6.2				
C11	600	60	1N1341A-46A	4.7	6.2	3.98	6.0				
C35	800	150	1N2154-59	10.1	16.3	6.3	12.2				
C150	1300	1500	1N3292-96					44.0			
C50	500	1000	1N3289-92					52.0	62.9		
C60	400	1000	1N3289-91					64	78.1		
C180	1300	3500	1N3735-42							106	
C185	500	3500	1N3735-39							106	

CELL PEAK REVERSE VOLTAGE RATING

25V - U	200V - B	500V - E	800V - N	2000V - L
50V - F	300V - C	600V - M	900V - T	
100V - A	400V - D	700V - S	1000V - P	

NOTE: FOR PRV RATINGS NOT LISTED USE MULTIPLE LETTERS: FOR i.e. - PB = 1200V

CIRCUIT DESIGNATOR



(Many Additional Variations Are Available Upon Request)

*Note: Circuit description is necessary when ordering stacks to this circuit configuration

22.9 SELENIUM COMPONENTS

Many of the inherent advantages of polycrystalline selenium over single-crystal germanium or silicon have gone relatively unnoticed in recent years. Yet, in certain applications General Electric's unique vacuum process, VAC-U-SEL*, selenium cells can reduce circuit component costs while assuring you of uniform quality, of high temperature operation, of excellent margins of safety, and of high reliability.

HIGH-VOLTAGE MINIATURE CARTRIDGE

A complete line of low-cost, miniature selenium rectifier diodes offer optimized application opportunities in NiCad battery charging, phonograph amplifiers, motor speed controls, and lamp dimmers.

Epoxy encapsulated, these miniatures exhibit exceptional electrical and mechanical properties. Available in a variety of standard circuit configurations including single-phase, half-wave, center-tap doublers and bridges, plus specials in cell sizes up to 15/32" round.

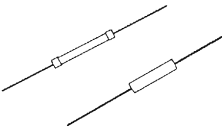
Ratings and Specifications

Current Range	**2 mA to 150 mA**
Input Voltage Range	**Up to 540 volts (RMS)**

Complete ratings and specifications available in Publication Number 180.25.

ENCAPSULATED MINIATURES

Industrial, high-voltage miniature cartridge (tubular) rectifier diodes incorporate thin cells which greatly increase function capacity in a given unit size. Metal end cap and epoxy-sealed types are available.



Applications include commercial and consumer precipitators, painting equipment, duplicating machines, automotive ignition analyzers, radiation detectors, and commercial radar sets.

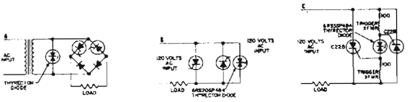
Current ratings range from 1.5 mA to 8.0 mA, and stacks are available with PRV ratings as high as 31,500 volts. Complete ratings and specifications available in Publication Numbers 180.50 and 180.51.

*Registered Trade Mark of the General Electric Company

THYRECTOR DIODES

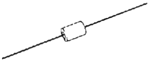
General Electric Thyrector Diodes (Transient Voltage Suppressors) have unique capabilities as voltage suppressors for guarding single-crystal rectifier diodes and transistors against damaging voltage transients.

Effective Transient Voltage Suppression With GE Thyrector Diodes
In (A) and (B) the Thyrector Diode shunts transient energy around the semiconductors while clipping voltage within semiconductor capability. In variation (C) the Thyrector Diode is connected in the gate circuit of the SCR's so that a portion of transient energy triggers the forward biased SCR into conduction, thereby protecting the reverse biased SCR from damage. This latter scheme utilizes a smaller, lower cost Thyrector Diode for a given degree of protective effectiveness.



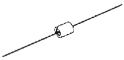
MINIATURE THYRECTORS

Available in either 9/32" or 15/32" round cells, from 30 to 600 volts (RMS). Complete ratings and specifications available in Publication Numbers 180.31 and 180.36.



ARC SUPPRESSORS

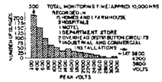
A special variation of the GE VAC-U-SEL process provides suitable characteristics for reduction of transient voltage magnitudes in solenoid circuits. Available in 9/32" and 15/32" round cell sizes. Maximum DC supply voltage per series blocking cell is 30 volts. Complete ratings and specifications available in Publication Number 180.40.

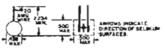


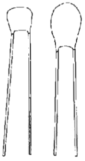
EPOXY-ENCAPSULATED THYRECTORS

Transients exist in all low-voltage distribution systems, and originate both inside and outside the system. Without protection, damage is likely to occur to all connected loads; especially semiconductors, lamps, clock motors, and other electronic devices.

Two (2), miniature, epoxy-encapsulated Thyrector Diodes have been designed specifically for application in household appliances, TV, and radio protection. They provide protection from line-conducted transient voltages having magnitudes as high as 2000 and 3000 volts, respectively. Complete ratings and specifications available in Publication Numbers 180.33 and 180.34.

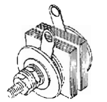






1" SQUARE THYRECTORS

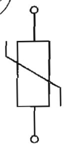
Twenty (20) sizes, from 25 to 500 volts (RMS). Through-bolt and stud mounting lockwashers and nuts. Brackets also available. Complete ratings and specifications available in Publication Numbers 180.30 and 180.35.



22.10 GENERAL ELECTRIC GE-MOV™ METAL OXIDE VARISTORS

Description:

General Electric Metal Oxide Varistors are voltage dependent, symmetrical resistors which perform in a manner similar to back-to-back zener diodes in circuit protective functions and offer advantages in performance and economics. When exposed to high energy voltage transients, the varistor impedance changes from a very high standby value to a very low conducting value thus clamping the line voltage to a safe level. The dangerous energy of the incoming high voltage pulse is absorbed by the GE-MOV varistor, thus protecting your voltage sensitive circuit components.



Electrical Symbol

GE-MOV VARISTORS–YOUR VOLTAGE TRANSIENT PROTECTION

Rating Table (Maximum Values):

Storage Temperature, T_{STG} . . . . −40°C to +125°C
Operating Surface Temperature, T_S . . . . 115°C
Operating Ambient Temperature (without derating) . . . . 85°C

Model Number	RMS Input Voltage	Recurrent Peak Voltage	Energy Rating	Average Power Dissipation Rating	Peak Current For Pulses Less Than 7 Microseconds Wide
	Volts	Volts	Joules	Watts	Amperes
VP130A10 VP130A20	130	184	10 20	0.5 0.85	1000 1250
VP150A10 VP150A20	150	212	10 20	0.5 0.85	1000 1250
VP250A20 VP250A40	250	354	20 40	0.6 0.9	1000 1250
VP420B40 VP460B40	420 460	595 650	40 40	0.9 0.9	1250 1250
VP480B40 VP480B80	480	679	40 80	0.7 1.0	1000 1250
VP510B40 VP510B80	510	721	40 80	0.7 1.0	1000 1250
VP1000B80 VP1000B160	1000	1414	80 160	0.9 1.3	1000 1250

Electrical Characteristics:

Model Number	Varistor Peak Voltage @ 1 mA AC (Peak) Min.	Varistor Peak Voltage @ 1 mA AC (Peak) Max.	Minimum Alpha* I_1 = 1 mA I_2 = 1 A	Capacitance (Typical)	Maximum Voltage Temperature Coefficient	Maximum Thermal Resistance Body-to-Air
VP	Volts	Volts	α (1–1000)	Picofarads	%/°C	°C/W
130A10 130A20	184	249		1000 2000		60 37
150A10 150A20	212	287		1000 2000		60 37
250A20 250A40	354	479		700 1400		50 35
420B40 460B40	595 650	805 880		450 450		35 35
480B40 480B80	679	914	25	430 800	−0.05	45 30
510B40 510B80	721	968		430 800		45 30
1000B80 1000B160	1414	1900		200 350		35 24

* $I = KV^{\alpha}$
where $\alpha = \text{Log}\left[\frac{I_2/I_1}{V_2/V_1}\right]$

FOR COMPLETE SPECIFICATION SEE PUBLICATION 180.59

23 APPLICATION AND SPECIFICATION LITERATURE; SALES OFFICES

General Electric semiconductor Application Notes and specification sheets provide more detailed application and device specification information than is possible in this Manual. Copies of the literature listed in Section 23.1 and as indicated in Section 23.2 may be ordered by Publication Number from:

Inquiry Clerk
General Electric Company
Semiconductor Products Department
Building 7 – Mail Drop 49
Electronics Park
Liverpool, New York 13088
USA

However, those Manuals listed as ERTM 3296, ETRM 3875A or ETR 3960A must be ordered from:

General Electric Company
Department B
3800 North Milwaukee Avenue
Chicago, Illinois 60641

A check or money order payable in US dollars must accompany each order.

Section 23.4 lists other General Electric Departments furnishing related electrical and electronic components.

23.1 SEMICONDUCTOR DEVICE CATALOGS

Two versions of this catalog abound. One is the Short Form Catalog (Publication No. 451.80). All of the devices appear in it with their condensed specifications. However, they have been arranged by application so that the "right" device for the job may be easily selected from among its brethren. Cross reference lists and selector guides further facilitate this task.

A bound Semiconductor Data Handbook is available which has more comprehensive data on each device. The price of this 1000+ page Handbook is $3.95, which includes periodic updating.

Both these catalogs can be ordered from the address following in Section 23.2.

23.2 APPLICATION NOTES

Publication Number 200.0, "Semiconductor Applications," contains abstracts of application notes, article reprints, technical papers

and application manuals listed in the following sub-sections. Particular publications which interest you may be ordered by publication number from: Inquiry Clerk, General Electric Company, Semiconductor Products Dept., Bldg. #7 Mail Drop 49, Electronics Park, Liverpool, N. Y. 13088.

23.2.1 General Applications for Power Semiconductors

- 90.16 Silicon Controlled Switches
- 90.21 How to Suppress Rate Effect in PNPN Devices
- 90.57 Using the Silicon Bilateral/Unilateral Switch
- 90.58 Reversible Ring Counter Utilizing the Silicon Controlled Switch
- 90.68 The Silicon Unilateral Switch Provides Stable, Economical Frequency Division
- 90.83 A highly Reliable, Fail Safe, Precision Undervoltage Protection Circuit
- 90.44 The Complementary SCR
- 200.1 Characteristics of Common Rectifier Circuits
- 200.5 General Electric Selenium Thyrector Diodes
- 200.9 Power Semiconductor Ratings Under Transient and Intermittent Loads
- 200.10 Overcurrent Protection of Semiconductor Rectifiers
- 200.15 Turn Off Time Characterization and Measurement of Silicon Controlled Rectifiers
- 200.19 Using Low Current SCR's
- 200.28 The Rating of SCR's When Switching Into High Currents
- 200.30 Capacitor Input Filter Design With Silicon Rectifier Diodes
- 200.32 A Variety of Mounting Techniques for Pres-Fit SCR's and Rectifiers
- 200.34 The Light Activated SCR
- 200.35 Using the Triac for Control of AC Power
- 200.36 The Solid State Thyratron
- 200.38 Application of Fast Recovery Rectifiers
- 200.39 The Series Connection of Rectifier Diodes
- 200.42 Commutation Behaviour of Diffused High Current Rectifier Diodes
- 200.50 Mounting Press Pak Semiconductors
- 200.55 Thermal Mounting Considerations for Plastic Power Semiconductor Packages
- 201.23 SCR – Ignitron Comparison
- 660.13 The Rating and Application of SCR's Designed for Power Switching at High Frequencies
- 660.14 Basic Magnetic Functions in Converters and Inverters Including New Soft Commutation
- 660.15 SCR Inverter Commutated by an Auxiliary Impulse
- 660.16 An SCR Inverter with good Regulation and Sine-Wave Output
- 660.21 Take the Guesswork Out of Fuse Selection
- 671.1 Economy Power Semiconductor Applications
- 671.12 Optimum Solid State Control Parameters for Improved Performance of In-Space Electric Heating Systems

ETRM-3875 Silicon Controlled Rectifier Manual, 5th Ed., $3.00
ETRM-3960 G-E Electronic Experimenter Circuit Manual ($2.00)

23.2.2 Silicon Controlled Rectifier and Other Thyristor Circuits

200.18 Fluorescent Lamp Dimming With SCR's and Associated Semcionductors
200.21 Three Phase SCR Firing Circuits for DC Power Supplies
200.31 Phase Control of SCR's With Transformer and Other Inductive AC Loads
200.33 Regulated Battery Chargers Using the Silicon Controlled Rectifier
200.43 Solid State Control for DC Motors Provides Variable Speed With Synchronous – Motor Performance
200.44 Speed Control for Shunt-Wound Motors
200.47 Speed Control for Universal Motors
200.48 Flashers, Ring Counters and Chasers
200.49 A Low-Cost, Ultrasonic-Frequency Inverter Using A Single SCR
200.53 Solid-State Incandescent Lighting Control
200.54 Design of Triggering Circuits for Power SCR's
200.58 Solid State Electric Heating Controls
201.1 A Plug-In Speed Control for Standard Portable Tools and Appliances
201.6 Touch Switch or Proximity Detector
201.9 Precision Temperature Controller
201.10 Auto, Boat, or Barricade Flasher
201.11 Time-Delay Relay
201.12 500 Watt AC Line Voltage and Power Regulator
201.13 Universal Motor Control With Built-in Self-Timer
201.14 Two Automatic Liquid Level Controls
201.15 Solid-State Control for Electric Blankets
201.16 Fan Motor Speed Control – "Hi-Intensity" Lamp Dimmer
201.17 Sequential Turn Signal System for Automobiles
201.18 High Voltage Power Supply for Low Current Applications
201.24 Thyristor Selection for Incandescent Lamp Loads

23.2.3 Unijunction Applications

90.10 The Unijunction Transistor Characteristics and Applications
90.12 Unijunction Temperature Compensation
90.19 Unijunction Frequency Divider
90.70 The D13T – A Programmable Unijunction Transistor
90.72 Complementary Unijunction Transistors

23.2.4 Test Circuits

201.3 Portable SCR and Silicon Rectifier Tester

23.3 SPECIFICATION SHEETS

The device specification sheets referred to on the condensed specifications of Chapter 22, and others that may be mentioned in this Manual, may be ordered by Publication Number from:

Inquiry Clerk
General Electric Company
Semiconductor Products Department
Building 7 – Mail Drop 49
Electronics Park
Liverpool, New York 13088
USA

23.4 RELATED GENERAL ELECTRIC DEPARTMENTS

The Semiconductor Products Department would like to remind its readers of the great variety of parts and services that our sister departments in General Electric can furnish to meet your SCR circuit needs. Among them are:

– SCR Capacitors for phase control and inverter commutation duty (GE Industrial and Power Capacitor Products Dept., Hudson Falls, N. Y.
– Transformer and chokes for inverters and power supply needs (GE Specialty Transformer Dept., Ford Wayne, Ind.)
– A complete family of GE cadmium sulfide cells and magnetic reed switches (GE Tube Products Dept., Owensboro, Ky.)
– A wide variety of electronic capacitors and rechargeable nickle-cadmium batteries (Electronic Capacitor and Battery Products Department, Irmo, S. C.)
– A complete family of high-reliability lamps and light emitting diodes for activation of light-activated SCR's (GE Miniature Lamp Dept., Cleveland, Ohio)
– Silicone potting and joint compounds (GE Silicone Products Dept., Waterford, N. Y.)
– And, of course, the industry's most complete line of motors and other related electrical and electronic equipment

23.5 GENERAL ELECTRIC SALES OFFICES

All products of the Industrial and Power Capacitor Products, Electronic Capacitor and Battery Products, Semiconductor Products, Specialty Transformer and Tube Products Departments as well as the light emitting diodes of the Miniature Lamp Department are sold through General Electric's Electronics Components Sales Department (ECSD) and through Component Sales Department (CSD) to original equipment manufacturers (OEM's) and distributors of electrical/electronic equipment and components. OEM Sales Offices of ECSD and CSD are listed below:

State	Electronic Components Sales Department	Component Sales Department
Alabama:		Birmingham 35202 2151 Highland Ave. P.O. Box 2602 205 322-7683
Arizona:	Phoenix 85012 United Bank Bldg. 3550 N. Central Ave. 602 264-1751	Phoenix 85012 United Bank Bldg. 3550 N. Central Ave. 602 264-1751
Arkansas:		North Little Rock 72119 2nd and Main Sts. P.O. Box 5641 501 376-3458
California:	Los Angeles 90064 11840 W. Olympic Blvd. 213 272-8566	Burlingame 94010 25 Edwards Court 415 692-0700
	Portola Valley 94025 3210 Alpine Rd. 415 854-4010	Los Angeles 90015 1543 W. Olympic Blvd. 213 381-1247
Colorado:	Denver 80206 201 University Blvd. P.O. Box 2331, 80201 303 388-5771	Denver 80206 201 University Blvd. P.O. Box 2331, 80201 303 388-4545
Connecticut:	Bridgeport 06602 1285 Boston Ave. 203 334-1012	Meriden 06450 1 Prestige Dr. P.O. Box 910 203 238-0791
District of Columbia:	Washington 20005 777-14th St., NW 202 393-3600	
Florida:	North Palm Beach 33403 321 North Lake Blvd. 305 844-5202	Tampa 33609 2106 S. Lois Ave. P.O. Box 10577 813 877-8311
	Tampa 33609 2104 S. Lois Ave. P.O. Box 10577 813 877-8311	
	Winter Park 32789 John Hancock Bldg. 370 Wymore Rd. 305 647-2030	

State	ECSD	CSD
Georgia:	Atlanta 30329 1699 Tully Circle, N.E 404 633-4522	Atlanta 30309 1860 Peachtree Rd., N.W. P.O. Box 4659, 30302 404 351-4400
Illinois:	Chicago 60641 3800 N. Milwaukee Ave. 312 777-1600	Oak Brook 60521 Oakbrook North 1200 Harger Rd. 317 654-2960
Indiana:	Ft. Wayne 46806 6001 S. Anthony Blvd. 219 447-1511	Evansville 47714 2709 Washington Ave. P.O. Box 3357, 47701 812 477-8821
	Indianapolis 46208 3750 N. Meridian St. 317 923-7221	Ft. Wayne 46804 1635 Broadway Bldg. 18-5 219 743-7431
		Indianapolis 46240 55 Winterton 1010 E. 86th St. P.O. Box 40216 317 846-6564
		South Bend 46601 430 N. Michigan St. 219 234-4196
Iowa:	Cedar Rapids 52401 210 Second St., SE 303 Dows Bldg. 319 364-9149	Bettendorf 52722 2435 Kimberly Rd. 314 359-0351
		Des Moines 50322 7200 Hickman Rd. P.O. Box 3809 Urbandale Branch 515 278-0451
Kansas:		Overland Park 66204 7219 Metcalf Ave. --- Mailing Address: Shawnee Mission 66201 P.O. Box 408 913 262-0442
Louisiana:	New Orleans 70112 National Bank Bldg. 613 Hibernia 504 525-4324	

State	ECSD	CSD
Massachusetts:	Wellesley 02181 1 Washington St. 617 237-2050	Wellesley 02181 1 Washington St. 617 237-2050
Michigan:	Southfield 48075 22255 Greenfield Road 313 355-4400	Grand Rapids 49508 2821 Madison Ave., S.E. P.O. Box 710 616 452-2121
		Southfield 48075 Box 1316 Northland Center Station 313 872-2600
Minnesota:	Minneapolis 55442 4900 Viking Dr. 612 927-5458	Minneapolis 55435 4018 West 65th St. 612 927-8814
Missouri:	Kansas City 64199 911 Main St. P.O. Box 13566 816 221-4033	St. Louis 63101 1015 Locust Street 314 436-4343
	St. Louis 63132 1530 Fairview 314 429-6941	
New Jersey:	Clifton 07014 200 Main Ave. 201 472-8100	East Orange 07017 56 Melmore Gardens 201 675-9426
New York:	Albany 12205 11 Computor Dr., West 518 458-7755	Mattydale 13211 5858 E. Malloy Rd. 315 456-7432
	East Syracuse 13057 7 Adler Dr. 315 456-1046	
	Great Neck 11021 425 Northern Blvd. 516 466-8800	Rochester 14618 3380 Monroe Ave. P.O. Drawer C 12 Corners Branch 716 586-6474
	Rochester 14624 35 Deep Rock Rd. 716 436-3480	

State	ECSD	CSD
North Carolina:	Charlotte 28211 2915 Providence Rd. 704 364-6313	Charlotte 28207 141 Providence Rd. P.O. Box 1969, 28207 704 375-5571
	Greensboro 27408 1828 Banking St. P.O. Box 9476 919 273-6982	
Ohio:	Cincinnati 45206 2621 Victory Pkwy 513 281-2547	Cincinnati 45206 2621 Victory Pkwy 513 861-3400
	Cleveland 44117 25000 Euclid Ave. 216 266-2900	Cleveland 44116 20950 Center Ridge Rd. 216 333-0552
	Dayton 454439 3430 S. Dixie Hway P.O. Box 2143 Kettering Branch 45429 513 298-0311	Dayton 45439 3430 S. Dixie Hway P.O. Box 2143 Kettering Branch 45429 513 298-0311
		Mansfield 44902 166 Park Ave., West 419 524-2622
		Toledo 43606 3450 West Central Ave. 419 531-8943
Oklahoma:	Oklahoma City 73112 3022 Northwest Expway 405 943-9015	3315 E. 47th Place Tulsa 74135 Suite 100 918 743-8451
Oregon:		Portland 97210 2929 N.W. 29th Ave. P.O. Box 909, 97207 503 228-0281

State	ECSD	CSD
Pennsylvania:	Erie 16505 2318 West 8th St. 814 455-8377	Fort Washington 19034 1260 Virginia Drive 215 643-1633
	Philadelphia 19102 3 Penn Center Plaza 215 568-1800	Pittsburgh 15234 Lebanon Shops 300 Mt. Lebanon Blvd. 412 531-6655
	Pittsburgh 15220 875 Greentree Rd. 3 Parkway Center 412 921-4134	York 17403 1617 E. Market St. 717 848-2828
Tennessee:		Chattanooga 37411 5800 Bldg., Eastgate Ctr. 615 894-2550
		Nashville 37204 2930 Sidco Dr. 615 254-1187
Texas:	Dallas 75205 4447 N. Central Expway 214 521-1931	Dallas 75247 8101 Stemmons Freeway P.O. Box 5821, 75222 214 631-3110
	Houston 77006 3110 Southwest Freeway 713 524-3061	Houston 77027 4219 Richmond Ave. P.O. Box 22045 713 623-6440
Virginia:	Charlottesville 22903 2007 Earhart St. P.O. Box 319 703 296-8118	
	Portsmouth 23707 810 Loudoun Ave. P.O. Box 7135 703 484-3521 ext 628	
Washington:	Seattle 98188 225 Tukwila Pkwy 206 244-7750	
Wisconsin:	Milwaukee 53202 615 E. Michigan St. 414 271-5000	Milwaukee 53226 Mayfair Plaza 2421 N. Mayfair Rd. 414 778-0259

23.6 INTERNATIONAL GE SALES OFFICES

In Canada, address inquiries to:
Canadian General Electric Co.
189 Dufferin St.
Toronto, Ontario, Canada
416 534-6311

ENGLAND
International General Electric
Company of New York, Ltd.
Lincoln House
296-302 High Holborn
London W. C. 1
Telephone 01-242-6868

SPAIN
International General Electric
Company of Spain, S.A.
Apartado 700
Avenida Jose Antonio
Madrid
Telephone 247.16.05

JAPAN
General Electric Japan, Limited
11-41, 1-chome
Akasaka, Minato-ku
Tokyo
Telephone 582-0371

MEXICO
General Electric de Mexico, S.A.
Apartado 53-983
Marina Nacional No. 365
Mexico 17 D.F.
Telephone 545-63-60

ITALY
Compagnia Generale di Elettricita
S.p.A.
Via F. Casita 44
Milan
Telephone 63-93-64

SWEDEN
International General Electric AB
Gardsfogdevagen 14, 11
161 70 Bromma
Telephone 28-29-45

GERMANY
General Electric-Germany
Postfach 3011
Eschersheimer Landstrasse 60-62
6 Frankfurt/Main 1
Telephone 611-1564-35

General Electric-Germany
Hermann Lingg Strasse 12
Munich 15
Telephone 537970

FRANCE
International General Electric
France, S.A.
42 Avenue Montaigne
Paris-8e.
Telephone 225-52-32

AUSTRALIA
Australian General Electric Pty.
Ltd.
103 York Street
Sydney, N.S.W., 2000
Telephone 29-8711; 29-7553

23.7 GENERAL ELECTRIC SEMICONDUCTOR DISTRIBUTORS

The distributor houses listed below have in stock the broad line of GE semiconductors. They also carry many other GE electronic components so that you may secure a wide variety of parts on a single order from a single source. Also don't forget to consult the "Yellow Pages" of your telephone directory for possible address changes or new additions.

ALABAMA

CRAMER/EW HUNTSVILLE
Huntsville, (205) 539-5722

FORBES DISTRIBUTING CO.
Birmingham, (205) 251-4104

ARIZONA

HAMILTON/AVNET ELECTRONICS
Phoenix, (602) 269-1391

KIERULFF ELECTRONICS, INC.
Phoenix, (602) 273-7331

ARKANSAS

CARLTON-BATES CO.
Little Rock, (501) 375-5375

CALIFORNIA

BRILL ELECTRONICS
Oakland, (415) 834-5888

CRAMER/LOS ANGELES
Glendale, (213) 243-6224

CRAMER/SAN FRANCISCO
Redwood City, (415) 365-4000

ELECTRONIC SUPPLY
Riverside, (213) 683-8110

ELMAR ELECTRONICS
Mountain View, (415) 961-3611

HAMILTON/AVNET ELECTRONICS
Culver City, (213) 870-7171
Mountain View, (415) 961-7000
San Diego, (714) 279-2421

KIERULFF ELECTRONICS, INC.
Los Angeles, (213) 685-5511
Palo Alto, (415) 968-6292
San Diego, (714) 278-2112

G. S. MARSHALL CO.
El Monte, (203) 686-0141
San Diego, (714) 278-6350

WESTERN RADIO & TV SUPPLY
San Diego, (714) 239-0361

COLORADO

DENVER WALKER ELECTRONICS
Denver, (303) 935-2401

ELECTRONIC PARTS CO.
Denver, (303) 266-3755

HAMILTON/AVNET ELECTRONICS
Denver, (303) 433-8551

CONNECTICUT

BOND RADIO ELECTRONICS, INC.
Waterbury, (203) 753-1184

CRAMER/CONNECTICUT
North Haven, (203) 239-5641

FLORIDA

CRAMER/EW HOLLYWOOD
Hollywood, (305) 923-8181

CRAMER/EW ORLANDO
Orlando, (305) 841-1550

HAMILTON/AVNET
Hollywood, (305) 925-5401

HAMMOND ELECTRONICS
Orlando, (305) 241-6601

SCHWEBER ELECTRONICS
Hollywood, (305) 927-0511

GEORGIA

CRAMER/EW ATLANTA
Atlanta, (404) 451-5421

JACKSON ELECTRONICS CO.
Atlanta, (404) 355-2223

ILLINOIS

ELECTRONIC DISTRIBUTORS, INC.
Chicago, (312) 283-4800

HAMILTON/AVNET ELECTRONICS
Schiller Park, (312) 678-6310

NEWARK ELECTRONICS CORP.
Chicago, (312) 638-4411

SEMICONDUCTOR SPECIALISTS, INC.
Elmhurst Industrial Park, (312) 279-1000

INDIANA

FT. WAYNE ELECTRONICS
Ft. Wayne, (219) 742-4346

GRAHAM ELECTRONICS, INC.
Indianapolis, (317) 634-8486

HUTCH AND SON
Evansville, (812) 425-7155

SEMICONDUCTOR SPECIALISTS, INC.
Indianapolis, (317) 243-8271

IOWA

DEECO, INC.
Cedar Rapids, (319) 365-7551

KANSAS

HAMILTON/AVNET ELECTRONICS
Prairie Village, (913) 362-3250

INTERSTATE ELECTRONICS SUPPLY CORP.
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KENTUCKY

P. I. BURKS CO.
Louisville, (502) 583-2871

LOUISIANA

EPCOR
New Orleans, (504) 486-7441

RALPH'S OF LAFAYETTE
Lafayette, (318) 234-4507

STERLING ELECTRONICS, INC.
New Orleans, (504) 522-8726

MAINE

HOLMES DISTRIBUTORS, INC.
Portland, (207) 774-5901

MARYLAND

CRAMER/EW BALTIMORE
Baltimore, (301) 354-0100

CRAMER/EW WASHINGTON
Gaithersburg, (301) 948-0110

HAMILTON/AVNET ELECTRONICS
Hanover, (301) 796-5000

KANN-ELLERT ELECTRONICS, INC.
Baltimore, (301) 889-4242

PIONEER/WASHINGTON
Rockville, (301) 424-3300

SCHWEBER ELECTRONICS
Rockville, (301) 427-4977

MASSACHUSETTS

CRAMER ELECTRONICS, INC.
Newton, (617) 969-7700

HAMILTON/AVNET
Burlington, (617) 272-3060

T. F. CUSHING, INC.
Springfield, (413) 788-7341

GERBER ELECTRONICS
Dedham, (617) 329-2400

SCHWEBER ELECTRONICS
Waltham, (617) 891-8484

MICHIGAN

NEWARK–INDUSTRIAL ELECTRONICS CORP.
Grand Rapids, (616) 452-1411

RS ELECTRONICS
Detroit, (313) 491-1012

SEMICONDUCTOR SPECIALISTS, INC.
Detroit, (313) 255-0300

MINNESOTA

GOPHER ELECTRONICS CO.
St. Paul, (612) 645-0241

LEW BONN COMPANY
Edina, (612) 941-2770

SEMICONDUCTOR SPECIALISTS, INC.
Minneapolis, (612) 866-3434

MISSISSIPPI

ELLINGTON ELECTRONICS SUPPLY, INC.
Jackson, (601) 355-0561

MISSOURI

HAMILTON/AVNET ELECTRONICS
Hazelwood, (314) 731-1144

L COMP–KANSAS CITY
North Kansas City, (816) 221-2400

NORMAN ELECTRONIC SUPPLY
Joplin, (417) 624-0368

OLIVE INDUSTRIAL ELECTRONICS
University City, (314) 863-4051

RADIO LAB., INC.
Kansas City, (816) 561-9935

NEBRASKA

RADIO EQUIPMENT CO.
Omaha, (402) 341-7700

SCOTT ELECTRONIC SUPPLY CORP.
Lincoln, (402) 434-8308

NEW JERSEY

CRAMER/NEW JERSEY
Union, (201) 687-7870

CRAMER/PENNSYLVANIA
Pennsauken, (609) 662-5061

GENERAL RADIO SUPPLY CO., INC.
Camden, (609) 964-8560

HAMILTON/AVNET ELECTRONICS
Cedar Grove, (201) 239-0800
Cherry Hill, (609) 662-9337

NEW MEXICO

CRAMER/NEW MEXICO
Albuquerque, (505) 265-5767

ELECTRONICS PARTS CO.
Albuquerque, (505) 265-8401

KIERULFF ELECTRONICS, INC.
Albuquerque, (505) 268-3901

NEW YORK

ARROW ELECTRONICS, INC.
Farmingdale, (516) 694-6800

CRAMER/BINGHAMTON
Binghamton, (607) 754-6661

CRAMER/LONG ISLAND
Hauppauge, (516) 231-5600

CRAMER/ROCHESTER
Rochester, (716) 275-0300

CRAMER/SYACUSE
Syracuse, (315) 437-6671

HAMILTON ELECTRO SALES
Syracuse, (315) 437-2641
Westbury, (516) 333-5800

ROCHESTER RADIO SUPPLY CO.
Rochester, (716) 454-7800

ROME ELECTRONICS, INC.
Rome, (315) 337-5400

SCHWEBER ELECTRONICS
Westbury, L.I., (516) 334-7474

STANDARD ELECTRONICS, INC.
Buffalo, (716) 883-5000
Endicott, (607) 754-3102

VALLEY INDUSTRIAL ELECTRONICS, INC.
Yorkville, (315) 736-3393

NORTH CAROLINA

CRAMER/EW WINSTON-SALEM
Winston-Salem, (919) 725-8711

DIXIE RADIO SUPPLY CO.
Charlotte, (704) 377-5413

SOUTHEASTERN RADIO SUPPLY CO., INC.
Raleigh, (919) 828-2311

OHIO

ELECTRONICS MARKETING CORP.
Columbus, (614) 299-4161

HUGHES-PETERS, INC.
Cincinnati, (513) 351-2000
Columbus, (614) 294-5351

PIONEER–CLEVELAND
Cleveland, (216) 587-3600

PIONEER/DAYTON
Dayton, (513) 236-9900

REM ELECTRONICS SUPPLY
Warren, (216) 399-2777

SUN RADIO CO., INC.
Akron, (216) 434-2171

WARREN RADIO CO.
Toledo, (419) 448-3364

OKLAHOMA

OIL CAPITOL ELECTRONICS CORP.
Tulsa, (918) 836-2541

TRICE WHOLESALE ELECTRONICS
Oklahoma City, (405) 524-4415

PENNSYLVANIA

ALMO ELECTRONICS CORP.
Philadelphia, (215) 676-6000

RESCO OF LEHIGH VALLEY
Allentown, (215) 435-6743

ROSEN ELECTRONICS CO.
York, (717) 843-3875

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APPLICATION INDEX

The circuits referred to in the following figure numbers are intended as a starting point for the equipment designer in achieving the detailed requirements of his application. Since these circuits are not necessarily "ultimate" for every application, it is hoped the imaginative designer will use them simply as a jumping-off point for his own development. Likewise, many of these circuits can be used for other functions besides those mentioned in the text. As a guide to some of the various thyristor circuits for accomplishing specific tasks, here is a tabulation of figures in this manual classified by possible application (please note that these are *Figure* numbers and not section or paragraph numbers):

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